1963 INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

Wednesday, Thursday and Friday—February 20, 21, 22, 1963

IEEE Professional Technical Group on Circuit Theory . . IEEE Philadelphia Sections . . IEEE Electronic Circuits and Systems Committee . . University of Pennsylvania

DIGEST of TECHNICAL PAPERS

Irvine Auditorium and University Museum, University of Pennsylvania

Sheraton Hotel, Philadelphia, Pa.

1963 INTERNATIONAL

SOLID-STATE CIRCUITS CONFERENCE

DIGEST of TECHNICAL PAPERS

First Edition

February, 1963

Publisher: Lewis Winner, New York 36, N. Y.

1963 International Solid-State Circuits Conference

DIGEST OF TECHNICAL PAPERS

PRINTED IN THE UNITED STATES OF AMERICA

Library of Congress Catalog Card No.: 59-44023

Volume VI

Editor: V. R. Saari

Associate Editors: C. J. Byrne..J. J. Kassig..D. Leenov..A. A. Geigel **Assistant Editor:** B. K. Winner

Consulting Editor: Lewis Winner

Foreword

A Decade of Achievement

WELCOME to the tenth anniversary of our annual conferences. Originating as a meeting devoted to transistor circuits, the scope of these conclaves has been gradually expanded to include all areas of solid-state applications: semiconductor, superconductive, ferroelectric, ferromagnetic and optical.

An interesting observation one can make is the considerable overlap of interests that has developed between device and circuit physicists and engineers during this period. When the only active devices available were relays, magnetic amplifiers and electron tubes, it was possible for device designers to pursue their programs with only occasional contact with those involved in circuit developments. Similarly, circuit designers were able to utilize active devices by treating them as black boxes with specified external characteristics. With the advent of the solid-state era, this situation was altered considerably. It was soon realized that completely new design techniques and circuit concepts would be required to exploit fully the unique properties of solid-state devices. The emerging fields of nonlinear circuit design, active network synthesis, microwave amplification, digital memories and wideband amplifier design have accented this requirement. These activities have created new directions for circuit designers and a corresponding heightened need for detailed information on device characteristics and operational theory.

Device designers have also recognized that to make optimum use of their technology, they require more knowledge of the circuit applications of their devices. Microelectronics represents a timely example of the rewarding results obtained through the close cooperation of circuitry and device designers. Clearly, the demarcation between circuit and device areas will become even less clear as further advances are made in the solid-state field.

Recognizing this overlap of interests, the program committee has, this year, reinstated the practice of scheduling a number of tutorial sessions. One tutorial session is concerned with the frequency and power limitations of transistors and varactors. Another is devoted to the large signal characterization of transistors and the design of transistor switching circuits. These sessions contain a rich mixture of both device physics and circuit applications.

Because of the large number of excellent papers programmed, and the addition of the two tutorial sessions, it has been necessary to increase the number of day sessions to twelve. It is hoped that the resulting increase in technical content will more than compensate for any inconvenience of the double sessions on Friday afternoon.

Franklin H. Blecher
Conference Chairman

Table of Contents

Table of Contents

Index to Authors

Index to Authors

SESSION I: Digital Memories

Chairman: A. K. Rapp

Philco Corporation, Blue Bell, Pa.

WAM 1.1: Operating Speed of Thin-Film Memories

H. J. Harloff

Siemens and Halske AG

Munich, Germany

THE MAXIMUM operating speed and size of thin-film magnetic and superconductive memories depend essentially on the transmission characteristics of the lines employed in the memories[1]. These lines are usually designed in the form of striplines, a configuration which is not only well suited to the structure of the memory modules but also warrants a relatively noisefree transmission of pulses.

The transmission characteristics of normally conducting and superconducting multilayer striplines have recently been investigated by *Swihart*[2] and *Piefke*[3]. The phase velocity and the wave attenuation depend on both the thickness of the conducting and insulating layers (Figures 1 and 2) and the frequency; Figure 3. The properties of a superconducting stripline are superior to those of a conventional stripline because ohmic line losses do not appear in superconductors, and effects of film thickness are encountered only when the film thickness is comparable with the penetration depth of the supercurrent. Therefore, phase velocity and attenuation of a superconducting stripline are mainly functions of the properties of the dielectric. Figure 3 assumes a frequency-independent dielectric constant.

A model for lines of the type occurring in thin-film memories is shown in Figure 4. In a magnetic-film memory, this model may be interpreted as a word line, crossed by n bit lines or sense lines per centimeter. In a superconductive memory, it may be looked upon as a cryotron control line, controlling n gates per centimeter. If all dimensions, except for the total length of the line, are small compared with the shortest wave length of the signals to be transmitted, the influence of the transverse lines can be accounted for in terms of evenly distributed capacitances and resistances. Thereby an equivalent circuit, as plotted on Figure 5, is obtained.

For the model shown in Figure 4, typical dimensions have been assumed for magnetic thin-film memories and for a cryotron array or a trapped-flux memory. The line characteristics for these two cases are plotted against frequency in Figure 6. In both cases the damping influence of the transverse lines becomes noticeable only at frequencies above 10^8 *cps*. The superiority of the superconductor line array is, in spite of the small film thicknesses, primarily a matter of lower attenuation.

Attenuation and phase velocity in a line, as depicted on Figure 4, depend also on the number of intersecting lines per unit of length. Generally, both the phase velocity and the range of the waves diminish as the number of transverse leads increases; Figure 7. It is, however, remarkable that under certain readily attainable conditions, the line loss of a superconductive stripline can be reduced by the addition of transverse lines with losses. This is shown by case II in Figure 7.

From Figure 7 we obtain the total number of permissible transverse lines, if we multiply the number per unit of length by the appropriate distance; 20% signal attenuation. Thus, in a magnetic thin-film memory, an upper limit for the word length (or integral multiples thereof) is established. In a cryotron array, the maximum number of cryotrons for which the stripline considered can serve as a control line is thereby fixed. Some numerical values have been summarized in table I for the examples chosen in Figure 6.

A measure of the pulse distortion in a stripline is the transient time τ. This has been calculated for table I as the reciprocal value of the maximum rising slope of a pulse which originally had an infinitely steep rise, after propagation over distance a in the stripline. Little pulse distortion results if pulses are used with a rise time of about ten times the transient time. Considered in conjunction with the maximum phase velocity in the lines, the transient time provides clues to the maximum possible operating speed of thin-film memories.

[1] Harloff, H. J., Preprint Proc. *Int'l. Fed. For Inf. Proc. Soc.*, p. 268; 1962.

[2] Swihart, J. C., "Field Solution for a Thin-Film Superconducting Strip Transmission Line," *J. Appl. Phys.* 32, p. 461; 1961.

[3] Piefke, G., *Arch. elektr. Ubertr;* to be published in 1963.

	I (normal conducting)	*II (superconducting)*
Width of the striplines; $b_1 = b_2$	*0.1 cm*	*0.02 cm*
Number n of crossing striplines *per-cm* line length	*5*	*5*
Distance a of 20% (power) attenuation; $f = 10^8$ *cps*	*66 cm*	*924 cm*
Permissible total number of crossing striplines; $a \cdot n$	*330*	*4620*
Phase velocity v; $f = 10^8$ *cps*	*10.7 cm/nsec*	*11.2 cm/nsec*
Time delay over distance a; a/v	*6.17 nsec*	*82.5 nsec*
Transient time τ	*0.12 nsec*	*1.3 nsec*

***TABLE I*—Properties of the thin-film stripline defined in Figure 6.**

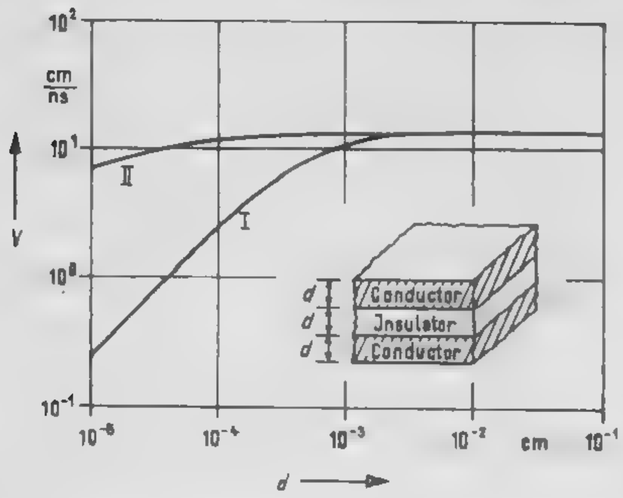


FIGURE 1—Phase velocity v versus film thickness d of infinite thin film striplines. Frequency is 10^8 *cps*; insulator $\varepsilon = 5\ \varepsilon_0$.
Conductors: I = copper, II = superconducting lead.

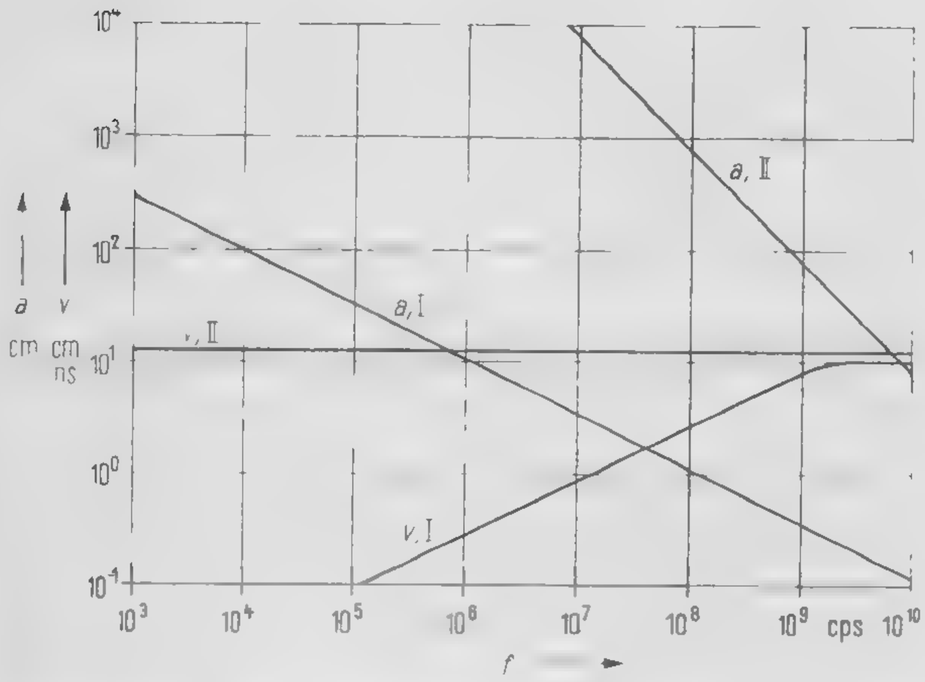


FIGURE 3—Phase velocity v and distance a of *20%* (power) attenuation versus frequency. Film thicknesses $d = 1\ \mu m$. See Figures 1 and 2 for notation.

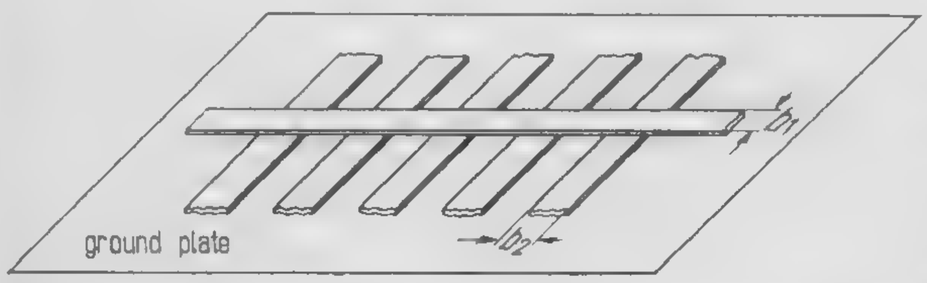


FIGURE 4—Model for stripline configurations in thin-film memories. A driving stripline crosses n driven striplines *per-cm* line length.

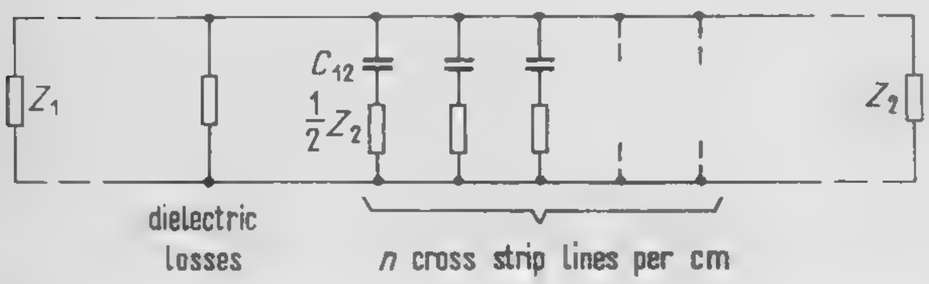


FIGURE 5—Equivalent circuit of the configuration of Figure 4: Z_1 — characteristic impedance of the driving stripline, Z_2 — characteristic impedance of the driven striplines, C_{12} — coupling capacity from the driving to a driven stripline.

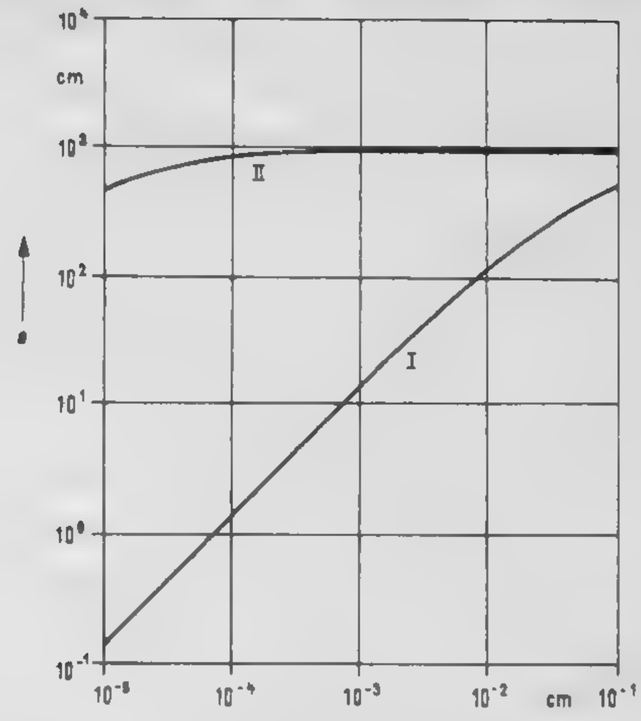


FIGURE 2—Distance a of *20%* (power) attenuation versus film thickness d. Frequency 10^8 *cps*. Notation: see Figure 1, except $\varepsilon = 5\ (1\text{-}j \cdot 10^{-2})\ \varepsilon_0$.

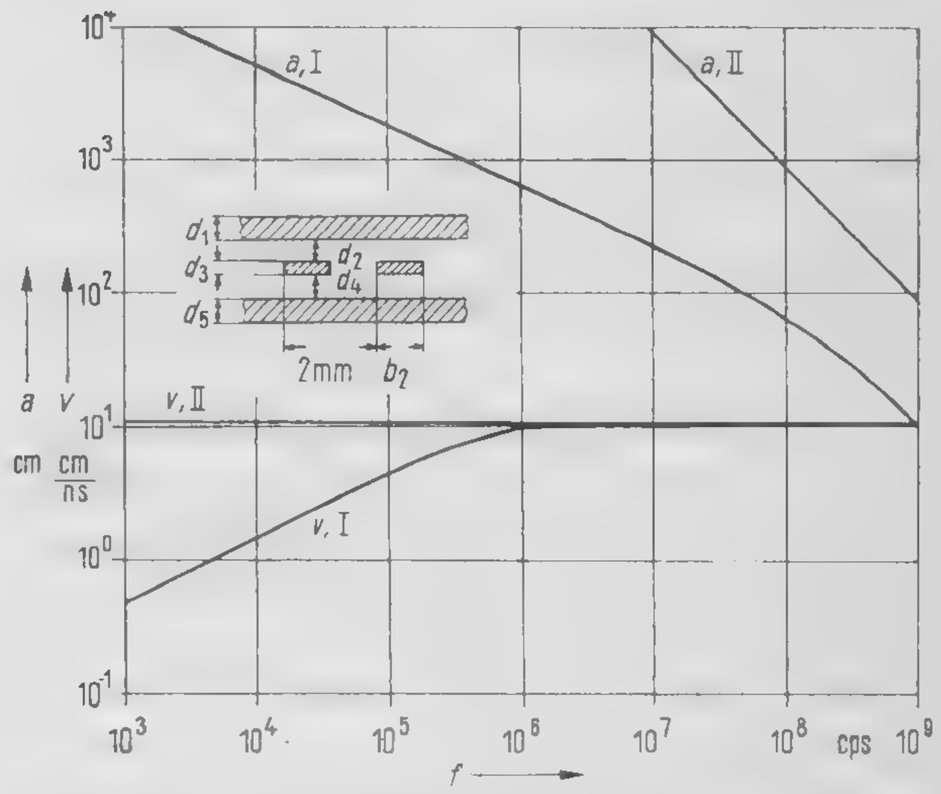


FIGURE 6—Phase velocity v and distance a of *20%* (power) attenuation versus frequency.

I. Magnetic film memory structure:
$d_1 = d_3 = 20\ \mu m$ *Cu*
$d_2 = d_4 = 20\ \mu m$, $\varepsilon = 3.5\ (1\text{-}j \cdot 10^{-2})\ \varepsilon_0$
$d_5 = 0.2$ *cm* Ag
$b_2 = 0.1$ *cm*
$n = 5$ crossing lines *per-cm*

II—Cryotron structure:
$d_1 = d_5 = 0.3\ \mu m$ Pb
$d_3 = 0.2\ \mu m$ Sn
$d_2 = d_4 = 0.5\ \mu m$, $\varepsilon = 5\ (1\text{-}j \cdot 10^{-2})\ \varepsilon_0$
$b_2 = 200\ \mu m$
$n = 5$ crossing lines *per-cm*

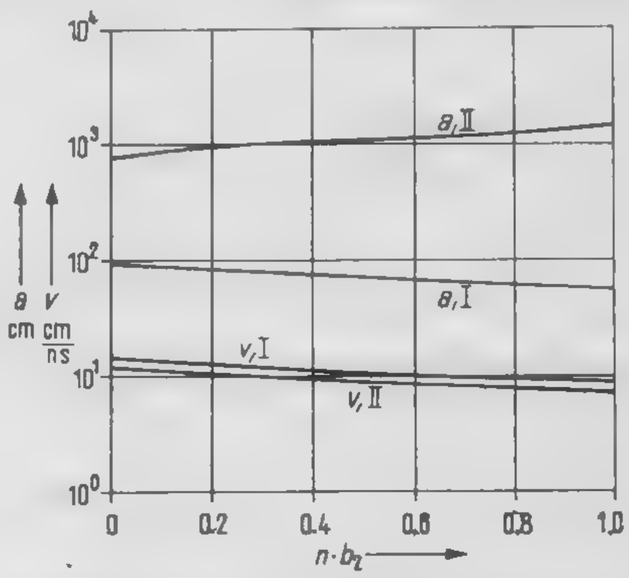


FIGURE 7—Phase velocity v and distance a of *20%* (power) attenuation versus normalized number of cross striplines. Frequency 10^8 *cps*; nb_2 filling factor, n number of cross striplines *per-cm*, b_2 width of a cross stripline. For I and II see Figure 6.

SESSION I: Digital Memories

WAM 1.2: An Application of Quantized Trapped Flux in a Superconducting Memory*

D. J. Dumin and J. F. Gibbons

Stanford University

Stanford, Calif.

RECENT EXPERIMENTAL evidence has been presented demonstrating the quantization of trapped flux in superconductors[1,2,3]. The theoretical quantum unit of flux is $\phi_q = \frac{hc}{2e} = 2.07x10^{-7}$ *gauss-cm²*. Utilizing superconductors throughout it is possible to use this fundamental effect to construct a multiple-level memory cell with non-destructive readout. This paper will describe such a memory cell and provide some experimental data on its operating characteristics.

The sample geometry is essentially that illustrated in *a* and *b* of Figure 1. The device, called the quantizer, consists of a quantizing loop and a detector. The quantizing loop (Figure 1*a*) consists of a lead ground plane upon which is evaporated a thin, narrow line of SiO. A lead bridge is deposited over the SiO and contacts the ground plane on either side of the SiO. Upon these layers, but insulated from them by SiO, is deposited a narrow piece of tin which acts as a detector; Figure 1*b*. The quantizer is covered with a layer of lead which is insulated from the trapping loop and the detector. This helps contain the fields. A photograph of a typical device is shown in c of Figure 1; corresponding elements can be compared with *a* and *b* of Figure 1.

The quantizer operates in the following manner: flux is trapped in the quantizing loop using the sequence described by *Deaver* and *Fairbank*[1]. The critical current of the tin detector is measured. When flux is trapped, the critical current of the tin detector will change due to the presence of the trapped magnetic field. Utilizing thin film technology, an SiO layer *.001"* wide and *1000Å* thick can be produced. The field associated with a flux unit under these conditions should be around *8.2 gauss*, which is not unreasonably small to detect by this method.

Five samples have been tested, and in three of them trapped flux quantization has been observed. A synopsis of the data is given in table I. The detector of sample *Q-IV* was sensitive to direction of the trapped flux, which should be expected since the detector is quite similar to an in-line cryotron, which has directional properties. It will be noted that sample *Q-V* trapped five levels of flux. The levels trapped agree within a factor of three with those calculated. A rectangular model similar to the circular model of *Keller* and *Zumino*[4] was used to calculate the flux levels.

A sample of the data taken on quantizer Q-III is shown in Figure 2. These data represent the *V-I* characteristics of the tin detector. When a quantum unit of flux is trapped the critical current of the tin should be altered. The first flux level is trapped for applied fields between *1.12* and *2.24 gauss*. The second level is trapped between *4.48* and *5.60 gauss*.

When these data are plotted as I_c versus H, a plot such as shown in Figure 3 results. On this plot the theoretically predicted values of the transition field are also shown. These values of $H_{Transition}$ are the odd-half integer values of the field associated with each flux unit. This is about where the field can be expected to trap either the upper or lower value of flux.

Additional Experiments Planned

Further experiments are to be performed on various drive mechanisms, on *ac* properties of the circuit, and on some of the fundamental physics of the device. In particular, it may be possible to use this structure to measure the flux unit versus penetration depth, flux unit versus temperature, and flux unit versus size dependences.

SAMPLE DATA	QUANTUM LEVEL	H_f (CALCULATED) IN GAUSS	H_f (MEASURED) IN GAUSS
Q-III			
t_{Pb} = 7500Å	1	2.15	$1.12 < H_f < 2.24$
d_{SiO} = 3000Å			
w_{SiO} = 0.001 IN.	2	4.30	$4.48 < H_f < 5.60$
T = 3.695°K			
Q-IV			
t_{Pb} = 500 Å	1	4.1	$2.24 < H_f < 4.48$
d_{SiO} = 1050Å			
w_{SiO} = 0.001 IN.			
T = 3.590°K			
Q-V			
t_{Pb} = 1000Å			
d_{SiO} = 1300Å			
w_{SiO} = 0.001 IN.			
T = 3.695°K	1	3.25	$6.7 < H_f < 9.0$
	2	6.5	$15.6 < H_f < 17.9$
	3	9.75	$27 < H_f < 29$
	4	13.0	$36 < H_f < 38$
	5	16.25	$42.5 < H_f < 45$

λ(0) ASSUMED TO BE 390Å AFTER SHOENBERG, D., SUPERCONDUCTIVITY, CAMBRIDGE UNIV. PRESS (1960), P.150.

TABLE 1: Compilation of five-sample data.

* Research supported under Air Force Contract No. AF 33(616)-7726.

[1] Deaver, B. S., and Fairbank, W. M., *Phys. Rev. Letters 7*, p. 43; 1961.

[2] Doll, R., and Nabauer, M., *Phys. Rev. Letters 7*, p. 48; 1961.

[3] Little, W. A., and Parks, R. D., *Phys. Rev. Letters 9*, p. 9; 1962.

[4] Keller, J. B., and Zumino, B., *Phys. Rev. Letters 7*, p. 164; 1961.

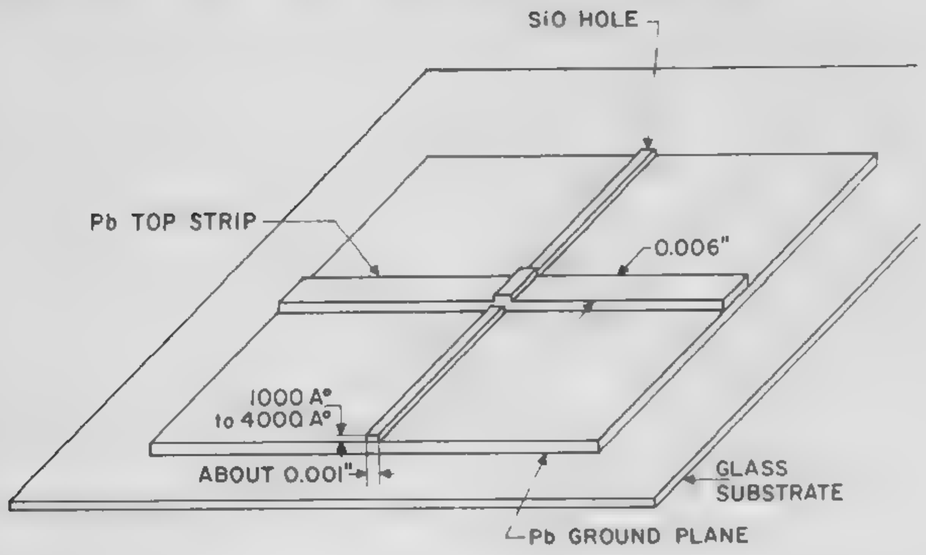


FIGURE 1a—**Basic quantizer loop; ground plane *0.040" x 0.040".***

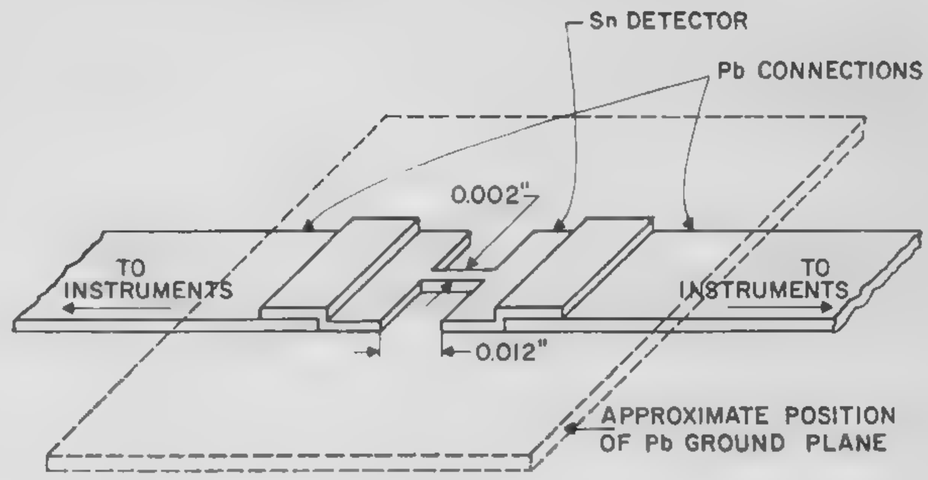


FIGURE 1b—**Detector for quantizer.**

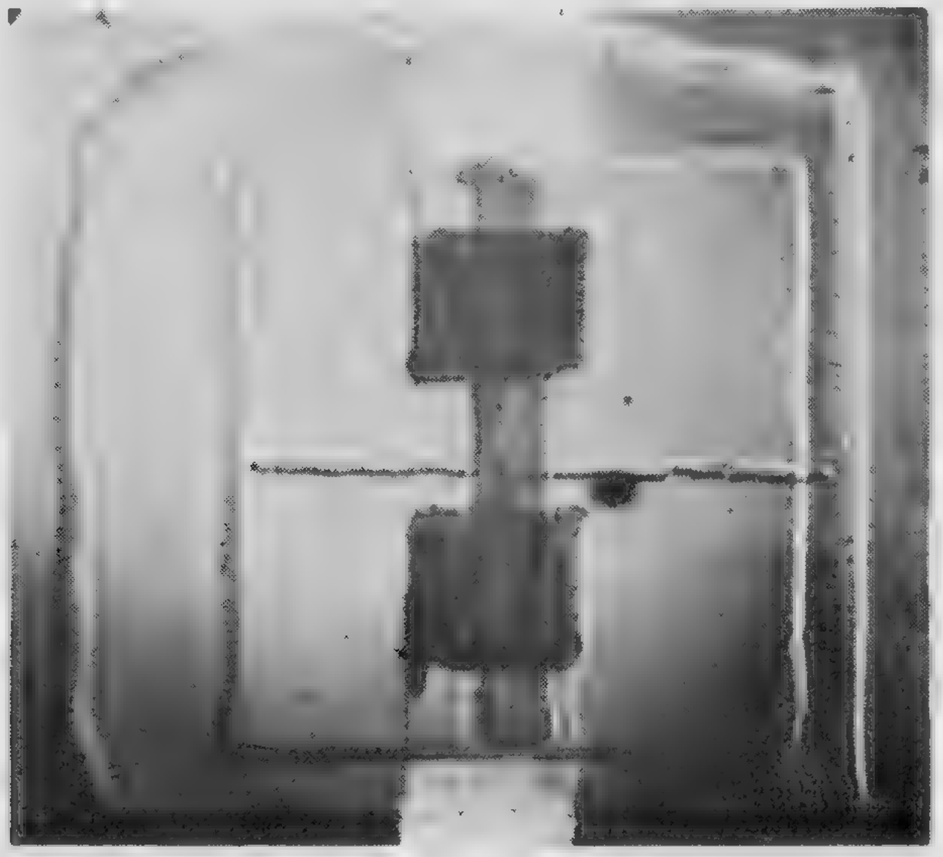


FIGURE 1c—**Photograph of a quantizer; lead ground plane is inner square *0.040" x 0.040".***

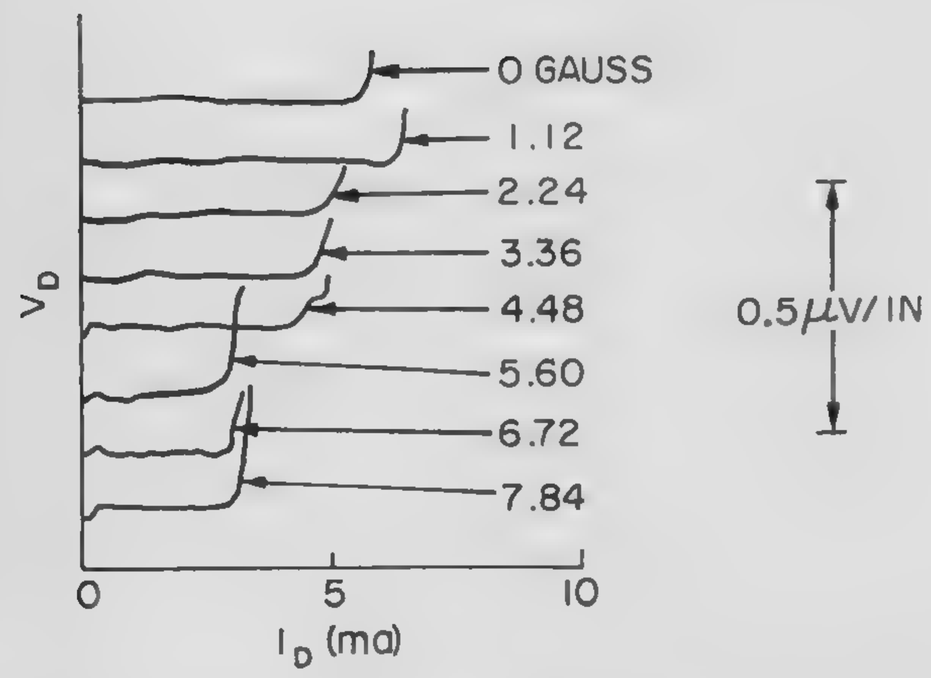


FIGURE 2—**V-I characteristic of the detector versus applied field.**

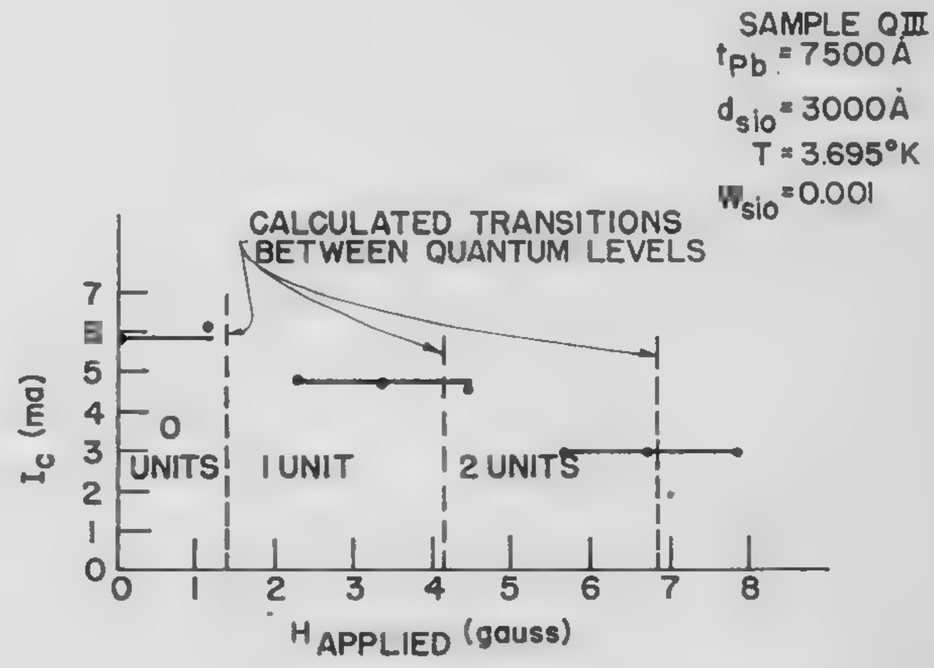


FIGURE 3—**Critical current versus flux level.**

SESSION I: Digital Memories

WAM 1.3: The Waffle Iron Store

T. R. Finch and A. H. Bobeck

Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

THIS PAPER will present a progress report on a *256*-word, *400-nsec waffle-iron* store. The memory seems eminently suited to the needs of the next generation storage systems in which the dominant requirements are considered to be: *(1)*—cycle time in the few hundred nanoseconds range, *(2)*—low-cost per-bit, *(3)*—reliable performance over a wide temperature range without manual adjustments, and *(4)*—one memory technology for destructive and nondestructive readout for variable and program store implementation.

The *waffle-iron* memory structure was described by *J. L. Smith*‡ in 1962[1]. Continued development has led to a structure primarily suited to high-speed variable store use. A soft, high-mu ferrite base plate and a thin, plated overlay of isotropic nickel-iron are used. This may be designed somewhat independently so that structural considerations that effect propagation time, drive line impedances and bit density may thus be treated separately from the overlay properties that effect cell uniformity, shuttles, and cycling speed. The structure is *open loop* for fabrications ease and low assembly cost, and *closed loop* for magnetic confinement and the control of critical interactions.

Slots are cut *5-mils* wide, *10-mils* deep on *15-mils* centers in a polished, high-permeability ferrite base plate in both word and digit directions. This results in the *waffle-iron* surface appearance with posts of *10-mils* by *10-mils* dimensions; Figure 1. Word and digit-line spacings are each *30 mils*, and the effective bit length is about *10 mils*. An overlay storage element, *97%* iron—*3%* nickel, is electroplated *50-μinches* thick on a flat copper substrate. The overlay has essentially isotropic properties and a coercive force of *9 oersteds*. An effective air gap of one *μinch* is realized along with high field efficiencies of approximately *100 oersteds* per-ampere. Four distinct and separate flux paths for each stable state provide redundancy of stored information. Flux patterns are shown in Figure 2.

The *256*-word store employs a word-organized memory using four submodules each *1⅛"* x *2¼"* x *¼"* and containing *64* word lines and *32* digit lines. The four submodules are wired into two sections of *128* words each. The digit drivers drive these two sections in parallel, and the digit detectors read through the four submodules in series. Representative contours of operation for a nominal overlay are shown in Figure 3.

The low back *emf*'s, *2-4 v*, and short propagation times, *4-9 nsec*, exhibit opportunities for large store design with circuit simplicity in drive and strobe arrangements; Figure 4. Interactions due to structural parasitics and voltage *bounce* of drive lines have been negligible problems in the *256*-word store.

Each bidirectional digit driver (Figure 5) injects a current of ± *100 ma* (write *one*, or write *zero*) into each section of *128* words. The applied digit current has a rise time of *50 nsec* and a duration of *120-150 nsec* which must overlap the word write current of *100 nsec* duration. The bipolar, ± *2 v* peak, write transient on each digit line is reduced at the input of the bipolar digit detector to approximately ± *100 mv* peak through transformer hybrid balance. The detector is single-sided and employs a current gate and tunnel-diode thresholding circuit.

The *+500 ma* read, *—350 ma* word-write current is driven through a single *16* × *16* diode matrix for the read-write operation; Figure 6. The bidirectional word drive is realized using a controlled stored charge access diode. The diodes are fabricated in multiples of eight on a single silicon chip. The design used permits a *350-ma* peak, *100-nsec* duration write current during the stored charge sweep-out interval. Negligible leakage occurs during the succeeding read operation in a different word location. Bidirectional word drivers are not required.

Preliminary data on write transients, word-digit interactions, propagation times, information sensitivities and margins with temperature indicate reliable store operation in the *200-400 nsec* cycle time, 256-1024 word size is feasible with present techniques. Development work is underway on a *1024*-word, *1-μsec* store employing a biased core access switch. It is expected that this approach will be extended to large *Waffle-Iron* stores.

Acknowledgments

Many members of the Bell Telephone Laboratories are contributing to this development project. In particular, the authors greatfully acknowledge the help of *J. L. Smith* on memory, *R. W. MacDonald* on the multiple-stored charge diodes, and *J. A. Ruff* and *J. H. Wuorinen* for circuit development.

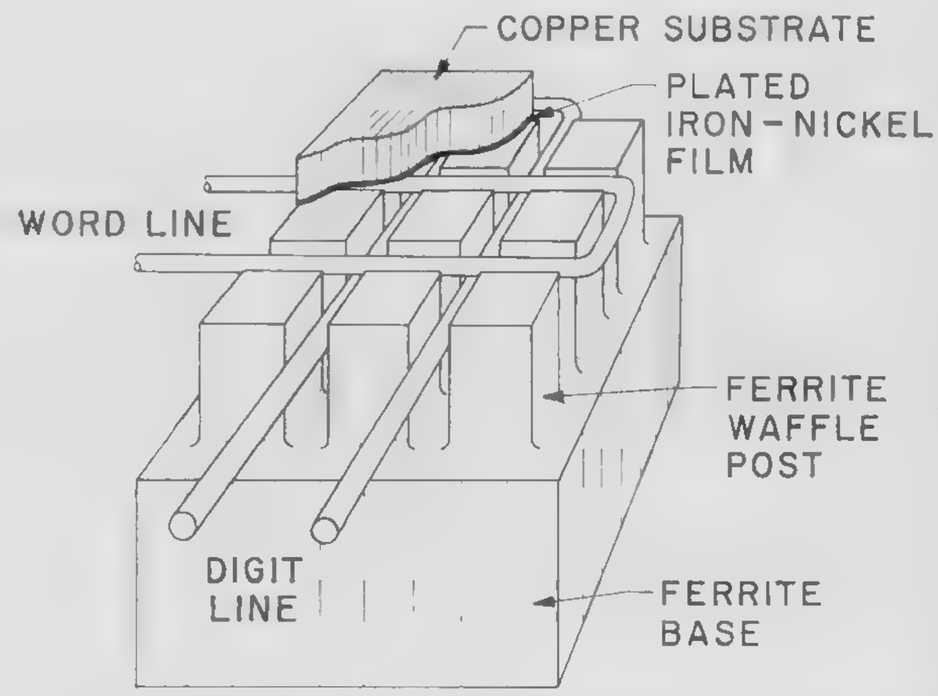


***FIGURE 1*—Waffle-Iron structure showing slotted ferrite base plate, nickel-iron overlay, one word line, and one digit line.**

‡ Bell Telephone Laboratories, Inc.

[1] Patent 2,825,891 *Magnetic Memory Device* by S. Duinker Eindhoven, Netherlands, discloses similar configurations.

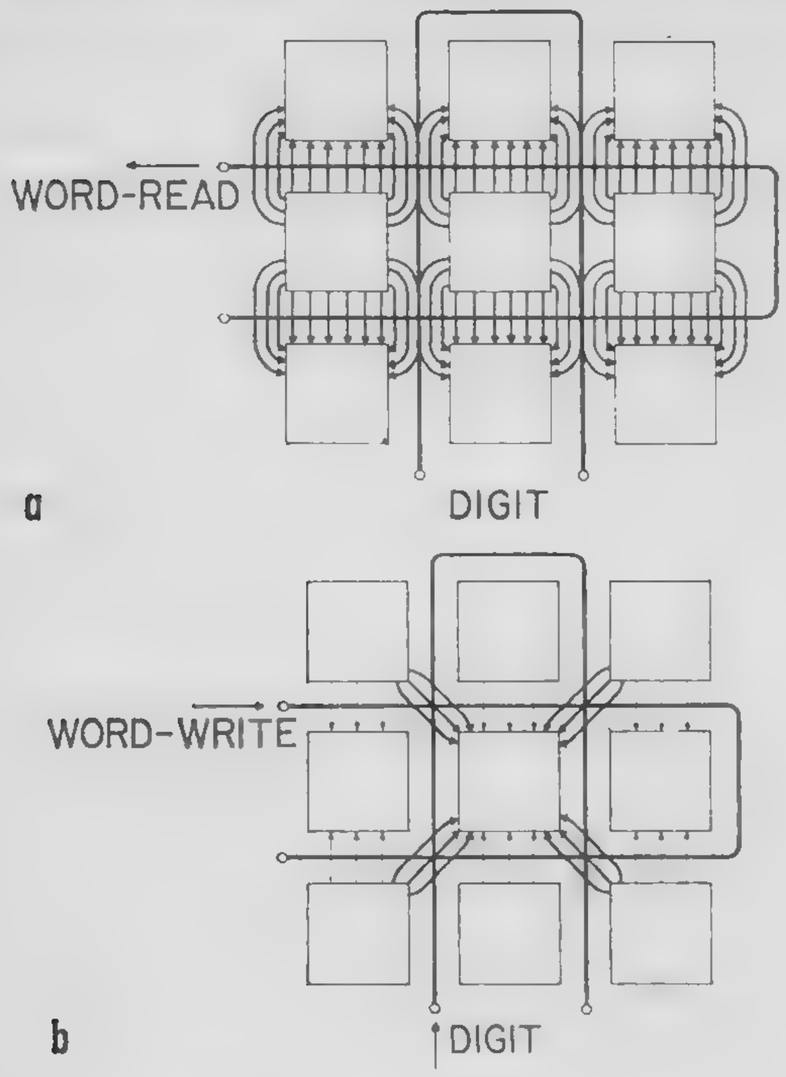


FIGURE 2—**Magnetization pattern *(a)* after a read operation; *(b)*—after a write operation showing four separate flux paths.**

CHARACTERISTIC	WORD LINE 32 DIGITS	DIGIT LINE-WRITE 256 DIGITS	DIGIT LINE-READ 256 DIGITS
LENGTH	2.4 IN	9 IN	18 IN
INDUCTANCE	0.2 UH	0.5 UH	2 UH
RESISTANCE	0.4 OHM	1.0 OHM	4 OHM
CAPACITANCE	5 UUF	40 UUF	40 UUF
PROPAGATION TIME	1.5 NS	4.5 NS	9 NS
BACK EMF	4V	2V	—
OUTPUT	—	—	±10 MV, 80NS

FIGURE 4—**Physical and operational data for a *256*-word, *32*-digit per-word memory module using drive currents with *50*-nsec rise time.**

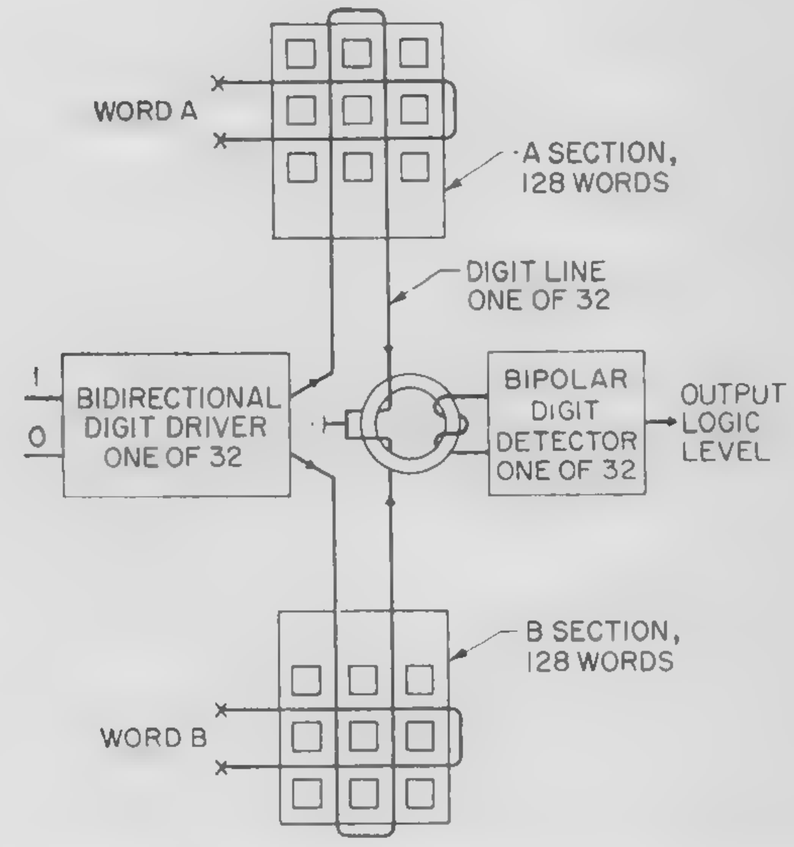


FIGURE 5—**Digit circuit. Connection arrangement for digit driver, memory submodules, and digit detectors.**

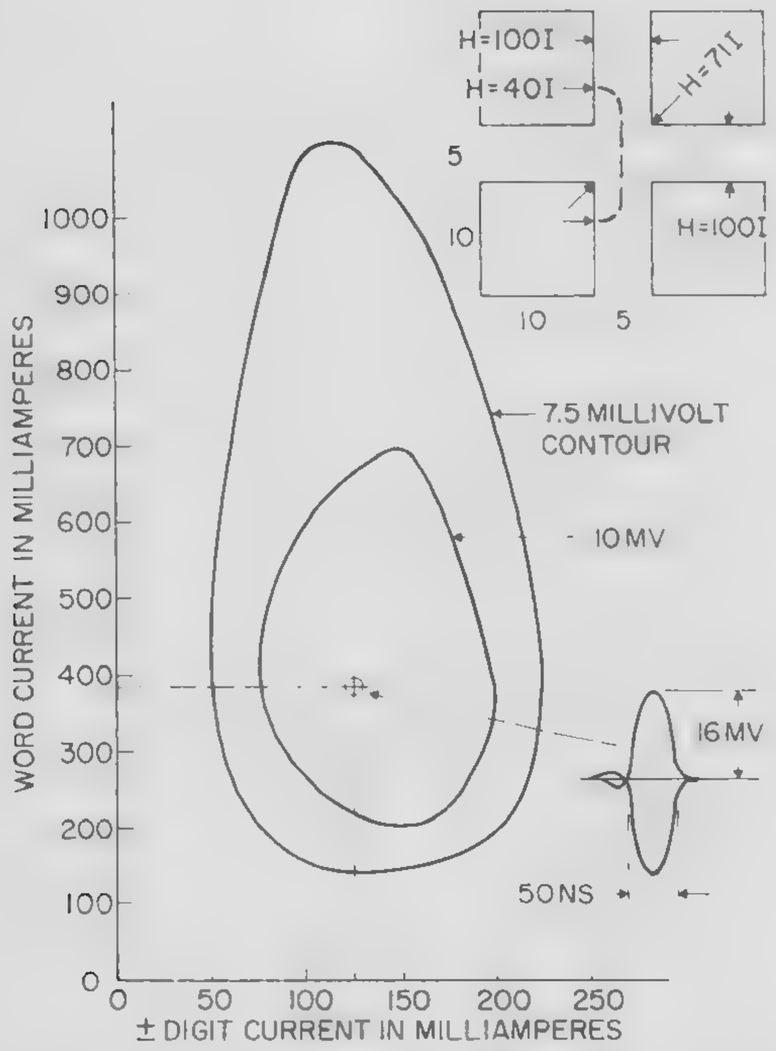


FIGURE 3—**Operating range for digit current and word current at two minimum output levels for a typical overlay. The tolerances required for drive currents and detector threshold are evidently not severe.**

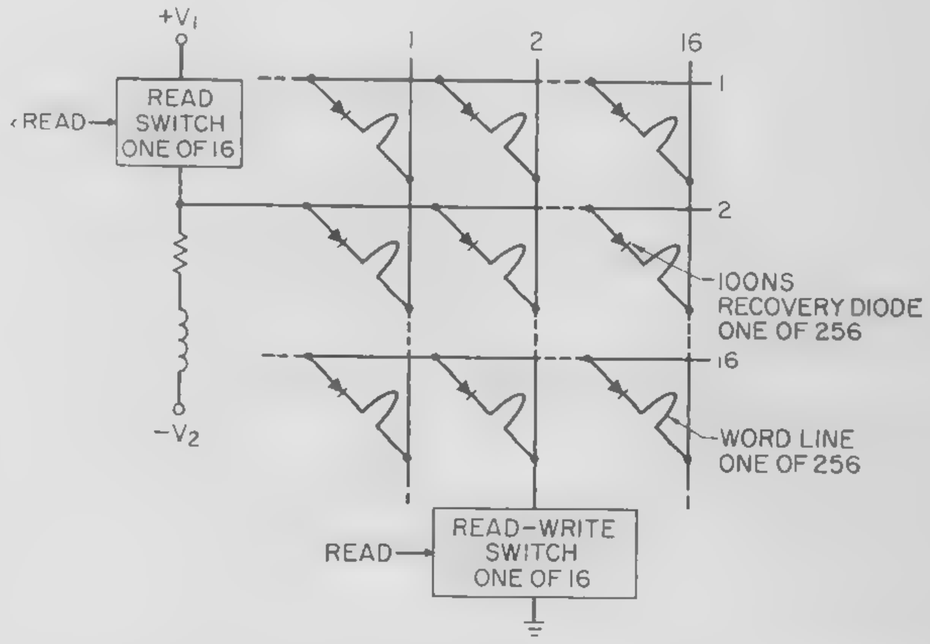


FIGURE 6—**Word circuit. Connection arrangement for driver, access diode, memory word line, and bidirectional switch. Only a single read timing pulse is used to control the read-write operation.**

SESSION I: Digital Memories

WAM 1.4: Electrical Delay-Line Memory System Using Tunnel Diodes

H. H. Harris and W. D. Pricer

Components Div., IBM Corporation

Poughkeepsie, N. Y.

THIS PAPER will describe a novel means of achieving fast high-capacity information storage with electrical delay lines and simple regeneration circuitry. Information storage at bit rates as high as *800 Mc* has been demonstrated. One-hundred and fifty bits have been stored on a single coaxial delay line. The simplicity of the regenerating circuitry in conjunction with etched-wire delay lines makes large arrays of these delay lines feasible. Any line in the array may be selected for input/output purposes without disturbing information stored in the other lines. Gain, pulse shaping, and re-clocking are all provided with the use of only one tunnel diode per line.

The necessary drive current is small (*10* to *20 ma*) and the sense signal is large (*2* to *3 ma*). Such favorable terminal conditions facilitate simple, fast, peripheral circuits. The serial-in-time nature of the storage makes for further simplification of the peripheral circuits; there is only one sense amplifier for the entire memory. Even at high speeds, two-dimensional word selection may be used.

Basic Memory Cell

The basic memory cell is shown in Figure 1; it consists of one printed electrical delay line, tunnel diode, conventional diode, resistor, and a printed capacitor, printed with the delay line. Each cell may store many bits; for instance, all the bits of a given word. All cells will regenerate continuously stored information independently until addressed by the drive circuitry. Coincidence in voltage pulses between *X* and *Y* will cause the conventional diode to conduct. It is through this diode that information passes in and out of the cell. A typical pulse pattern, along with the bit-rate clock is shown in Figure 2. The bit-rate clock serves to synchronize all stored information on all lines.

Information is represented by two voltage levels. A change in voltage level always occurs in phase with an appropriate zero crossing of the clock. To accomplish this relationship, the round-trip line delay is always an integral multiple of a clock period plus one-half of a clock period. Information is stored in a pulse train introduced at the tunnel diode. These pulses travel down the length of the delay line to the termination, a low impedance relative to the cable, where they are inverted by being reflected. The entire pulse train then traverses the line toward the tunnel diode. At the tunnel diode the pulse train is combined with the bit-rate clock signal. The combined signal is sufficient to trigger the tunnel diode circuit into its opposite stable state. The presence of the bit-rate clock serves to re-time the stored pulses, and the amplifying action of the tunnel diode circuit serves to reshape the stored pulses. It can be seen that this process inverts the pulse train every round trip. This property of the cell allows information to be erased and written with monopolar control drives and accessed through a single connecting diode, even with two coordinates of selection. This simplicity of selection and the increased storage capacity offered by non-return-to-zero are the principle advantages over previous systems proposed by *Goto* and *Perry*[1,2].

Typical Operative Model

A fully operative model, which contains all the circuits for a complete system, including circuits for parallel input and output and commutation from serial to parallel operation, has been constructed. This model is representative of a *256*-word, *8* bits-per-word system, but is partially populated. It employs a *115-Mc* clock and has a complete read/write cycle time of *240 nsec*. Except for the details of the timing controls, the block diagram of a typical system, as shown in Figure 4, represents this model.

An independent experiment consisting of the basic cell and the delay line showed that the cell and a coaxial line of type RG9A/U cable could perform at *810 Mc* with a *5-ma, 3-pf,* tunnel diode. A *150*-bit cell was produced using a *160-nsec* line of RG9A/U, a bit-rate frequency of *450 Mc,* and a *5-ma, 5-pf,* tunnel diode. These experiments verified the fact that for best performance, the impedance level and switching speed of the tunnel diode should be compatible with the delay-line characteristics.

This new memory system offers great flexibility of application over a wide spectrum of capacities and speeds. Besides achieving higher information rates than more conventional systems do, this system promises attractive cost factors because of its simplicity.

---

[1] Goto, E., Murata, K., Nakazawa, K., and Nakagawa, K., "Esaki Diode High-Speed Logical Circuits". *IRE Trans.* Electronic Computers, p. 25-29; March, 1960.

[2] Perry, K. E., "A Tunnel Diode Reflex Memory," *MIT Lincoln Lab* Report 52G-0018.

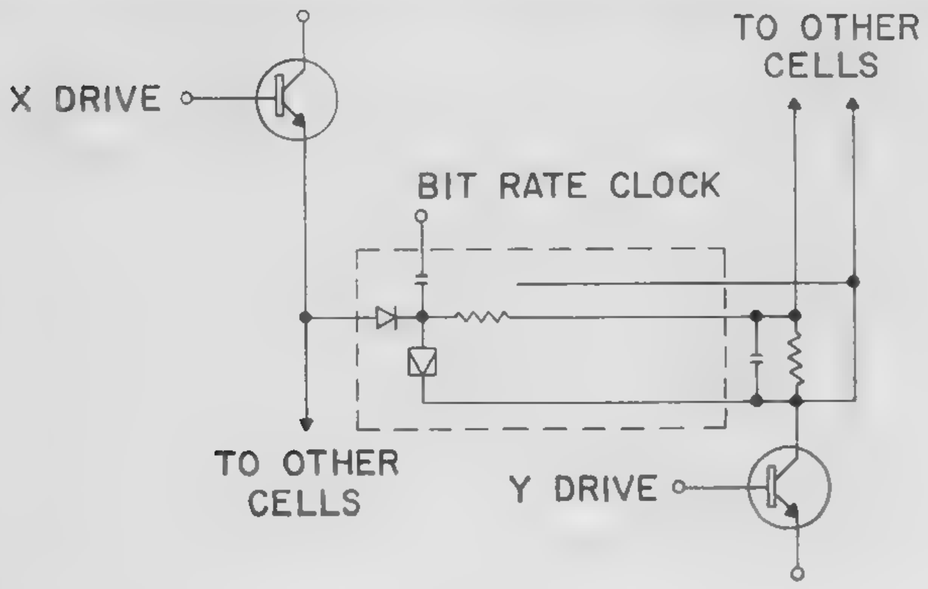


FIGURE 1—**Shielded basic memory cell—in dashed line area.**

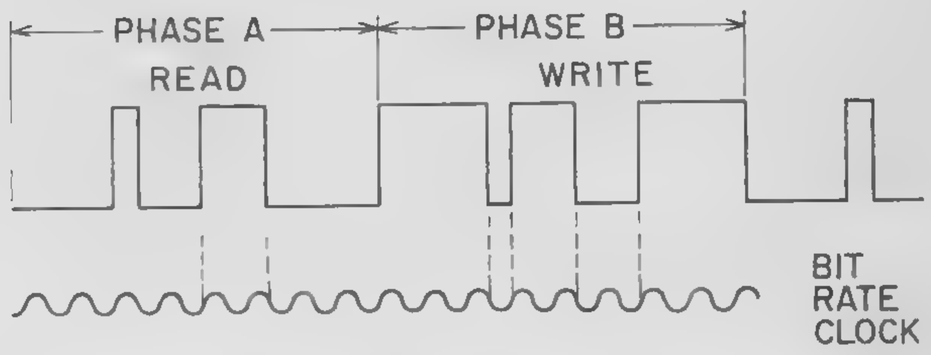


FIGURE 2—**Typical pulse pattern stored on delay line.**

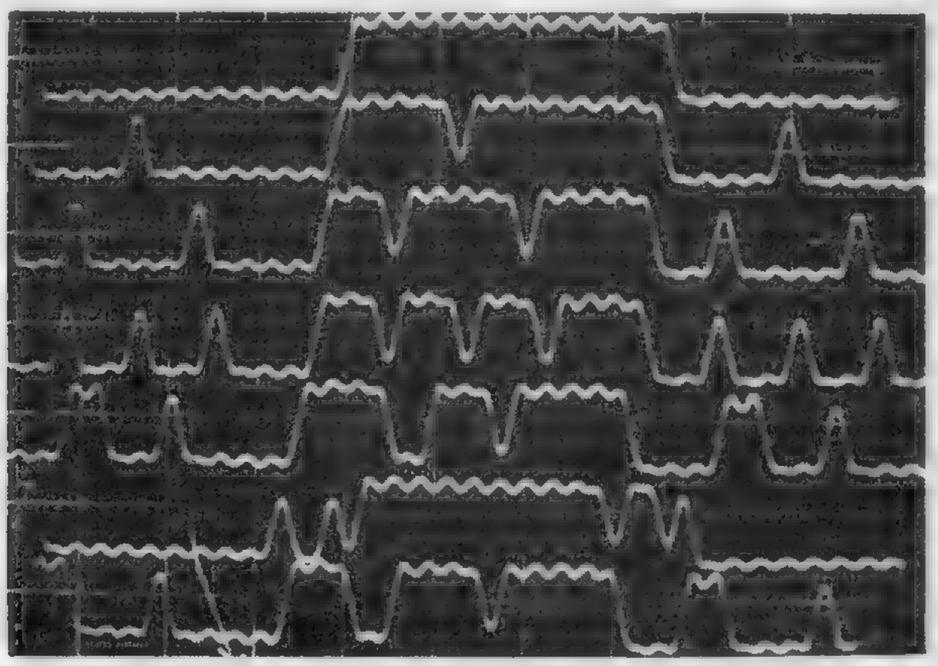


FIGURE 3—**Actual *650-Mc* waveform. Vert: *0.5 v/div;* hor: *5 nsec/div.***

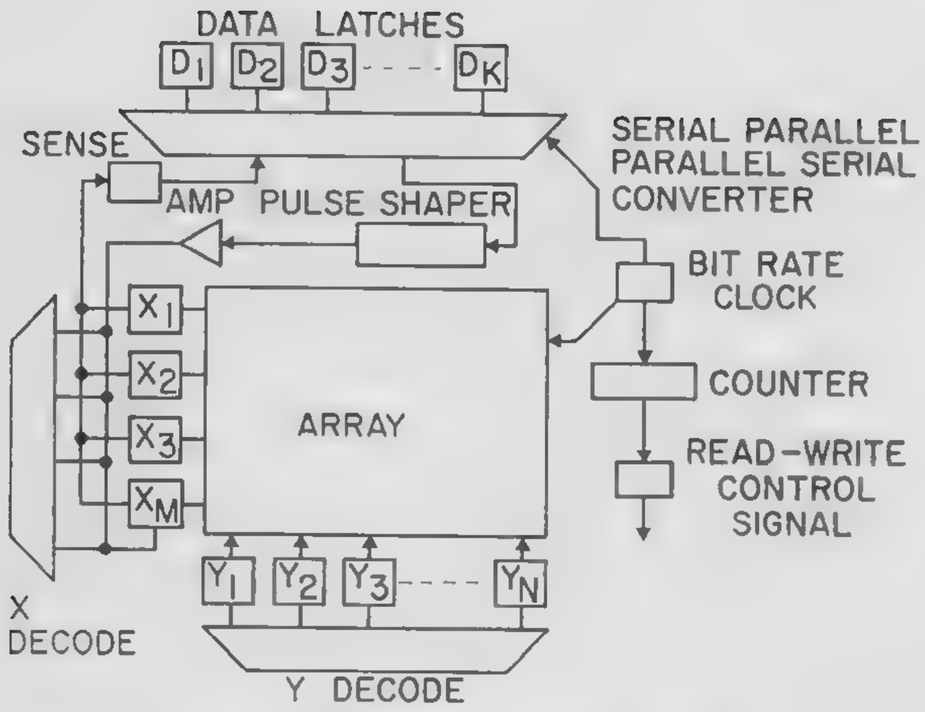


FIGURE 4—**Typical system block diagram.**

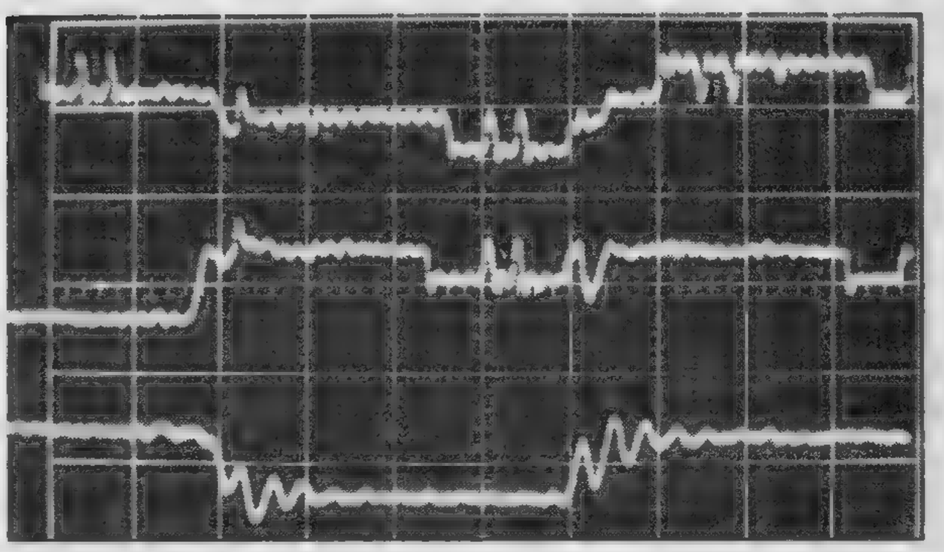


FIGURE 5—**Typical pattern of the *115-Mc*, 8-bit model. Vert: *0.5 v/div;* hor: *50 nsec/div.***

SESSION I: Digital Memories

WAM 1.5: A 64-Bit Cryogenic Addressable Memory Plane

J. P. Beesley, R. H. Blumberg, E. C. Buton, Jr.

Federal Systems Div., IBM Corporation

Kingston, N. Y.

A 64-BIT, CRYOGENIC, addressable memory plane, containing cryogenic memory cells for storage and superconductive switches for memory addressing, has been designed, fabricated, and operated; Figure 1. All *64* cells have functioned satisfactorily during dynamic addressing and interrogating of cells in time sequence, as well as during continuous interrogation of a single cell.

Memory Cell Structure

An enlarged view of the memory cell area is shown in Figure 2. The memory cell consists of right-angle crossings of *X* and *Y* drive lines over a superconductive storage plane. A diagonal sense line crosses the intersection of the *X* and *Y* drive lines.

The memory-addressing switches consist of inline cryotron tree decoders which steer the memory-operating currents to the proper *X* and *Y* drive lines. These decoders are controlled by a memory address register. A single superconductive path exists through each decoder when a memory cell is being selected and interrogated.

Magnetic Field Storage

At the selected cell, coincident currents in the *X* and *Y* drive lines generate a magnetic field which can cause the storage plane to switch from the superconducting to the resistive state, thus allowing a magnetic field to be stored. When information is to be read from memory, currents are applied so that the generated magnetic field adds to the stored magnetic field (if a *1* is stored) and the storage plane is switched; however, if a *0* is stored the generated magnetic field is opposed by the stored magnetic field, and the storage plane is not switched. A voltage pulse is induced on the sense line whenever the storage plane is switched; therefore, the contents of the selected memory cell can be determined by the presence of a voltage pulse on the sense line. Since the selected memory cell always contains a *0* after information has been read from it, reading is destructive.

The Memory Plane

A memory plane is fabricated in a single pump-down of an evaporator system equipped with a mask and source changer. Thirty-two separate evaporations of lead, tin, and silicon monoxide are required to complete a memory plane.

The inline cryotrons in the tree decoder are *0.005"* wide and *0.215"* to *0.290"* long. The memory cell drive lines are *0.010"* wide on *0.040"* centers, while the sense line is *0.005"* wide. The storage density is *625* bits per-square-inch.

Current-Voltage Waveforms

Typical instruction-current and sense-voltage waveforms for a memory cell being interrogated at a *1.6-Mc* rate are shown in Figure 3. The current pulses are *80 ma* in magnitude. The time scale is *0.2 μsec* per large division. The voltage pulse is *0.8 mv* in amplitude and *50 nsec* wide at the base.

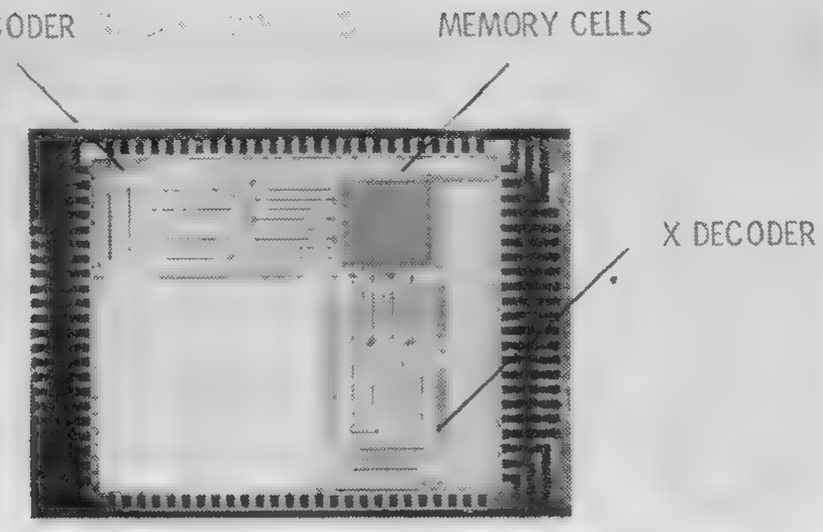


FIGURE 1—**A 64-bit, cryogenic, addressable memory plane.**

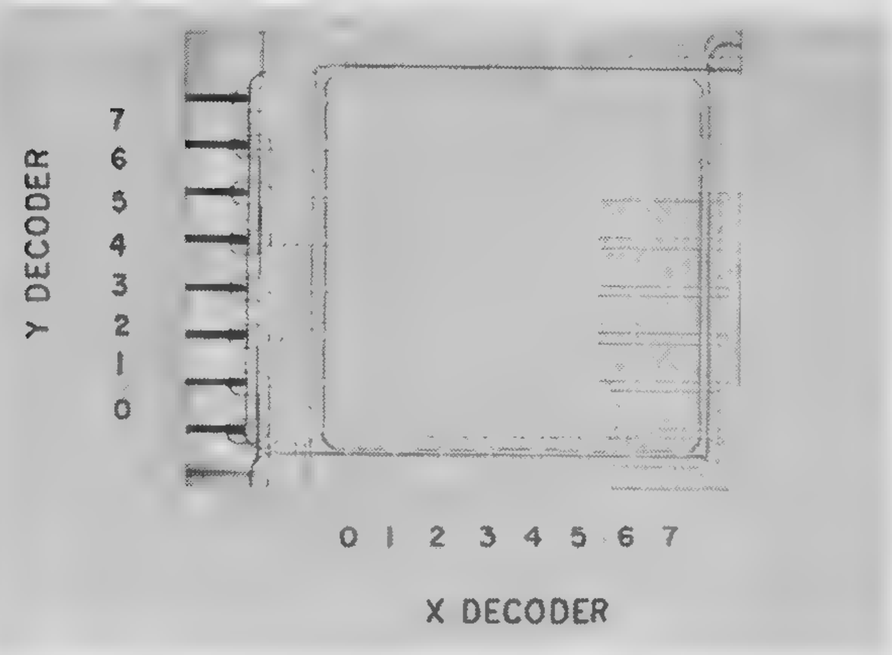


FIGURE 2—**Enlarged view of cryogenic memory cells.**

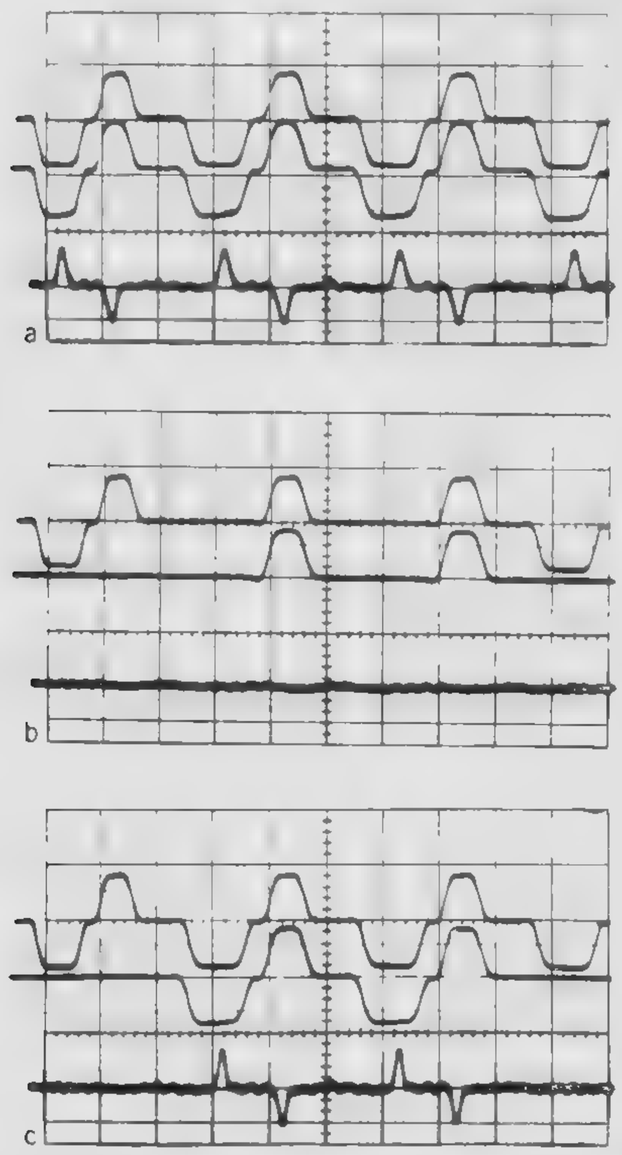


FIGURE 3—**Cryogenic memory cell waveforms: waveforms for continuous read-write *1* cycles are shown in *a*; waveforms for two read cycles between half-select read-write cycles appear in *b*; waveforms for two read-write *1* cycles between half-select read-write *1* cycles are in *c*.**

SESSION II—TUTORIAL: Frequency and Power Limitations of Solid-State Devices

Chairman: E. O. Johnson

RCA, Somerville, N. J.

WAM 2.1: High-Frequency Limitations of Solid-State Devices and Circuits

M. E. Hines

Microwave Associates, Inc.

Burlington, Mass.

The diversity of distinct types of solid-state electronic devices and circuits prohibits a comprehensive discussion of the high frequency limitations of each. This paper will be limited to those simple semiconductor devices which have been found useful at frequencies on the general order of *1000 Mc* and higher.

The talk will cover performance degradations at increasing frequencies for such parameters as: *(1)*—power handling capacity, *(2)*—speed or bandwidth, *(3)*—gain, and *(4)*—conversion efficiency.

Diodes

High-frequency diodes can usually be described by the familiar equivalent circuit of Figure 1. R_s, L_s, and C_p are parasitic circuit elements which affect the performance at high frequencies. The junction elements C_j and G_j are variables which perform the active device function. As a general rule, diodes do not perform as well at high frequencies because the reactance of the junction reduces and becomes comparable with the series resistance, resulting in circuit losses. Figure 1 shows *figures of merit* for various types of diodes. These figures are remarkably similar in form, and each includes a product of R and C in the denominator. To some degree of proportionality these represent a measure of the upper frequency limit of useful operation.

In general, the active region of a diode is confined to a very thin planar zone which includes the *pn* junction. Beyond this zone, the semiconductor material acts as a simple passive conductor, whose resistivity is the major contributor to the series resistance R_s. Obviously, it is desirable to reduce the thickness of the passive semiconductor as far as possible. With expitaxial techniques, it has become possible to use high conductivity material for the major block of semiconductor material. If this block is covered with a thin layer of material appropriately doped for the active diode zone, we can go far in reducing the resistance of the passive parts of a high frequency diode. A diode using such techniques is illustrated in *(a)* of Figure 2.

The next significant factor is that of geometry. The junction size and shape has a profound effect on the high-frequency performance; Figure 3. A simple reduction in junction area will generally improve the Q of a diode. Long narrow junctions are superior to circular junctions of the same area. Junctions in line form, *star* or *snowflake* patterns, or circular ring form offer distinct improvements; Figure 2. Several small junctions or diodes in parallel are superior to a single large junction of the same total area. Appropriate equations are shown in Figure 4. If a substantial total power capacity is required at high frequency, the single round junction is the poorest; the ring, star, or snowflake is better; but a number of small dots is the best geometry if such dot junctions can be made with a diameter as small as the width of a line junction.

Skin effect is a significant mechanism for degradation of device performance at high frequency. Again, small junction areas and line geometries are to be favored for this reason. Applicable equations are shown in Figure 4.

Power dissipation in small junctions is another limiting factor. Because small junctions are necessary, power capacity usually decreases as frequencies rise. It should be noted, however, that the temperature rise of a small junction will be much less than that of a large junction if we maintain *a constant dissipation per-unit junction area;* Figure 5. It may be noted that a small junction *.002-cm* in diameter on the surface of a block of silicon can dissipate continuously a power of approximately *170 mw* through the silicon with a temperature rise of *50°C*. This represents approximately *50 kw/cm²*.

It is evident that great improvements in varactor diode capabilities at high frequencies are possible through the use of optimum epitaxial techniques and junctions of very small dimensions. Substantial power improvements are possible through the use of multiple spot junctions or narrow line junctions in circle, star, or snowflake configurations.

Triode and Transit Time Devices

Development of triode-transistor amplifier devices has shown great advances in the past. Designers have made use of the principles of miniaturization discussed to extend useful operating frequencies as high as *3 Gc*. It would be foolhardy at the present time to suggest that a dead end has been reached for standard triode devices. However, it is evident that future advances along this line will require diligent effort in developing techniques for fabricating complex structures of very minute dimensions.

A likely different attack, however, is to make use of transit-time negative resistance effects in simple multilayer devices using only two terminals. One such approach is the *diffusion delay diode*‡.

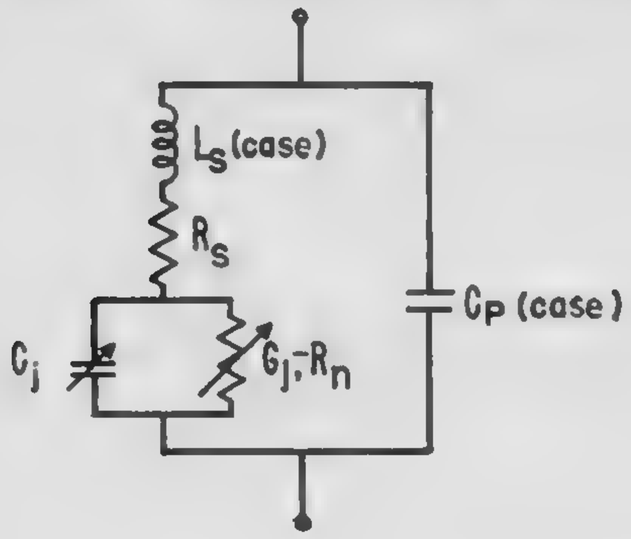
This structure resembles a triode transistor except that no external *ac* drive is applied to the base. With an open-circuited base, negative resistance between emitter and collector can be found at a high frequency such that transit time effects cause an appropriate phase reversal in convection current across the collector-base junction; Figure 6. The simple equation in Figure 6 assumes no thermal dispersion of current waves in the intrinsic region. It is also assumed that the base is thin. Thermal dispersion on the base is accounted for by the magnitude of alpha.

Such approaches show theoretical promise of providing modest power at microwave frequencies by direct oscillation or negative-resistance amplification. Good experimental work is badly needed.

Let us consider a possible silicon varactor of the type shown in Figure 3. We assume an *active* layer *2-microns* thick which is linearly graded in impurity content. Outside of this region we assume high conductivity metal

[Continued on page 118]

‡ Proposed by *Shockley. Weinreich,* formerly at Bell Telephone Laboratories, Inc., and now at University of Michigan, established feasibility of the principle several years ago.



VARACTOR

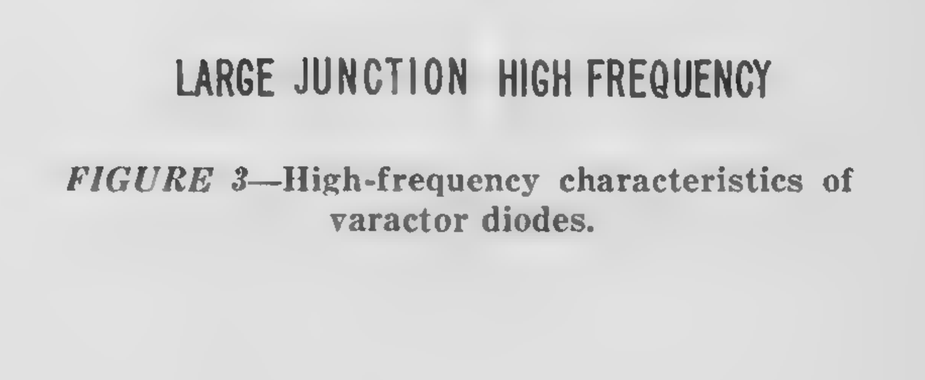
$$f_c' = \frac{1}{2\pi R_s (C_j)_{min}} - \frac{1}{2\pi R_s (C_j)_{max}}$$

$$Q = \frac{1}{2\pi f C_j R_s}$$

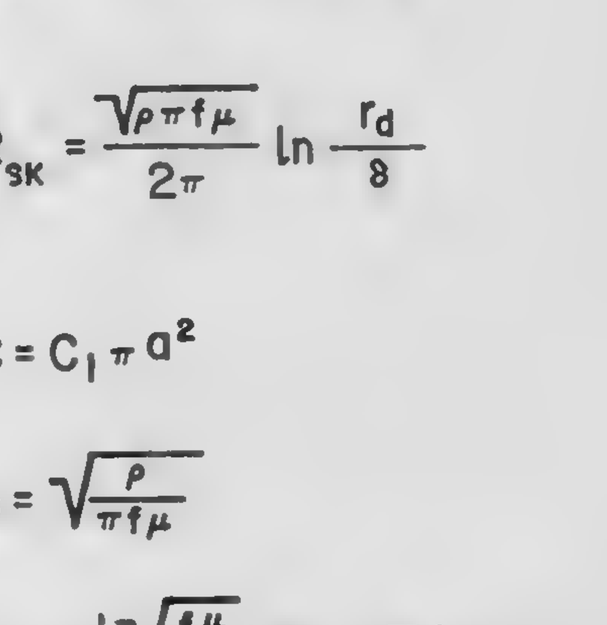
ESAKI :

$$f_{max} = \frac{1}{2\pi C \sqrt{R_S R_N}} \sqrt{1 - \frac{R_S}{R_N}}$$

FIGURE 1—**Equivalent circuit and figures of merit for microwave diodes.**



SMALL JUNCTION HIGH FREQUENCY



LARGE JUNCTION HIGH FREQUENCY

FIGURE 3—**High-frequency characteristics of varactor diodes.**

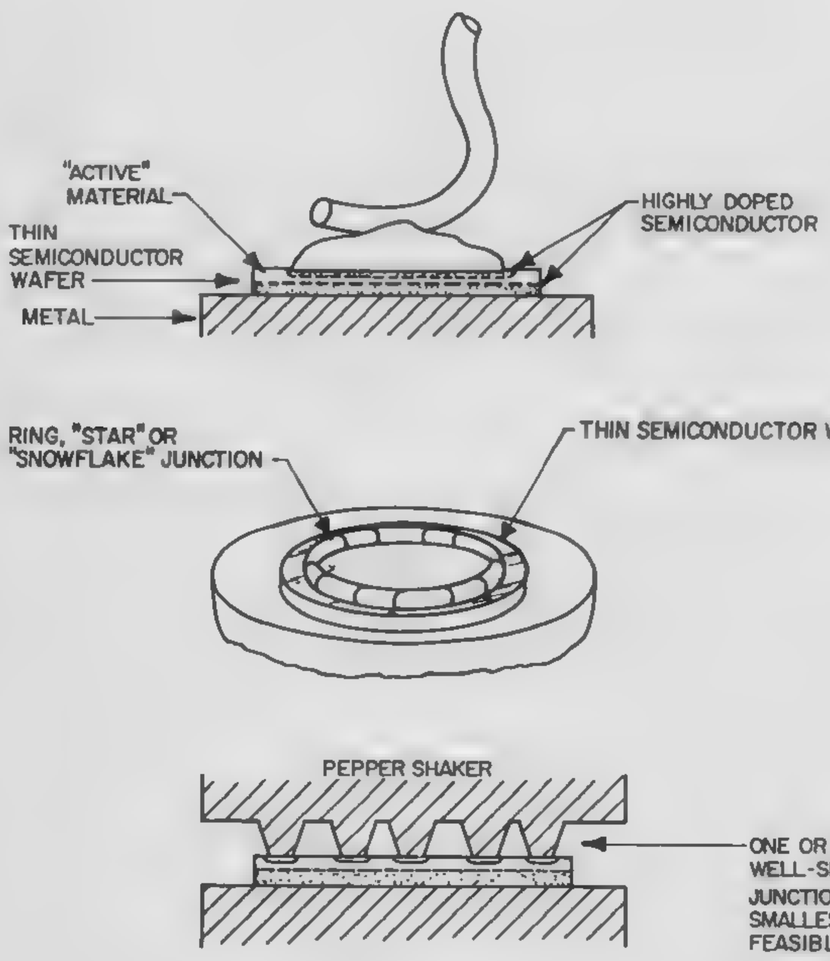


FIGURE 2—**Three types of diode geometry. The first *(at top)* is poorest at high frequency. A line, ring, star, or pepper-shaker configuration should be used to minimize resistance and temperature rise if a single junction of minimum feasible size cannot supply enough power.**

$$R_{SP} \sim \rho \left[\frac{1}{4a} - \frac{1}{2\pi\delta} \right]$$

$$R_{SK} = \frac{\sqrt{\rho \pi f \mu}}{2\pi} \ln \frac{r_d}{\delta}$$

$$C = C_1 \pi a^2$$

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}}$$

$$R_{SK} = \frac{1}{\delta} \sqrt{\frac{f\mu}{\pi}} \left(\sqrt{\rho_1} + \sqrt{\rho_2} \right) \neq f(a)$$

$$Q = \frac{4}{\pi^{2/3} f^{3/2} \mu^{1/2} \left(\rho_1^{1/2} + \rho_2^{1/2} \right) C_1 a^2}$$

FIGURE 4—**Equations for Figure 3. First three apply to small junction, last two to large junction, dominated by skin effect.**

SESSION II—TUTORIAL: Frequency and Power Limitations of Solid-State Devices

WAM 2.2: Are Transistors Approaching Their Maximum Capabilities?

J. M. Goldey and R. M. Ryder

Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

IN THE LAST SEVERAL years transistor performance has improved rapidly. In this paper this performance shall be compared with the ultimate limitations on speed, power output, low power operation and noise.

Although there is no single figure of merit which describes completely transistor capabilities, quantitative measures of performance do exist and some of these are used where appropriate.

Speed

We shall use here the (power-gain)$^{1/2}$ — bandwidth product as a figure of merit, first described by *Pritchard*[1]. This product is equal to the maximum frequency of oscillation of a transistor and is expressed in equation *(1.1)** in terms of the time constants τ_T and τ_c. As shown in equation *(1.2)*, the time τ_T is made up of four terms; the emitter charging time τ_e, the base transit time τ_b, the delay time associated with carrier transport through the collector barrier τ_x, and the time required to charge the collector barrier through the emitter resistance and collector series resistances τ_{rcc}. The latter is negligible for modern epitaxial transistors as well as for alloy transistors and will not be considered further. The other contributions to τ_T are dependent on geometry, materials properties and fundamental physical quantities.

The controlling limitation on τ_T is the delay time associated with carrier transport through the collector barrier. The barrier charging times in τ_T can be made small at high current density. The base transit time can, in principle, also be made vanishingly small. For transistors in which carriers are moving at scattering limited velocity, the collector delay time is determined by the thickness of the collector space charge layer. This barrier thickness cannot be reduced without limit because to do so would cause an increase in the base resistance—collector capacitance time constant τ_c. This time constant, calculated for a transistor of linear geometry with stripe-width s and stripe-spacing $s/2$ is given in equation *(1.3)*. The equation shows that τ_c is dependent upon s, as well as the space charge layer thickness χ_c. *Early*[2] has carried out the appropriate optimizations and derived equation *(1.4)* for f_{max} in terms of s.

To compare present achievements with future possibilities we assume an ability to fabricate structures of 1μ linear dimension. Equation *(1.4)* then gives f_{max} of *60-100 Gc*. Currently, germanium transistors with f_{max} of about *6 Gc* are available.

Other measures of speed are important. Paramount among these is switching time.

Figure 2 shows the pulse response of a silicon epitaxial planar transistor for a circuit gain of *2*. The various components of the switching interval are indicated in the figure. The most significant feature is that the storage time is a very small fraction of the total switching time even though the transistor is heavily saturated. This suggests that now becoming available are transistors which can be used in saturated switching circuits at speeds comparable to those achievable with the same transistor in a nonsaturated circuit.

High Power

The power handling ability of a transistor is determined by circuit efficiency, the power dissipation ability of the transistor and signal frequency. The first factor shall not be considered in this paper.

For a high frequency figure of merit the product of class-*A* power output and bandwidth is used; this may be expressed in the approximate form equation *(2.1)*. Here I_1 is the *rms* collector current and I_0 the *dc* bias. An evident feature is that for power, one should use large area to increase current drive I_0, while also maintaining close emitter-base spacings as described before.

Although high current density is required for high-frequency performance, there is an upper limit on current density and both an upper and lower limit on voltage for high-frequency operation as pointed out by *Early*[3]. These limits, shown in Figure 2 for *pnp* germanium, combine to provide an upper limit on maximum rapidly switchable power density. Maximum voltage is set by collector breakdown, while the minimum voltage is that required to maintain a field of *10,000 v/cm* to achieve carrier scattering-limited velocity. Both decrease with increase of collector body doping as shown. The maximum current density for the condition stated is that which can be carried by a charge equal to that of the doping of the collector body, moving at scattering limited velocity and is therefore an increasing function of doping. These factors combine to give the maximum rapidly-switchable power density which is a slowly-varying function of doping. The maximum calculated value is about 2×10^5 *w/cm*^{2} (for *pnp* Ge), which compares with the highest measured value—8×10^4 *w/cm*^{2}—with which we are familiar. Silicon material and *npn* structures are both slightly more favorable.

It appears that, subject to such maximum limits, it will be possible to make higher power high-frequency transistors by increasing area. It should be noted that such large area transistors, with high current-to-voltage ratios, will encounter the difficulty of operation at impedance levels of less than one ohm. *Early*[4] has derived an expression for the product of power, impedance level, and the square of maximum angular frequency in terms of certain device and material parameters. Equation *(2.2)* relates the performance factors to the charge required to terminate the breakdown field, the carrier scattering limited velocity and the dielectric coefficient. (The constant K is of order 10^{12} and depends on the charge Q_B required to terminate a breakdown field.)

At low frequencies, limitations on power are set by maximum allowable junction temperature, maximum current density or breakdown voltage. In principle, therefore, any amount of power can be handled provided the transistor wafer is suitably large, the current is uniformly distributed, the mounting and heat sinking are sufficient, and the transistor is protected against secondary breakdown. Since these limitations are technological and economic rather than fundamental, we expect that the present limit of several hundred watts will be exceeded as technology advances.

Low Power Operation

For low-power operation, noise and leakage currents set fundamental limits on current at low frequencies, while at high frequencies other factors enter. Important progress has been made in low-power operation at low

---

* Equations appear on page 119.

[1] Pritchard, R. L., "Frequency Response of Grounded-Base and Grounded-Emitter Junction Transistors," *AIEE Winter Meeting;* January 1954.

[2] Early, J. M., "Structure-Determined Gain-Band Product of Junction Triode Transistors," Proc. IRE, p. 1924-1927; December, 1958.

[3] Early, J. M., "Maximum Rapidly-Switchable Power Density in Junction Triodes," IRE Trans. Electron Devices, vol. ED-6. p. 322-325; July, 1959.

[4] Early, J. M., "Speed and Semiconductor Devices," IRE Nat'l. Conv.; March, 1962.

[5] Iwersen, J. E., private communication.

frequencies in silicon transistors in the past few years as a result of the diminution of leakage currents resulting from the use of planar technology. In Figure 3 are shown plots of the collector and base currents for a planar epitaxial silicon transistor of 2N914 geometry as a function of the base-emitter voltage V_{EB}. From this figure it is evident that *dc* current gains of unity are achievable at currents of 10^{-12} amperes, and as high as *10* in the 10^{-9} to 10^{-8} range.

Low-Current High Frequency Performance

The high-frequency performance at low currents is markedly different however, since, for this case, the emitter cutoff dominates the total frequency cutoff, and the former is proportional to the current density through the emitter resistance and capacitance. This is illustrated in Figure 3 where we have indicated the common emitter cutoff frequency f_{Te} for various currents. The basic limitation on high-frequency/low-power operation is, then, one of size—here area rather than stripe spacing being the critical factor when low power operation at high frequency is required.

Some insight into how far transistors may be able to go in the low-power, high-speed field can be gained by calculating the charge required to switch a transistor between two states. Equation *(3.1)* offers the switching time in terms of the circuit gain *G* and the appropriate time constants. The first is the emitter-charging time, the second the base-transit time, the third the collector-delay time and the fourth the collector-charging time through the load resistance. Neglecting the first two terms as before and optimizing the width of the space charge layer x_c to provide minimum t_{sw}, results in equation *(5.2)*[5]. The right hand expression is for silicon.

Assuming an emitter area of *1* square micron, a collector area of *10* square microns, an emitter current density of *100* a/cm^2, and a circuit gain of *two*, one calculates a switching time of approximately 10^{-10} *sec* when switching 10^{-5} *a*. For a voltage swing of *1 v*, this corresponds to a power of 10^{-5} *w* and an energy of 10^{-15} *joules*, implying an impedance level for connecting transmission lines at 10^5 *ohms*.

A comparison with data available today indicates that we currently are *3 orders* of magnitude away from these goals.

Noise

Noise in bipolar transistors consists of shot noise, thermal noise and *1/f* noise. The first two are well understood body effects, while the third arises from a surface mechanism which, even today, is not fully understood. The surface generated *1/f* noise gives rise to the familiar increase in noise figure at lower frequencies. Improvements in fabrication technology are resulting in its gradual elimination as a major noise source.

Further improvement is expected to result, but will do so for bipolar transistors only through improvement in the high-frequency characteristics of transistors.

At higher frequencies, transistor noise figures are already better than receiving tubes up to about *1 Gc*.

Summary and Conclusions

In attempting to answer the question *Are Transistors Approaching Their Maximum Capabilities?*, four key

[Continued on page 119]

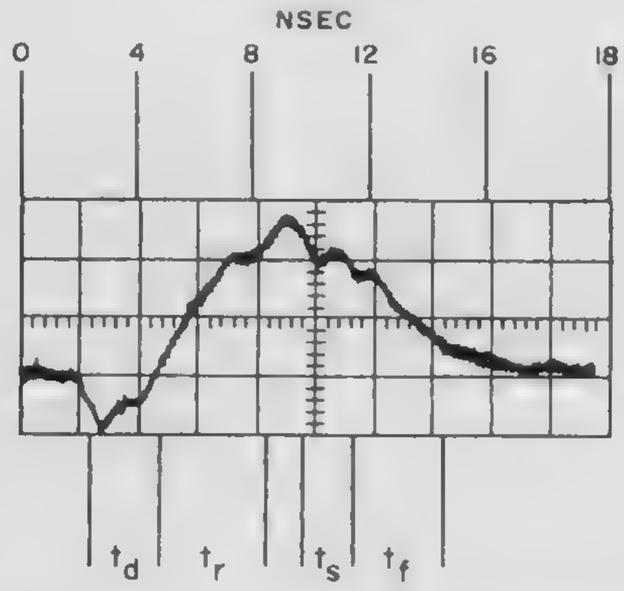
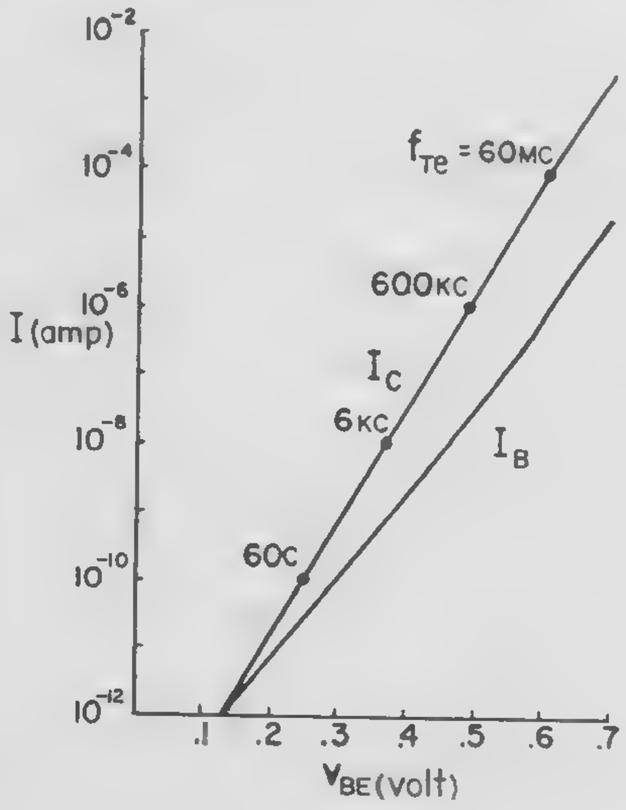


***FIGURE 1*—Pulse response time of a planar epitaxial silicon transistor, showing times of delay, rise, storage, and fall. Note that storage accounts for less than 20% of the total switching time.**



(Left)

***FIGURE 3*—Low-current operation of a planar epitaxial silicon transistor. Cutoff frequency f_{Te} is closely proportional to collector current.**

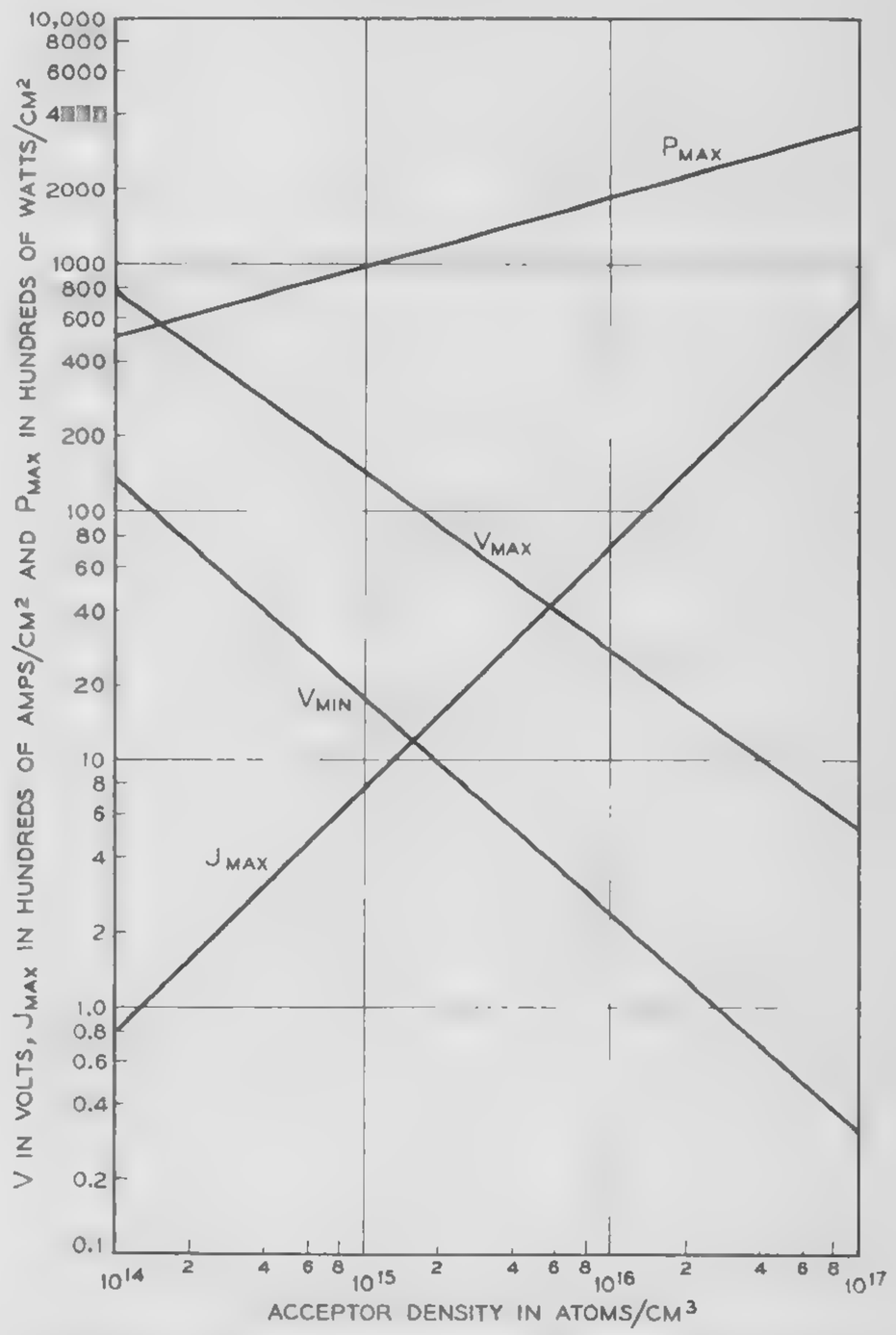


***FIGURE 2—Early's* power density limits for *pnp* Ge at scattering-limited hole velocity of *5 x 10⁶ cm/sec*. Silicon limits and *npn* limits are somewhat more favorable.**

Formal Opening of Conference

Introductory Comments

Chairman of Conference—**F. H. Blecher**, Bell Telephone Laboratories, Inc.

Welcoming Remarks

D. R. Goddard, Provost, University of Pennsylvania

1962 Conference Awards

Chairman, 1962 Conference—**J. J. Suran**, Electronics Lab., General Electric Company

Invited Address

The Role of Network Theory in Solid-State Electronics—Present Accomplishments and Future Challenges

J. H. Mulligan, Jr., Chairman, Electrical Engineering Department, New York University, New York

The Conference gratefully acknowledges assistance received from the Office of Naval Research

Invited Address: The Role of Network Theory in Solid-State Electronics—

Present Accomplishments and Future Challenges

J. H. Mulligan, Jr.

Chairman, Electrical Engineering Department, New York University, New York

THE INVENTION of the transistor and the enormous solid-state technology spawned as a result has not only been affected by, but has also stimulated developments in network theory. The convenience and effectiveness of the transistor and the *Esaki* or tunnel diode as active elements have stimulated a whole new area of network theory, usually referred to as *active networks*. Significant theoretical advances have been made in this area, representative examples of which are the synthesis of *n* port active networks, the synthesis of driving point and transfer functions with one active element, the conditions for optimum sensitivity of transmission functions, with respect to changes in an active element, and normal modes associated with active networks. Circuit designers have drawn on the results of research in both passive and active network theory, plus the development of models of varying degrees of sophistication of transistors and tunnel diodes for guidance in creating practical circuit designs.

Recent advances in methods of manufacturing transistors and diodes, as well as developments in solid-state technology generally, portend an era in which the need is even greater for the extension and application of network theory. Several specific areas can be cited where theoretical advances would assist greatly in the development of new solid-state devices as well as in their optimal utilization.

Distributed Network Theory

Thin film distributed *RC* networks of both uniform and tapered varieties have been investigated theoretically and experimentally as possible filter structures. Particular attention has been given to their use as notch filters or null networks. Recently, progress has been reported on the problem of the systematic synthesis of uniform *RC* networks to achieve prescribed driving point and transfer functions. The preceding efforts and the availability of thin-film transistors suggest the synthesis of distributed active networks. In these, desired transmission functions would be synthesized by combination of uniform or tapered-line sections of appropriate length and impedance level inserted between a suitable number of transistors.

While thin-film transistors are as yet relatively low-frequency devices, existing high-frequency wafers can be combined with strip line sections to form high-frequency active transmission systems. But what of the optimum arrangement of line sections and devices to yield a desired characteristic when the frequency range above *1 Gc* is involved? And to carry the spectrum even higher, a need exists for a rational basis for the synthesis of filter elements for use in millimeter-wave transmission systems. The use of phase correcting *Fresnel*-zone plates in the *100* to *300-Gc* range has been described in the literature, but it appears that the utilization of solid-state materials is yet to be reported.

Statistical Network Theory

Solid-state fabrication techniques have already been developed to the point where a large number of transistor or diode wafers can be produced simultaneously in an extremely small volume. When one has minute active elements available at the same (or lower) cost as passive components, the question immediately arises as to the optimum strategy to use in synthesizing a given transmission function. Attention to the problems of network synthesis on a statistical basis is urgently needed. A systematic investigation of the extensive use of multiple feedback paths, as well as redundant elements, would be valuable in extending important results already attained in these areas.

A more basic objective, however, is the development of techniques for network synthesis on a statistical basis. That is, given active and passive elements with characteristics expressed in terms of probability distributions, how does one combine these to achieve a time, frequency, or phase response within certain confidence limits? Related to this problem is another which is of importance to designers of integrated circuits, namely, the synthesis of prescribed transmission characteristics with elements whose values are constrained to certain ranges because of limitations in fabrication processes.

Guidelines implied by developments in statistical network theory would find immediate practical application in two respects. The effect of unavoidable production tolerances in active and passive circuit elements on network performance could be assessed more readily than at present. Furthermore, inherent difficulties associated with accurate measurement of high frequency device parameters *in situ* would not offer as serious a limitation to the reliable estimation of circuit behavior.

Multivariable Network Theory

The ways in which the various properties of solid-state materials can be used to perform desired functions seems virtually limitless. Within the last few months public announcement has been made of the following representative, but widely diverse, applications: The interaction of charge carriers and ultrasonic waves in a piezoelectric semiconductor (CdS) to achieve ultrasonic amplification; the dependence of microwave acoustic loss on magnetic field strength in yttrium iron garnet to produce microwave delay lines and acoustic transducers with properties controllable by a *dc* current; microwave modulation of light using the electrooptical effect produced in KDP; a pickup means for signals recorded on magnetic tape employing the *Hall* effect to affect carriers produced in a semiconductor crystal by illumination of the crystal; and even an anti-skid warning device employing a sensor based on the temperature dependent relation between transistor collector current and base-to-emitter voltage.

The design of complete functional assemblies utilizing the combined effect of electric and magnetic fields as well as acoustical, optical, and thermal influences is already well in process. To date, however, it appears that design or synthesis problems associated with each such assembly have been considered from a specific, rather than general, point of view. *Network theory*, viewed from a broader standpoint than heretofore, seems to have much to offer to solid-state technology as far as future applications are concerned. The use of power dissipation as a design constraint in conjunction with the properties of electrical networks has already provided the circuit designer with insight valuable for circuit optimization. The time has arrived for the combination of additional appropriate principles of physics with mathematical techniques to develop a *multivariable network theory*, applicable to systems suggested by the examples cited.

Challenges For the Future

All present signs point to the development of increasingly more sophisticated solid-state devices and systems in which optical, acoustical and thermal properties of materials are exploited jointly with the electrical characteristics. If one considers active network theory to be that of optimal utilization of active devices, then network theory today includes a class of problems of appreciably greater breadth than considered heretofore. Even partial solutions in some of the areas mentioned will provide important guidelines in the future development and application of solid-state devices and components.

SESSION III: Logic I

Chairman: R. E. McMahon

MIT Lincoln Laboratory, Lexington, Mass.

WPM 3.1: Microwave Logic Circuits Using Esaki Diodes

Y. Komamiya*

Digital Computer Laboratory, University of Illinois

Urbana, Ill.

HITHERTO, an asynchronous circuit system has usually been a *dc* system. But an asynchronous logic circuit system can be constructed in which a binary code *1* and *0* correspond to an oscillating wave signal and a *dc* level (zero level) signal, respectively. Such a system can be called *Dynamic Asynchronous Logic Circuit System*‡[1,2,3].

The features of the system and the results obtained are:

(1)—Letting a tunnel diode operate in a monostable state (point *P* in Figure 1), the logic circuit can be constructed so that the non-uniformity of the characteristic of tunnel diodes does not have much influence.

(2)—The logic circuits of a microwave *DALC* system consist of the logical sum circuit, the negation circuit (Figure 2) and the high-speed carry circuit, Figure 3, also called the gate circuit or the logical product circuit.

(3)—An oscillation of a tunnel diode has no transient state under the condition ($|\rho| \cong r$, where ρ is the negative resistance of the tunnel diode and r is the lumped-load resistance); that is, the amplitude becomes the steady state from the beginning. Therefore the tunnel diode is operated by the front edge of the wave of the preceding stage oscillation, except in the negation circuit. Thus, the information is transmitted at very high speed. In fact, a tunnel diode is operated less than ¼ period of the oscillation frequency after the front edge of the triggering oscillation frequency in the logical sum and the high-speed carry circuit, etc. In the negation circuit, the switching speed is about two periods of the oscillation frequency. According to the experiment, the switching speed of the logical sum and the high-speed carry circuits is less than about *0.2 nsec* at *300 Mc-400 Mc*. Therefore, the necessary time for the high-speed carry circuit of a *40*-bit binary parallel adder is estimated at less than *0.2 nsec* × *40* = *8 nsec* in *300 Mc*. When the oscillation signal comes from the input terminal *(1)*, i.e., when the *dc* voltage rises through the low pass filter in Figure 3*a*, the tunnel diode D_3 is triggered by the input signal from the input terminal *(2)*. If the signal at terminal *(1)* is a binary *0* (no oscillation) D_3 is not triggered and the input signal from *(2)* is damped; accordingly, it does not appear at the output terminal *(3)*. The switching speed in the negation circuit is about *5-6.5 nsec* in *300 Mc*.

(4)—The limitation of the maximum frequency f_{max} under the foregoing condition is:

$$f_{max} = \frac{1}{4\pi \mid \rho \mid C_d}$$

where C_d is the barrier capacity of a tunnel diode. For example, when $|\rho| = 20\ \Omega$ and $C_d = 10\ pf$,

$$f_{max} \cong 400\ Mc.$$

The equation is obtained from the partial differential equation of the distributed circuit (Figure 4), where Z_0 and l are respectively the characteristic impedance and the length of the line, and where $\rho < 0$ is assumed to be a linear negative resistance.

(5)—The fanouts in the *DALC* system are more than *ten*.

(6)—The negation circuit is unilateral and the high-speed carry circuit is considered similarly as a relay circuit; that is, the terminals *(1)*, *(2)* and *(3)* in Figure 3*a* correspond to the terminals *(1)*, *(2)* and *(3)* in Figure 3*b*, respectively. Therefore, in the DALC system, an ultra-high speed computer can be constructed using only tunnel diodes, a *dc* power source and linear circuit components.

(7)—The phase of the signal wave and the layout of the circuits have no influence at all on the action of the circuits.

(8)—The analysis of the oscillation condition of a tunnel diode shows that there are two values of the regional length of the distributed line ($l_1 < l_2$) when the resistance r and the oscillation frequency of the tunnel diode f are fixed. The amplitude on the length l_2 is larger than that on the length l_1 and the oscillation on the length l_2 is more stable in the presence of fluctuations of r and f.

Tunnel-Diode Figures of Merit Used

The experiment described was performed by using tunnel diodes whose figures of merit are $|\rho| = 20\ \Omega$ and $C_d = 10\ pf$. If tunnel diodes whose figures of merit are better than $|\rho| = 10\ \Omega$ and $C_d = 1\ pf$ are used, $f_{max} > 8000\ Mc$ will be obtained. Accordingly, the switching speed can be made 20 times faster.

---

* On leave, Electromechanical Laboratory of the Japanese Government.

‡ DALC System.

[1] Komamiya, Y., Sugiyama, T., Tajima, H., Ogata, K., "New Logic Circuit System Using Tunnel Diodes on which the Non-uniformity of the Characteristic of Tunnel Diodes does not give much Influence (Dynamic Asynchronous Logic Circuit System)," *Prof. Group Electronic Comp.*, Inst. of Electrical Communication Engineers of Japan; Aug., 1960.

[2] Komamiya, Y., Tajima, H., Sugiyama, T., "Microwave DALC System Using Tunnel Diodes for Ultra High Speed Computer," *PGEC* of IECEJ; Dec., 1961.

[3] Komamiya, Y., "Microwave Logic Circuits Using Tunnel Diodes—Dynamic Asynchronous Logic Circuit System," *Bull. of Electrotechnical Laboratory*, Japanese Government, vol. 26, no. 6, p. 454-472; 1962.

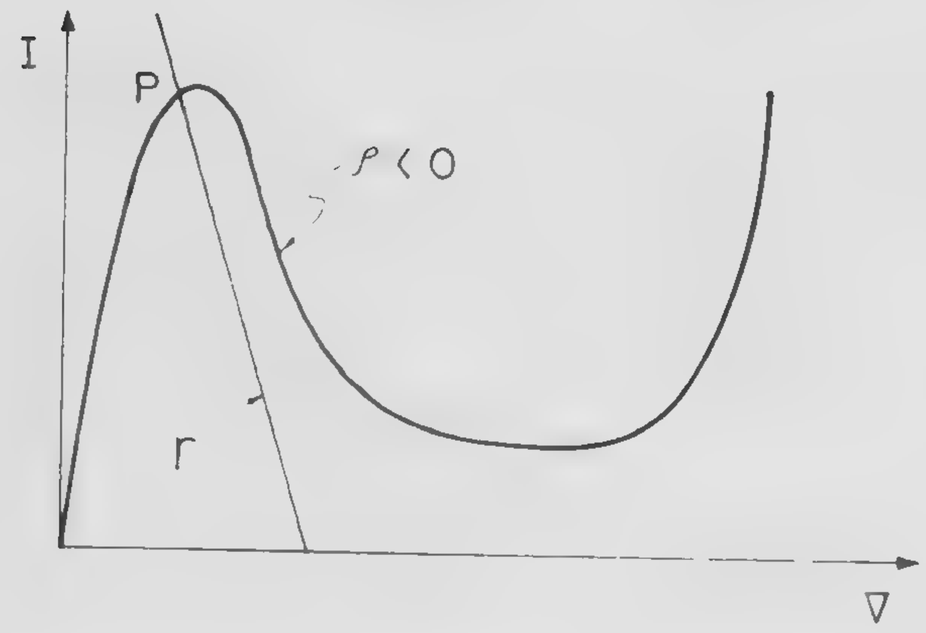


FIGURE 1—The operating point of a tunnel diode and the load resistance line in the *DALC* system.

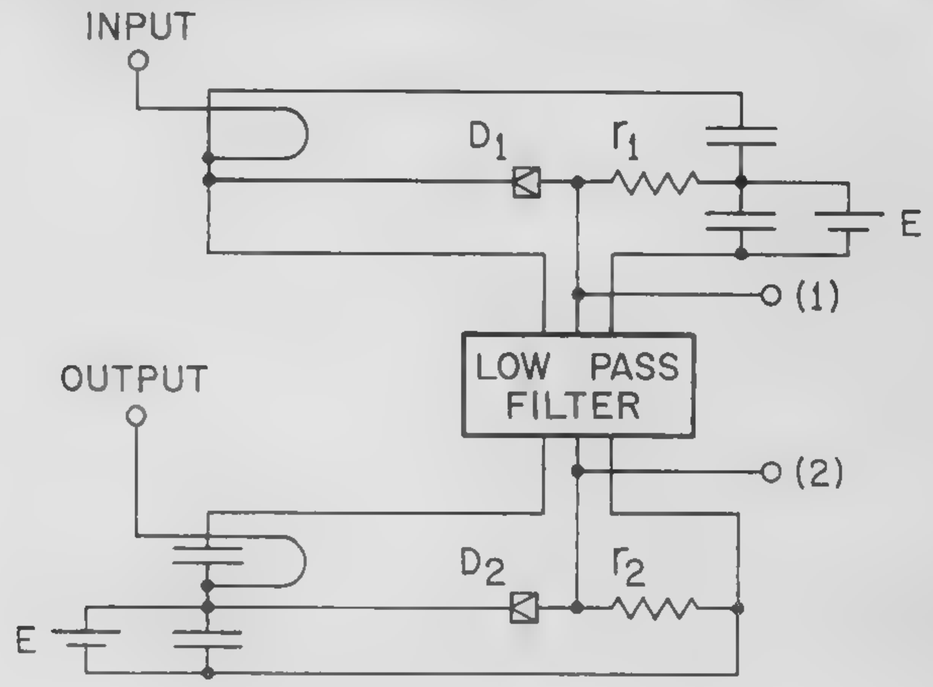
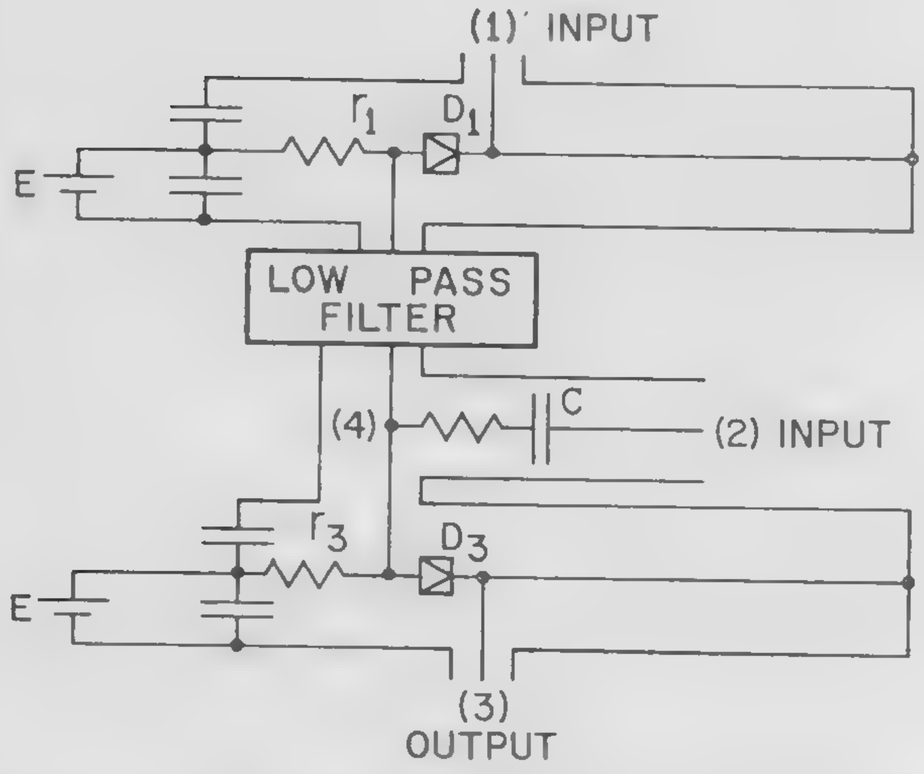


FIGURE 2—The negation circuit.



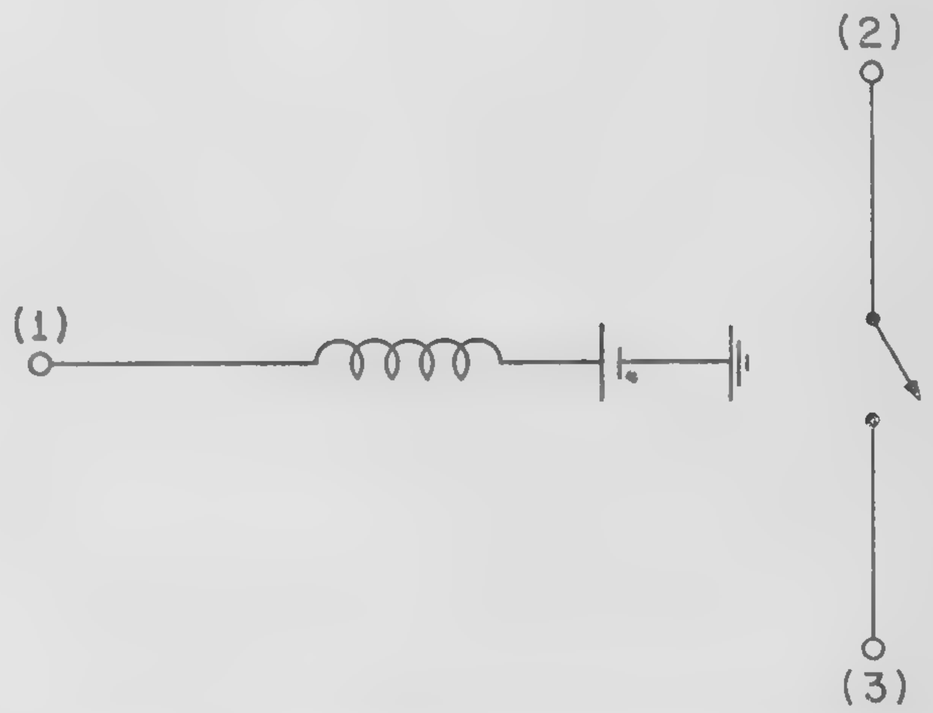


FIGURE 3a and *b*—The high-speed carry circuit is shown at left in *(a)*; in *(b)* at right the relay circuit corresponding to the high-speed carry circuit.

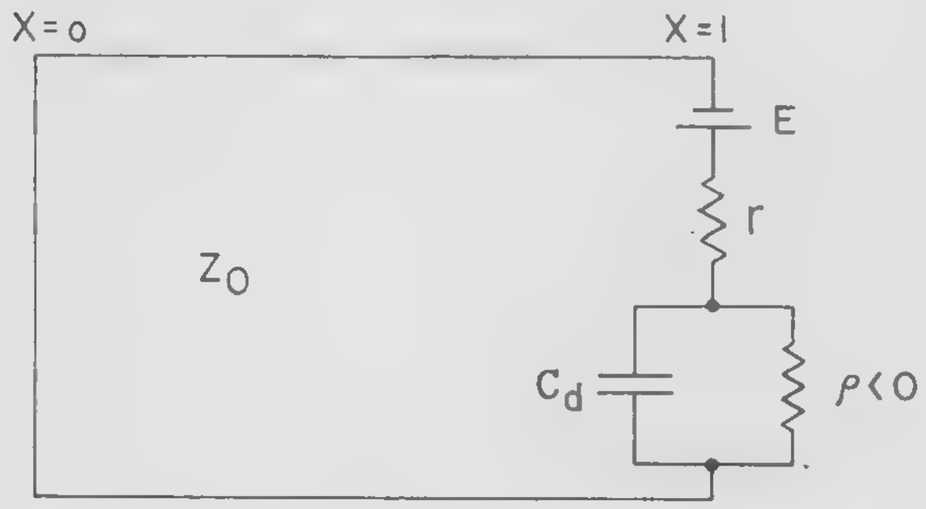


FIGURE 4—The distributed circuit connected to the equivalent circuit of a tunnel diode and the lumped load resistance.

WPM 3.2: The Enhanced Tunnel-Diode Logic Circuit

B. E. Sear

Martin Marietta Corporation

Baltimore, Md.

J. S. Cubert and W. F. Chow

Univac Div., Sperry Rand Corporation

Blue Bell, Pa.

THIS PAPER will describe a unique circuit using a combination of charge-storage diode in a gate and as a diode amplifier, and a tunnel diode to provide high gain without loss of bandwidth. A significant improvement in high speed tunnel diode logic has been achieved.

Simplified Form of Circuit

A simplified form of the enhanced tunnel diode *NOR* circuit is shown in Figure 1. The circuit consists of a tunnel diode *TD* used in the bistable mode, a constant current source $\frac{E_{bb}}{R_B}$ high-speed input diodes d_1 arranged in a diode-gate combination with a charge storage diode d_c, a set clock diode d_s and a reset diode d_r. A small resistor R_1 adjusts the storage diode bias voltage for proper gating action. After *TD* is reset to the low voltage state by a negative pulse, the input voltage to d_1 from previous logic stages either inhibits or enables the flow of forward current through d_c. If all of the inputs are low *(0)*, d_c conducts a current I_f for a period t_f. The resulting stored charge $Q_f = I_f\ t_f$ for several classes of diodes[1] can then be recovered efficiently by applying a fast rise low impedance set clock via d_s to *TD* at the end of t_f. The reverse current, I_R, is limited by the clock voltage and the loop impedance and flows ideally for a time $t_r = Q_f/I_R$. The output current of the stored diode provides sufficient input to cause *TD* to switch to the high voltage state *(1)*. A high input voltage to d_1 *(1)* prevents d_s from conducting. Consequently, with no stored charge, only the capacitive feedthrough current flows in *TD* upon application of the set clock, and *TD* remains in the low voltage state *(0)*.

Gain-Tolerance Characteristics

The logic circuit gain and tolerance characteristics will be discussed with reference to cascaded stages. The storage diode provides a large current gain for a very short duration output pulse; Figure 2*a*. The energy of the narrow pulse is sufficient to cause the tunnel diode to switch beyond the intersection of the load line with the negative resistance portion of the *V-I* characteristics. The bias current then provides current to complete the switching operation. With faster tunnel diodes the storage diode current duration is sufficient to allow constant current switching. Figure 2*b* shows the allowable range of low voltage state bias point variations. $I_{B\ min}$ is determined by the storage diode gain, the required overdrive bias source and peak current variations. $I_{B\ max}$ is determined by the capacitive feedthrough of the storage diode as well as peak current and bias source tolerances. At *1.5-ma* forward current and *4-nsec* forward injection times, storage diode gains of *10* are typical. This results in a fan-out of *5* at ± *5%* peak current tolerance. The fan-in is limited by the clock shunting effects of the input diode capacitance and charge storage. Circuits with five inputs have been used.

Feasibility Model

A feasibility model containing *150* logic circuits is in operation with a logical delay per stage of *2 — 4 nsec*. The model consists of three *32*-bit delay line registers, an arithmetic unit, comparator and control logic. It performs and checks successive serial additions and subtractions for all 2^{32} possible bit patterns. The two basic logic elements used in the model are the enhanced tunnel diode *NOR* circuit and delay elements. Logical rules permit a fan-in of *5* and a fan-out of *5* for a circuit with storage diode gain of *10*. Terminated cables up to *8″* are used between *NOR* circuits.

Acknowledgment

The authors wish to express their appreciation for the efforts of the Univac Advanced Circuits Department and especially to *T. LoCasale* and *J. Stone* for their significant contributions in circuit development and test, and to *W. J. Bartik* and *L. Schwartz* for their advice and assistance in the design of packaging and interconnection of the model.

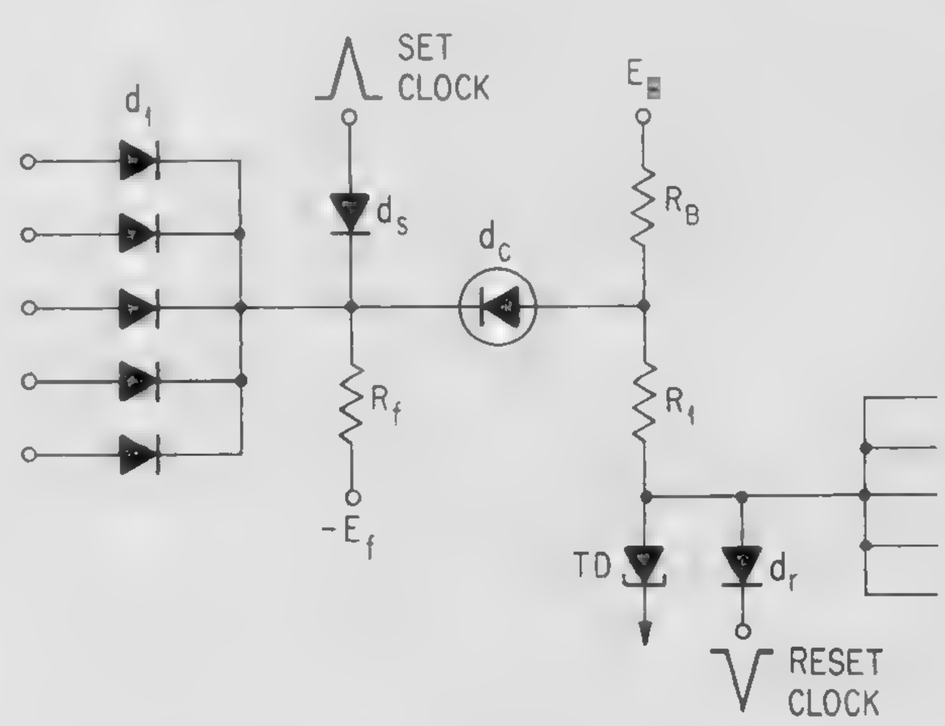


FIGURE 1—Simplified ETD logic *NOR* circuit.

[1] Moll, J. L., Krakauer, S., and Shen, R., "P-N Junction Charge-Storage Diodes," *Proc. IRE*, p. 43-53; Jan., 1962.

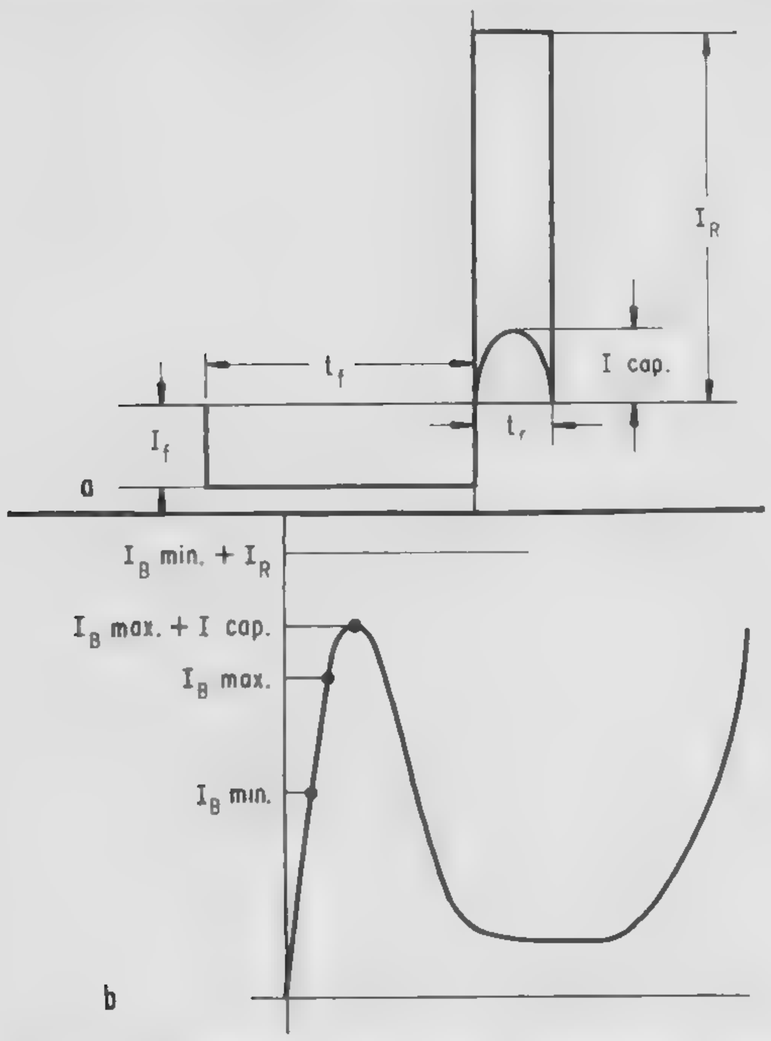


FIGURE 2a—Basic gain and tolerance factors: *a*—storage diode gain and capacitive feedthrough; *b*—tunnel-diode operational tolerances.

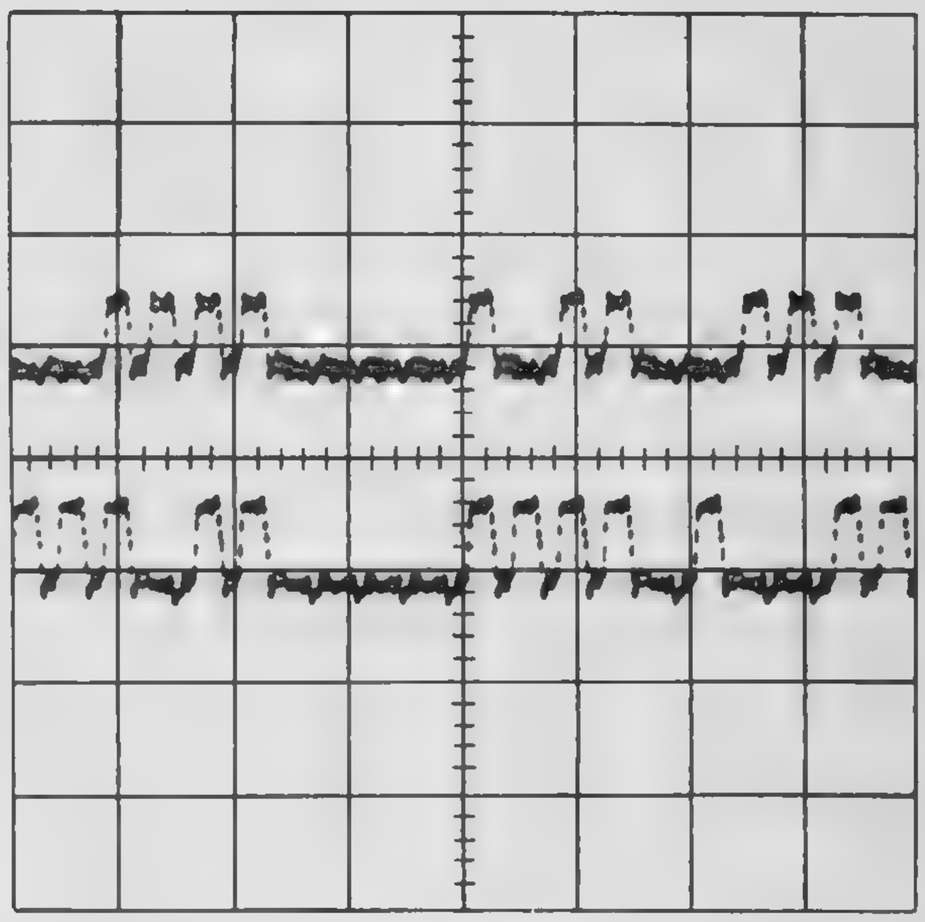


FIGURE 4—Pulses recirculating in a *32*-bit register at a *125-Mc* clock rate, *250-Mc* phase rate; tunnel-diode output waveforms for the *2Φ* system, with an output period of *4.5 nsec* out of *8 nsec*.

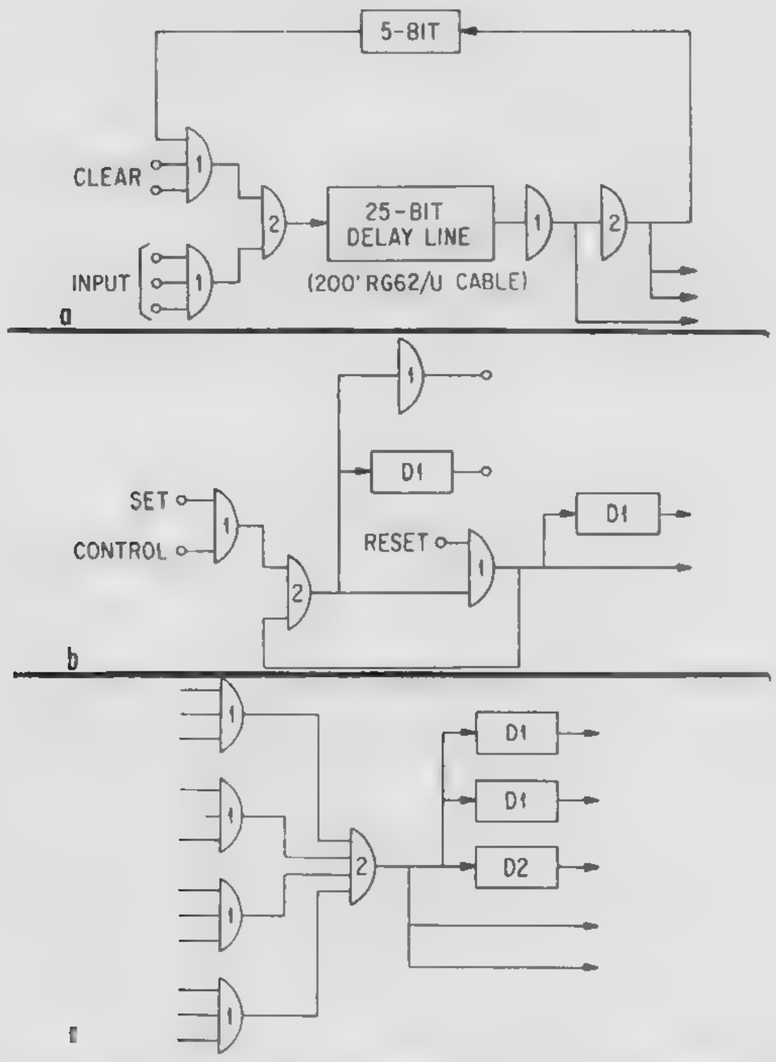


FIGURE 3a (top), *b* (center) and *c* (bottom). The basic TUDAT register logic is shown in *a*. The TUDAT dynamic flip-flop illustrating use of a single-phase delay to obtain a complement output is shown in *b*. The arithmetic logic portion of TUDAT is in *c*.

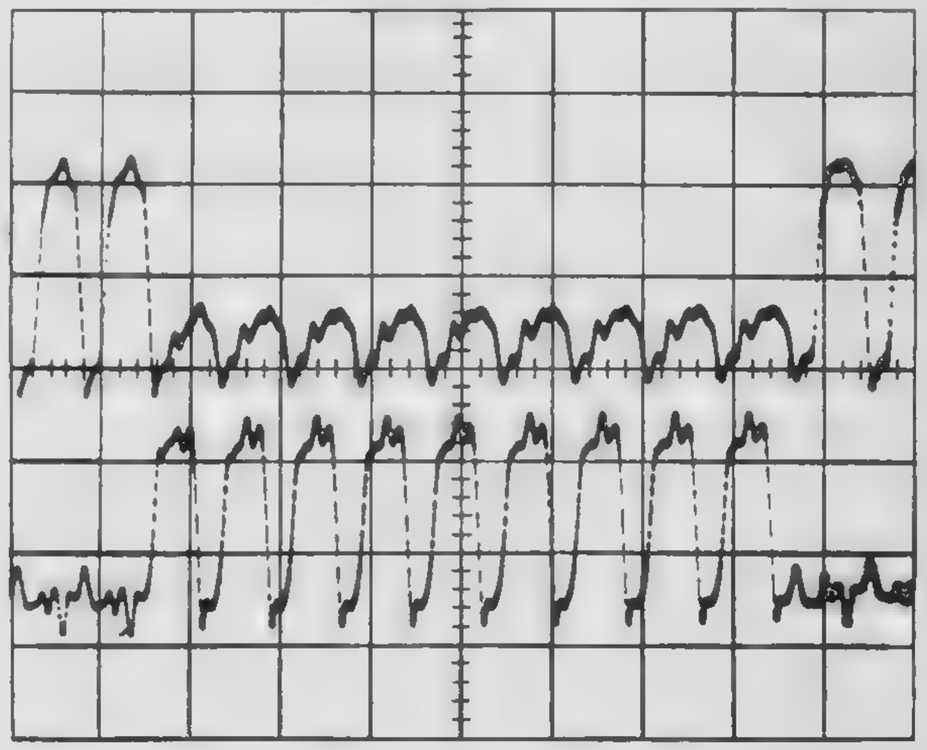


FIGURE 5—A *1-0* transfer between logic circuits at a *500-Mc* phase rate.

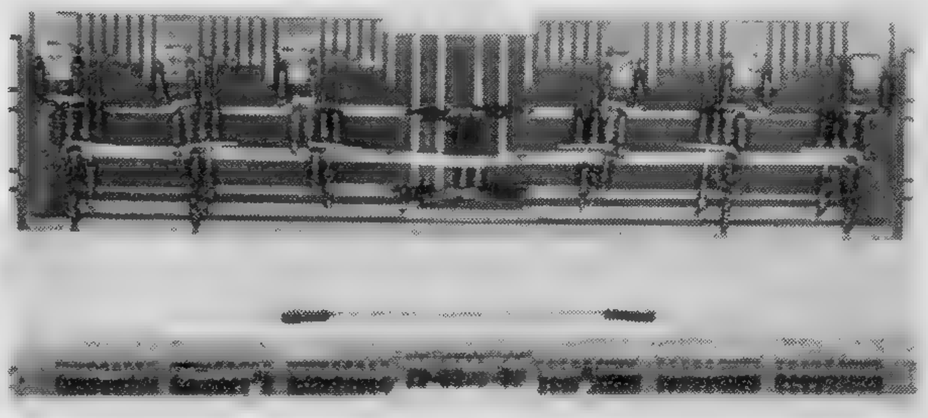


FIGURE 6—Card layout, cables and connectors of TUDAT. Local clocking on each card for six circuits is used to minimize pulse distribution delays and distortion.

SESSION III: Logic I

WPM 3.3: High-Speed Arithmetic Unit Using Tunnel Diodes

J. F. Kruy

Minneapolis-Honeywell Regulator Company

Needham, Mass.

THE MAIN LIMITATIONS of the tunnel diode in digital computer circuits stem from its bilateral nature and from the difficulty of obtaining inversion and good logic gain, while preserving high operating speed. These faults and the rapid increase in transistor switching speeds over the recent years make it unlikely that tunnel diodes will replace transistors in digital systems. Instead, they can successfully complement the transistor to achieve a wider range of circuit operating speeds and economy.

This paper will describe an experimental high speed arithmetic unit which has been built and operated in conjunction with a computer*. The use of tunnel diode circuits in four key areas, namely, tunnel diode memory using non-destructive read-out, memory selection drivers, tunnel diode adder and bidirecctional shift register, achieves high performance and cost reduction in the unit. The unit performs a *48*-bit binary multiplication in an average time of *12 μsec* and a *48*-bit binary divide in *36 μsec*. These operating times are presently limited by the *.75 μsec* central processor clock rate. Propagation delays less than *2.2 nsec* were achieved between logic stages of a *48*-bit binary full adder.

Simplified Form of Arithmetic Unit

The simplified block diagram of the arithmetic unit is shown in Figure 1. A *sub-multiple algorithm* is used in both multiplication and division. The algorithm requires the generation of the multiples of the multiplicand according to a four bit sub-group of the multiplier. These multiples are subsequently added to the partial products previously obtained by the same procedure. One operand and its complement are stored in the non-destructive tunnel diode memory. Proper selection in this memory allows ± *1, 2 4* or *8* times the stored operands to be sent to a tunnel-diode binary full adder. This adder is capable of performing a full *48*-bit binary addition in *175 nsec*. A bidirectional hybrid shift register is used to store the low-order product and multiplier in multiplication and quotient in division.

Now let us consider the particular circuits. The storage element in the auxiliary memory is a tunnel diode operated in the bi-stable mode; Figure 2. Four read-transistors are driven by the tunnel diode with time sharing, i.e., only one of the four transistors draws base current at a time. When not selected, the read-transistors are biased in the cut-off state by a sufficiently negative potential at their emitters. During read time the emitter of the selected transistor is raised to a slightly positive potential. Consequently, the transistor will conduct if a *0 (—.5v)* is stored in the tunnel diode and remains cut off if a *1 (—.05v)* is stored in the tunnel diode. Since the tunnel diode does not change state during a read operation, the read-out is non-destructive. The CLEAR pulse resets all tunnel diodes to the *1* state. To write a *0*, the DIGIT and WRITE terminals must be simultaneously negative.

The diagram in Figure 3 illustrates the organization and *read-shift* operation of the word organized memory. Corresponding to the decoded address, the stored operand or its complement can be shifted left *0, 1, 2* or *3* places simultaneously with the readout, thus generating the ± *1, 2, 4* and *8* submultiples. With this organization, *96* tunnel diodes can provide any one of eight 48 bit words. During addressing, the transistors are operated essentially in the common base mode, resulting in worst case access times under *50 nsec*. The time required to reload the memory after CLEAR pulse is approximately the switching time of the tunnel diode in the circuit, since D and D are simultaneously available during write operation. The virtual elimination of the sense line of low-voltage level in the memory considerably eases layout problems.

Tunnel diodes of high peak current are used in the memory selection drivers, Figure 4, thereby making the required speed and bi-polar addressing voltage levels readily available. The very low output impedance needed is obtained by operating the tunnel diodes in the region of high reverse tunnel current.

The *48-bit* synchronous parallel adder consists of a *48*-bit carry chain, and individual sum stages performing analog threshold logic. To gain speed and circuit simplicity in the sum stage, the negation of the carry signal, rather than the carry, is propagated. Both practical operating voltage margins and high speed are achieved by utilizing some of the logical advantages of synchronous operation. A carry ntwork which performs *2* out of *3* threshold logic (the tunnel diode output is *1* when two or more of the inputs are *1*'s) is shown in Figure 5. The effect of the tunnel-diode output voltage variations is reduced by eliminating the conventional *dc* bias to the tunnel diode. Noise susceptibility is decreased and input currents of tighter tolerance are obtained by connecting the input signals through resistor-diode networks. An alternative circuit which makes use of the three different voltage levels of the backward diode, rectifier diode and tunnel diode has also been operated successfully. The sum is generated by a tunnel diode-transistor hybrid circuit. Due to the signal inversion of this transistor, only the complement of the operand is needed in the adder module, making packaging requirements less stringent. The storage capabilities of tunnel diodes are also utilized to advantage in simplifying timing problems.

The bidirectional shift register stages use hybrid tunnel-diode transistor circuitry; Figure 6. The use of the HOLD pulse eliminates the need for interstage delay and considerably eases the tolerance requirements. The timing between HOLD and SHIFT pulses is not critical. Bidirectionality is obtained by a simple interconnecting network requiring standard logic control voltage levels used also for clearing the register.

The unit has undergone extensive evaluation tests. Discussion of packaging and noise problems and results of diagnostic tests will be included in the talks.

* Honeywell H-800.

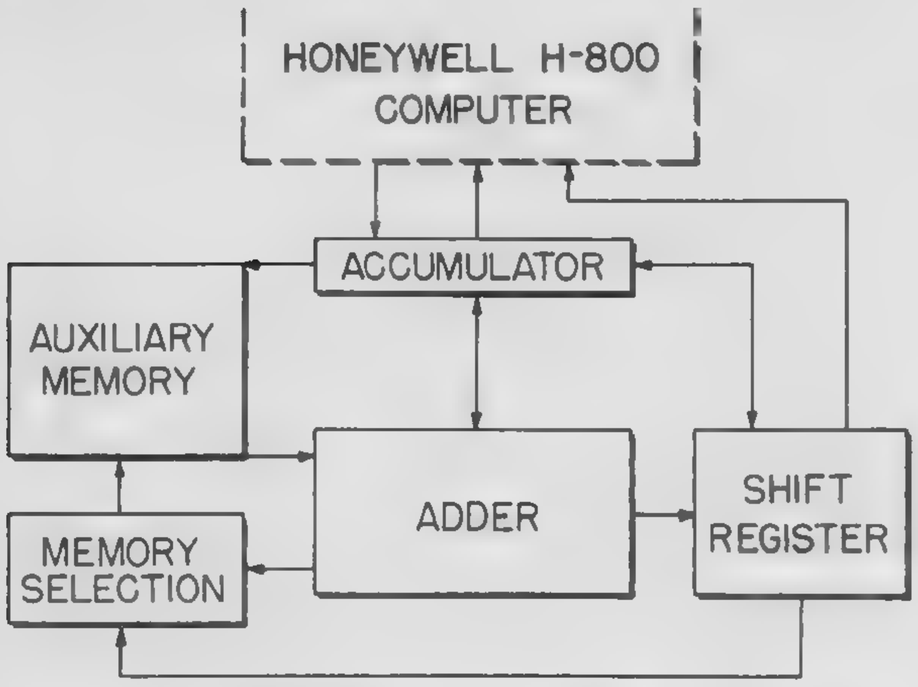


FIGURE 1—**Simplified block diagram of arithmetic unit. Arrows show the flow of information.**

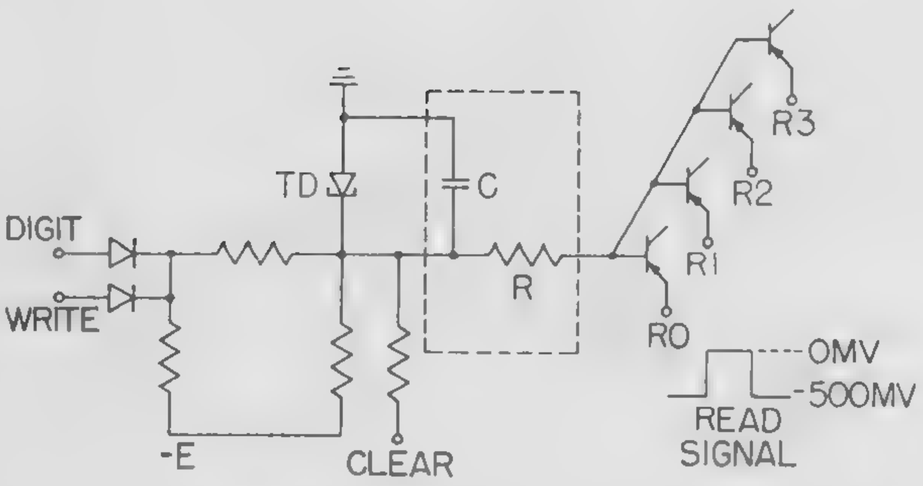


FIGURE 2—**Memory cell and read-transistors. *R-C* network may be omitted in certain cases.**

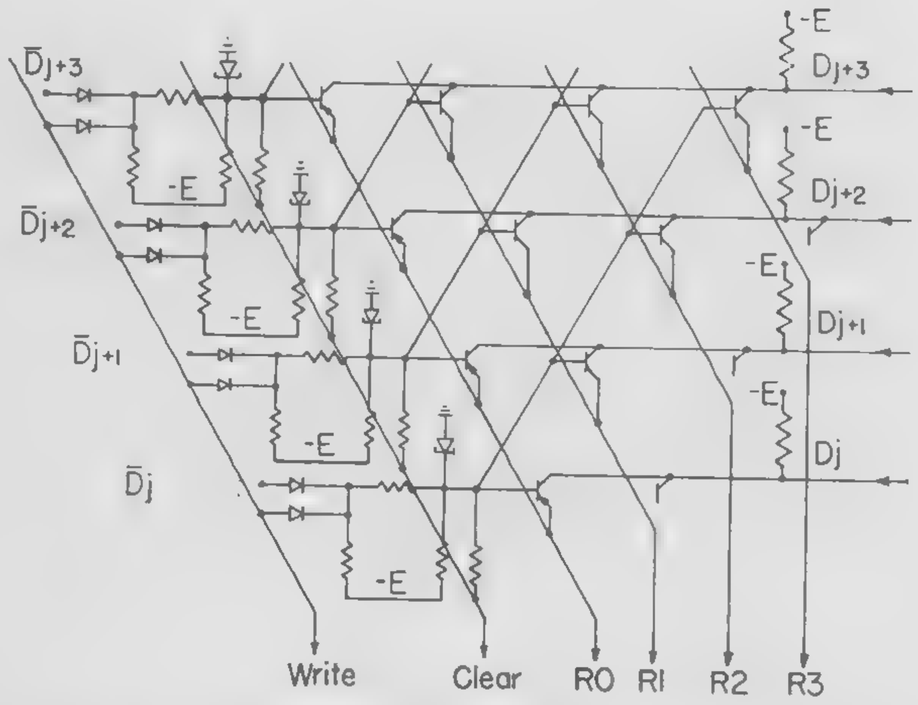


FIGURE 3—**Simplified organization of memory, illustrating the storage and the read-shift operation of digits *j* to *j* + *3*.**

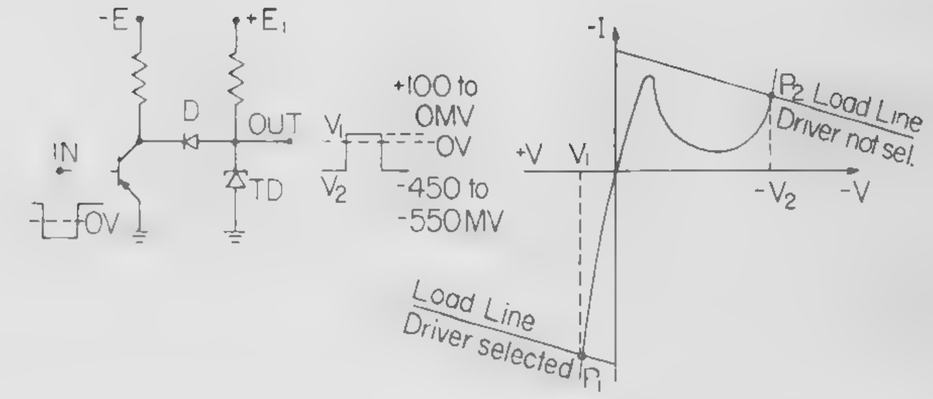


FIGURE 4—**Memory selection driver. P_1 and P_2 are the static bias points of the tunnel diode.**

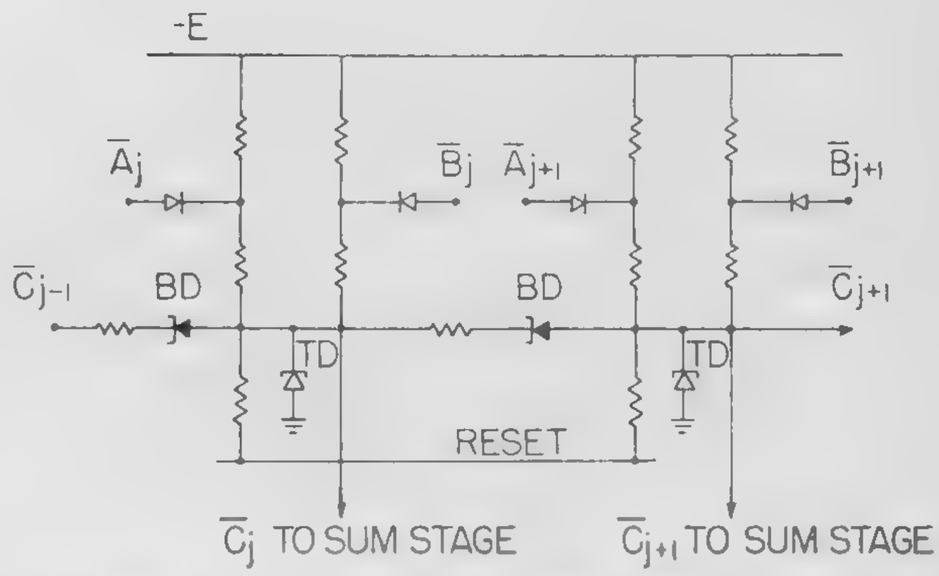


FIGURE 5—**Two bits of the carry chain are shown. The complement of the carry signal is propagated from left to right.**

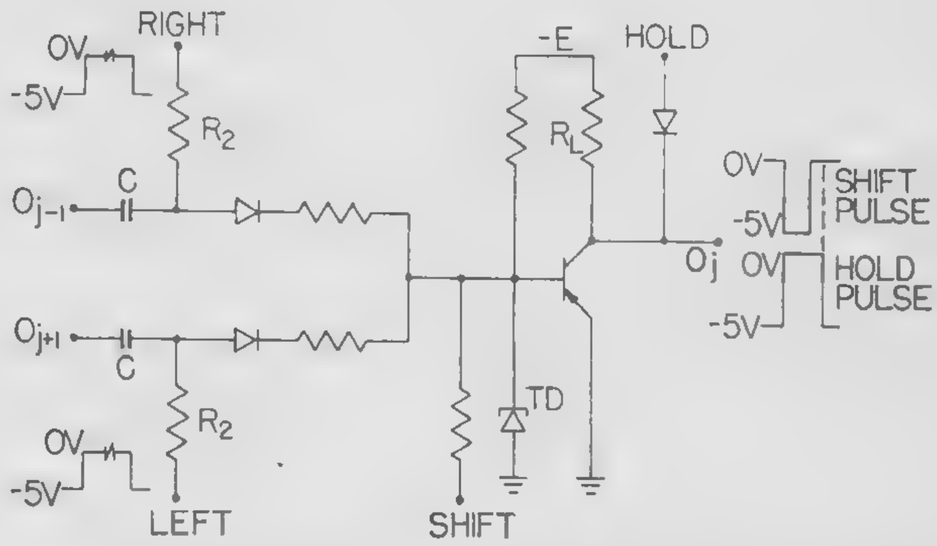


FIGURE 6—**Bidirectional shift register. HOLD pulse eliminates race conditions; clear when both RIGHT and LEFT signals are *−5 v*.**

SESSION III: Logic I

WPM 3.4: Two New Compatible Logic Elements

G. Csanky and R. M. Warner, Jr.

Motorola Semiconductor Products, Inc.

Phoenix, Ariz.

In an ideal logic element, the full excursion of output voltage occurs within a very small range of input voltage. Furthermore, the output excursion should occur at a point near the middle of the input range. This relationship is shown in Figure 1. (Of course, an analogous relationship between output and input current would serve as well.) Such an element is efficient because complete switching occurs with minimum input drive, large margins are allowed for the initial and final values of input drive, and a switching *speedup* effect is realized.

This ideal characteristic can be approximated closely by using a field-effect transistor[1] in combination with a current limiter[2] as shown in Figure 2*a*. The underlying reason for this behavior can be seen in Figure 2*b*. Here the characteristic of the current limiter is plotted as a load line. As a negative voltage is applied at the input, the transistor's characteristic is driven down and the intersection of the two curves moves rapidly from point *(1)* to point *(2)*.

It is, of course, true that a steplike switching transition can be achieved with a negative-resistance device, under conditions where its characteristic makes multiple intersections with the load line during at least a portion of the switching cycle. But this leads inevitably to hysteresis. In the interaction of the field-effect transistor and current limiter, on the other hand, there is no hysteresis from this cause, since there is but a single intersection of the two characteristics at all times.

The circuit in Figure 2*a* is a low-frequency type. Because its voltage gain is high, the gate-drain capacitance of the field-effect transistor plays an important part in reducing frequency response.

This circuit also poses a voltage translation problem. That is, negative voltages are required at the input, while positive voltages are delivered at the output. Therefore, a complementary element must follow, or else a fairly large offset voltage must be provided.

The modified circuit shown in Figure 3 solves the voltage translation problem and also improves frequency response. Consider the frequency response problem first: *a source follower* input stage is added. It provides high input impedance, and its voltage gain of approximately one makes input capacitance a minimum. Additionally, the voltage divider in the source circuit, consisting of R_1 and R_2, provides a low-impedance means for driving the second stage of this element, which mitigates the input capacitance of the second stage.

Next, consider the solution of the voltage translation problem: the source of the second-stage transistor is held above ground by R_3. Therefore, the voltage divider, R_1 R_2, can carry the gate of the second stage negative with respect to its source. Consequently, direct *dc* coupling of these circuits is possible. No voltage translation is necessary.

The element, whose circuit is shown in Figure 3, inverts phase. In Figure 4 is shown a second element which possesses all the virtues of the first but does not invert phase. Figure 5 shows an experimental V_{OUT} versus V_{IN} characteristic for this element.

Because of the nature of the output-versus-input characteristic for either element, the voltage transition at the output is much faster than that at the input. Switching time, τ_{switch}, is a constant percentage of the time for a complete cycle, $1/f$, for sinusoidal drive. Hence, the dimensionless product $f\tau_{switch}$ is constant within the operational frequency range of the logic element. The present modules can accept a sine wave of a few hundred *kc* without appreciable hysteresis or other degradation in the switching characteristic.

Either circuit can be used as a snap-action buffer in conjunction with a diode gate. Alternatively, it is possible to put additional transistors in parallel with the source follower transistor to provide additional inputs for logic, as shown in Figure 6. This arrangement utilizes fully the high input impedance advantage of the field effect transistors.

These elements cannot compete in speed with circuitry employing conventional transistors, although improvements in speed are possible by employing technology already in hand. Still, in applications where speed is not of paramount importance, such as the peripheral equipment in a computer, their other advantages can be fully exploited. Among these advantages is the convenient integration of field effect devices. This is true because the current axis is in the plane of the wafer rather than normal to it. Thus, simple concentric gate patterns place field effect devices in series. Further, no capacitors or inductors are needed in the proposed systems.

Because the field-effect transistors and the current limiter have the same relative temperature dependence of current, these circuits are largely temperature compensated. Further advantages are direct *dc* coupling with no *offset* problem, phase-inversion or no phase-inversion, as desired, a possibility for low power drain, and a steplike characteristic with its attendant advantages.

---

[1] Shockley, W., "A Unipolar 'Field-Effect' Transistor," *Proc. IRE*, p. 1365-1376; Nov. 1952.

[2] Warner, Jr., R. M., et al, "A Semiconductor Current Limiter," *Proc. IRE*, p. 44-56; Jan., 1959.

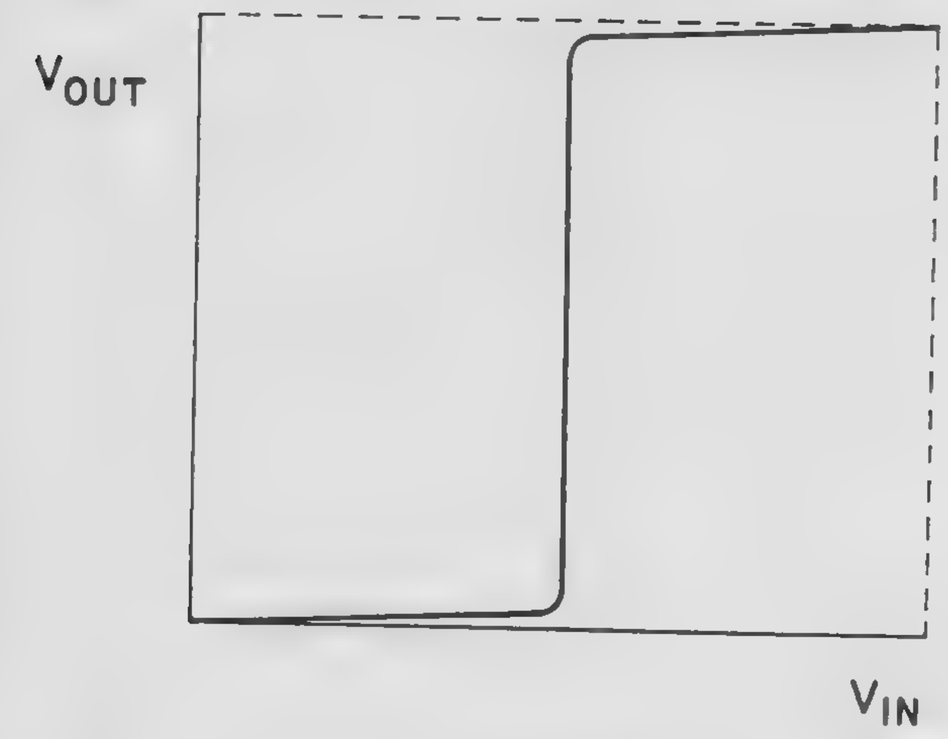


FIGURE 1—Output voltage versus input voltage for an ideal logic element.

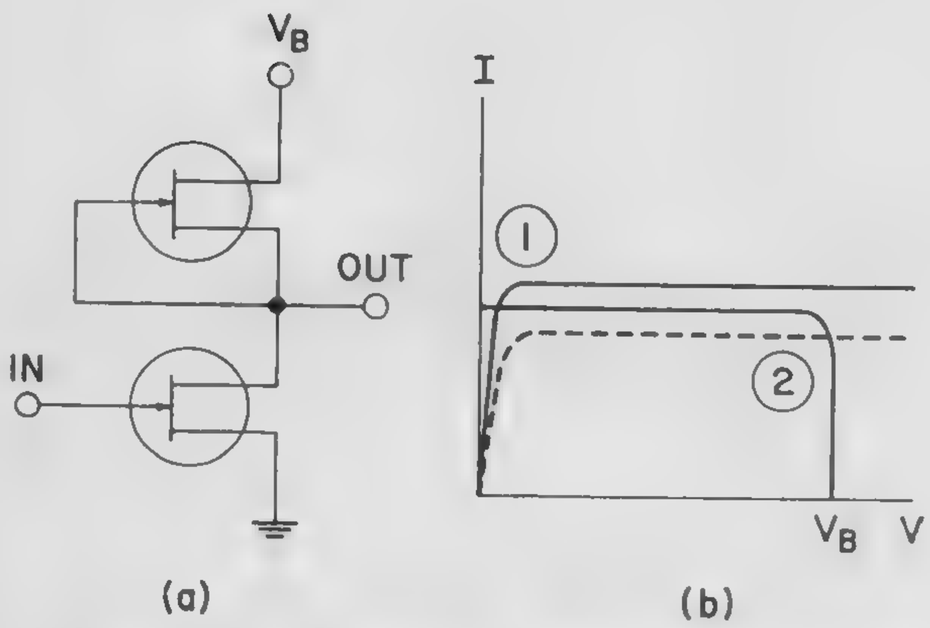


FIGURE 2—The field effect transistor and current limiter configuration yielding steplike output versus input characteristic is shown in *(a)*; interaction of current-voltage characteristics in *(b)*.

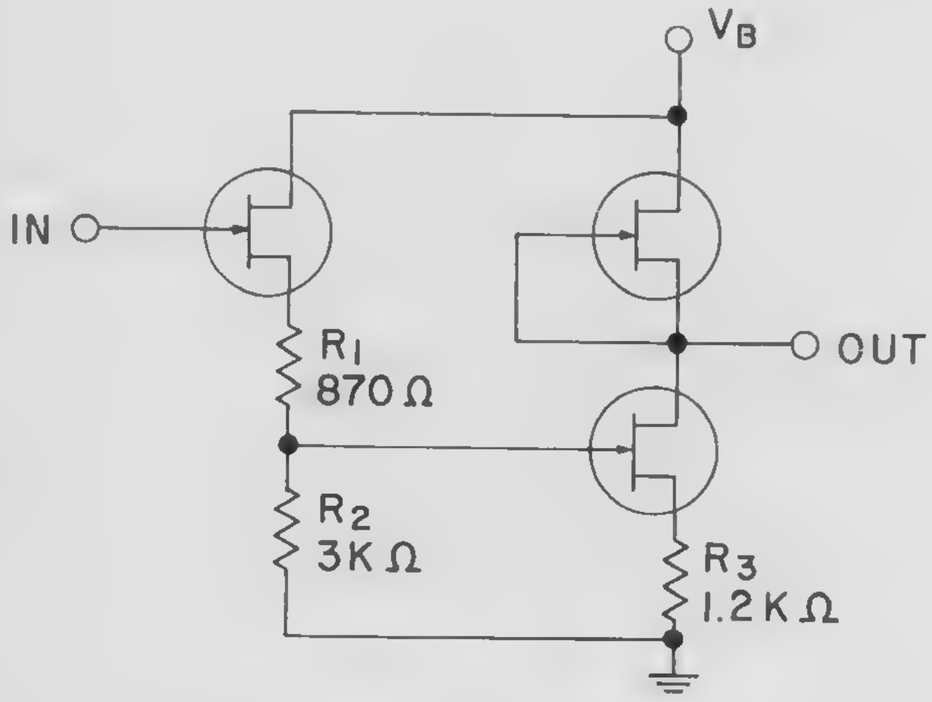


FIGURE 3—Phase-inverting logic element.

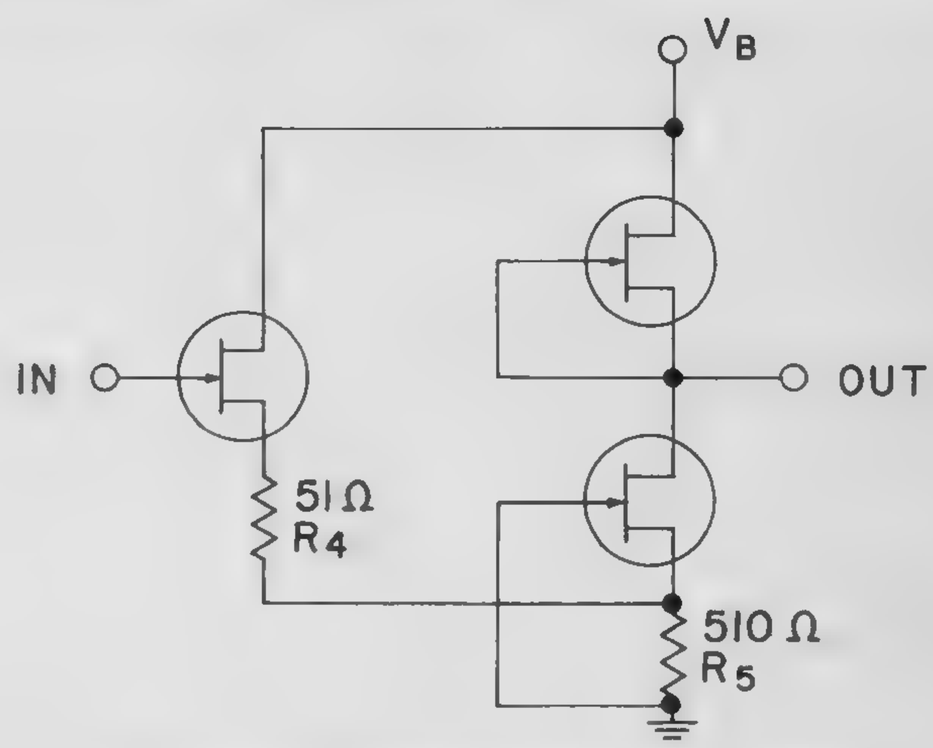


FIGURE 4—Non-phase-inverting logic element.

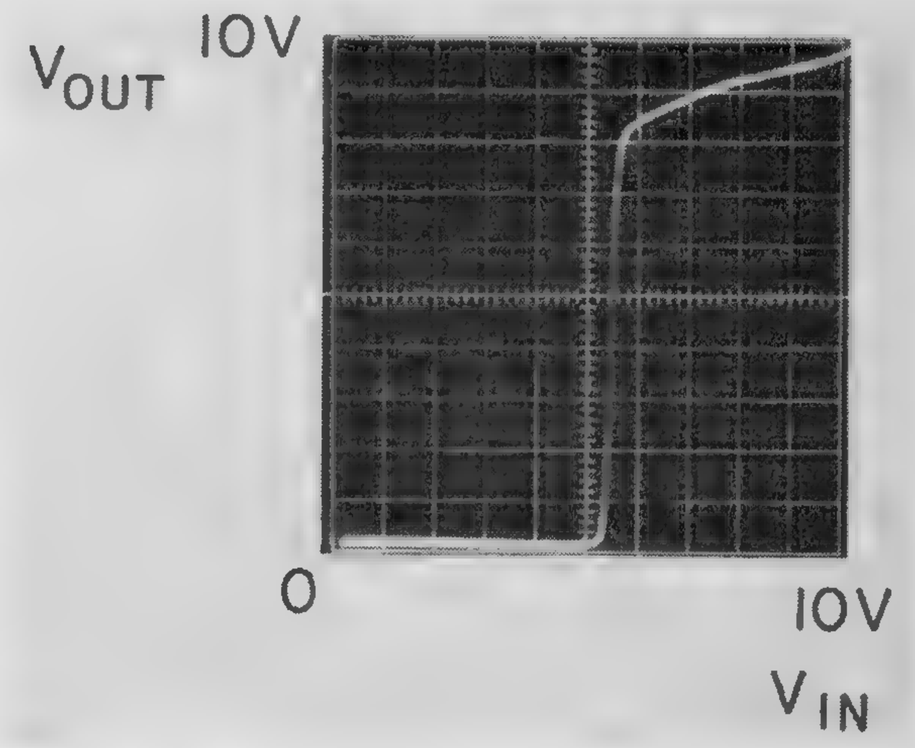


FIGURE 5—Experimental output versus input characteristic for element shown in Figure 4.

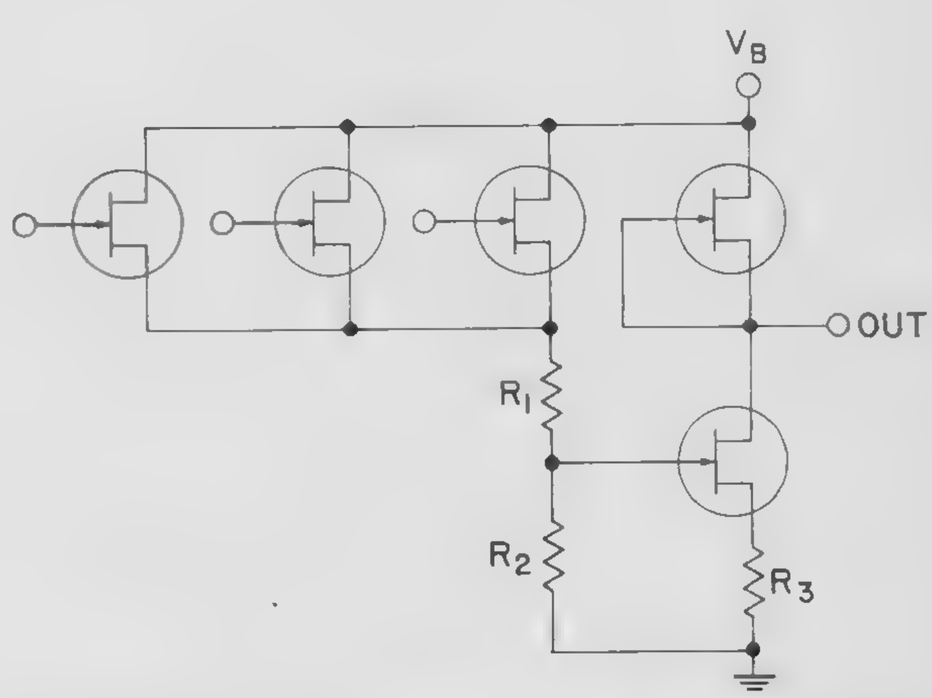


FIGURE 6—NOR circuit employing phase-inverting logic element.

SESSION III: Logic I

WPM 3.5: Nanowatt Logic Using Field-Effect Metal-Oxide Semiconductor Triodes

F. M. Wanlass and C. T. Sah

Fairchild Semiconductor Div., Fairchild Camera-Instrument Corporation

Palo Alto, Calif.

Complementary N and P-type field-effect *metal-oxide-semiconductor-triodes* have been fabricated from silicon by a planar diffusion process. These devices have gate input resistances of $\sim 10^{15}$ *ohms* and input capacitances of < 10 *pf*. The cross sections of both types of these triodes, which will be referred to as *N* and *P* elements, are shown in Figure 1. If a *N* element is biased with a positive drain source voltage, as shown in Figure 2*a*, and if its gate is tied to its source, then drain source current I_{DS} will be of the order of that flowing in a reverse-biased silicon diode. But I_{DS} can be increased considerably by making the gate source voltage $V_{GS} \geq +10$ *v*. Typically, I_{DS} can be switched from $< 10^{-9}$ *a* to > 10 *ma* by a change of *20 v* in V_{GS}. The *P* element is described the same way as the *N* element except that all voltages need to be reversed. Thus, if a *P* element is connected as in Figure 2*b*, I_{DS} can become very large if the gate is biased negative, with respect to the source. Figure 3 shows characteristic I_{DS} versus V_{SD} curves for both types of field-effect triodes when connected as in Figure 2.

Consider the inverter circuit of Figure 4 as an example of low power logic that uses only *N* and *P* elements without the need for resistors or any other components. Here the *N* element, acting as an active load for the *P* element, is turned on when the *P* element is off, and off when the *P* element is on. This combination will only dissipate appreciable power during switching. The leakage current is so low for a field-effect triode in the off-state that 10^7 circuits, like that of Figure 4, would use less than one watt of standby power.

Even though the standby power of the inverter of Figure 4 is extremely low, it can still switch very fast. In an effort to measure the signal propagation delay of the inverter, the three-stage ring oscillator of Figure 5 was set up. A plot of the output of one of the stages is in Figure 6; it will be seen that the propagation delay is less than *100 nsec*. Part of the observed delay is due to oscilloscope input capacitance across the output.

Other useful logic circuits using only complementary *N* and *P* elements can be readily designed. For example, Figure 7 shows a *NOR* circuit and Figure 8 a set-reset flip-flop. In these circuits appreciable energy is dissipated only at a rate proportional to the information processing rate.

The output of a logic circuit composed of complementary field-effect triodes can fan out to a large number of other inputs by direct coupling; the only consideration in limiting the number is switching speed. It should be possible to drive approximately *50* inputs from one output and have less than a *1* μ*sec* signal propagation delay.

Since these field-effect triodes are switched in the voltage mode and no resistor tolerances enter in the *dc* switching considerations, high temperature differentials between different parts of *N* and *P* element circuitry can be tolerated well. This means that a volume of *N* and *P* elements dissipating power can be cooled efficiently using a small amount of heat exchange area. Thus, because *(1)* both standby power density will be extremely low and *(2)* switching power density can be high, it should be possible to construct field-effect triode logic circuitry with a very high packing density.

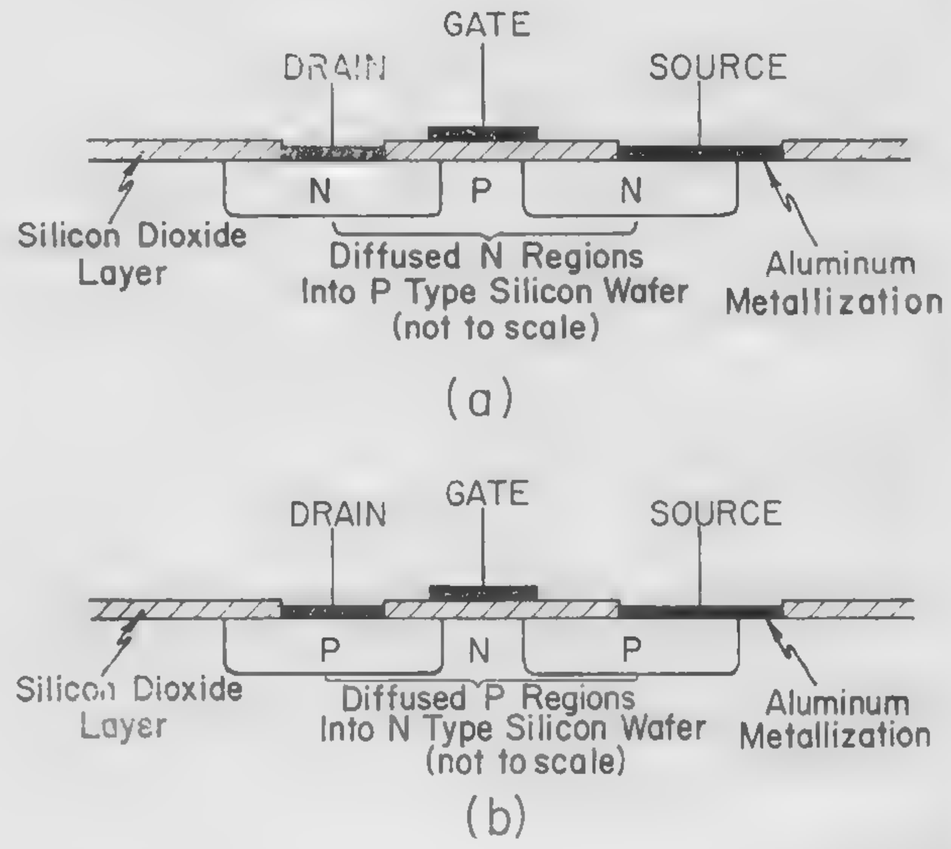


***FIGURE 1*—Cross sections of metal-oxide-semiconductor-triodes: *(a)* the *N* type element; *(b)* the *P* type element.**

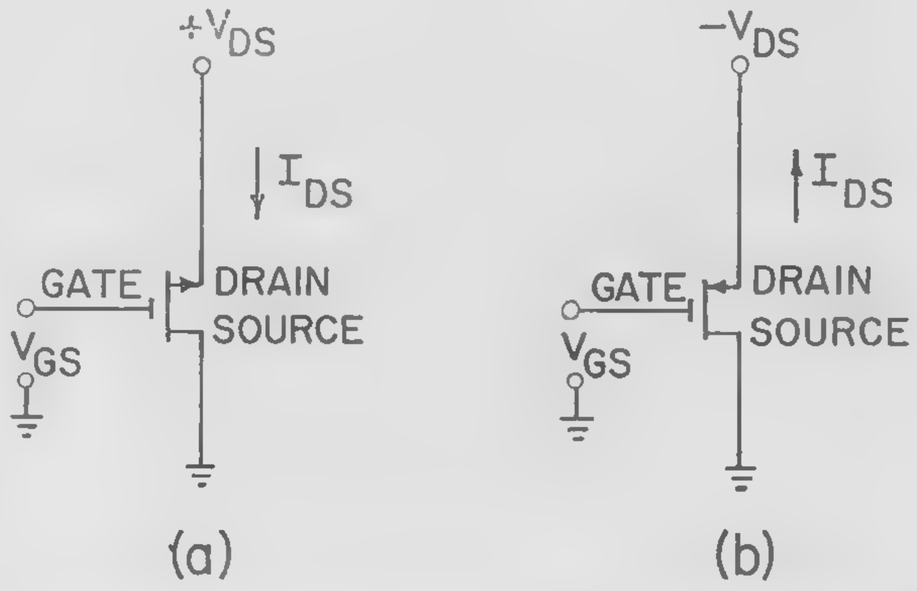


***FIGURE 2*—Suggested field-effect triode symbols and proper bias voltage polarities: *(a)* for *N* type element; *(b)* for the *P* type element.**

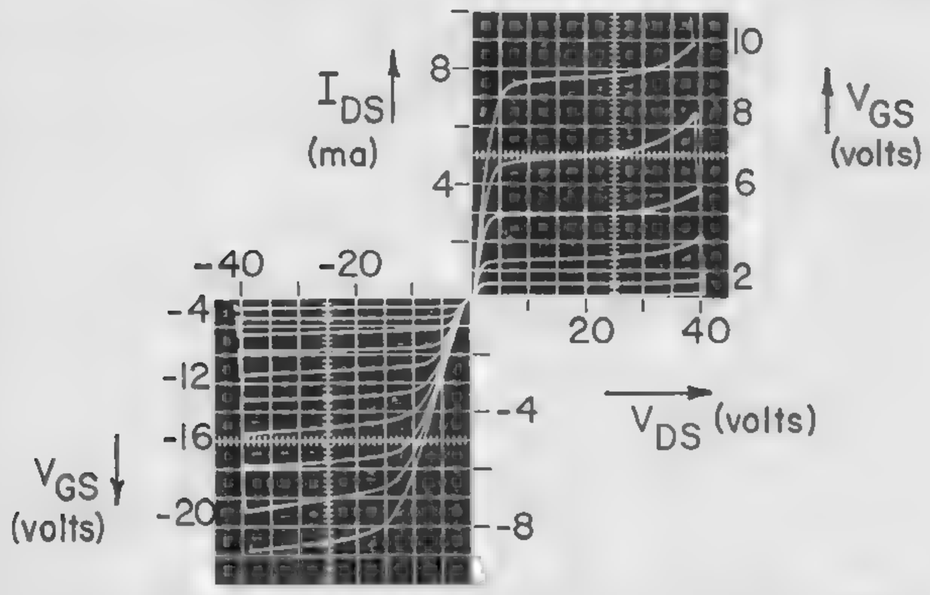


FIGURE 3—Characteristic curves for the field-effect triodes where drain current is plotted against drain voltage for source grounded and for different values of gate bias. The *N* element curves are plotted in the first quadrant.

(Left)

FIGURE 4—Low standby power inverter circuit; when $V_i = +V$, $V_o = -V$ and when $V_i = -V$, $V_o = +V$.

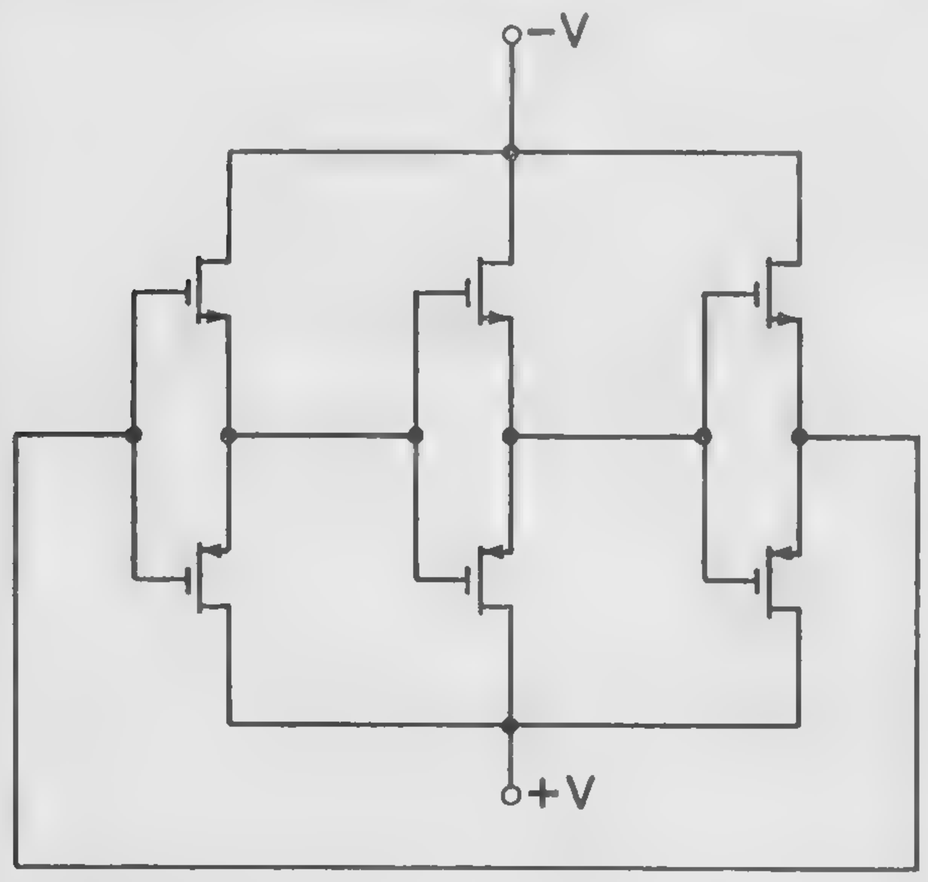


FIGURE 5—Ring-oscillator circuit for determining propagation delay of complementary inverter circuit.

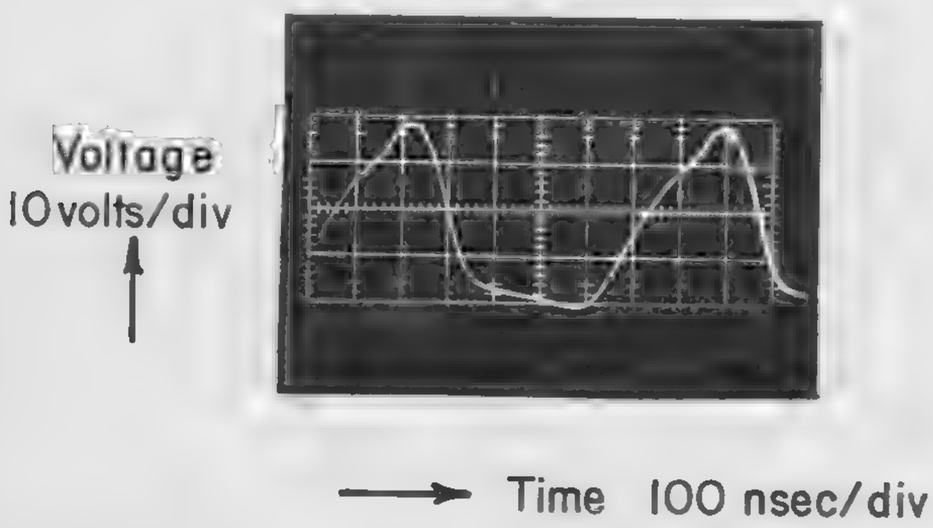
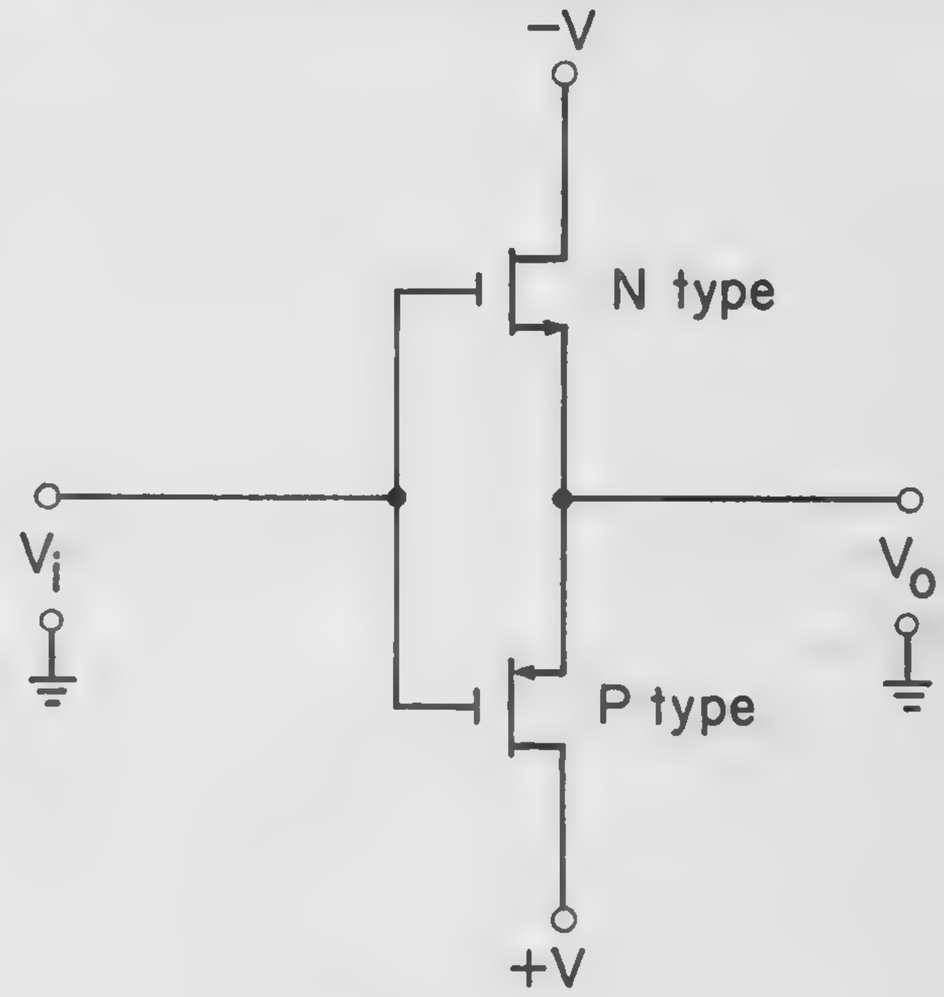


FIGURE 6—Plot of output voltage waveform from one stage of ring oscillator circuit.



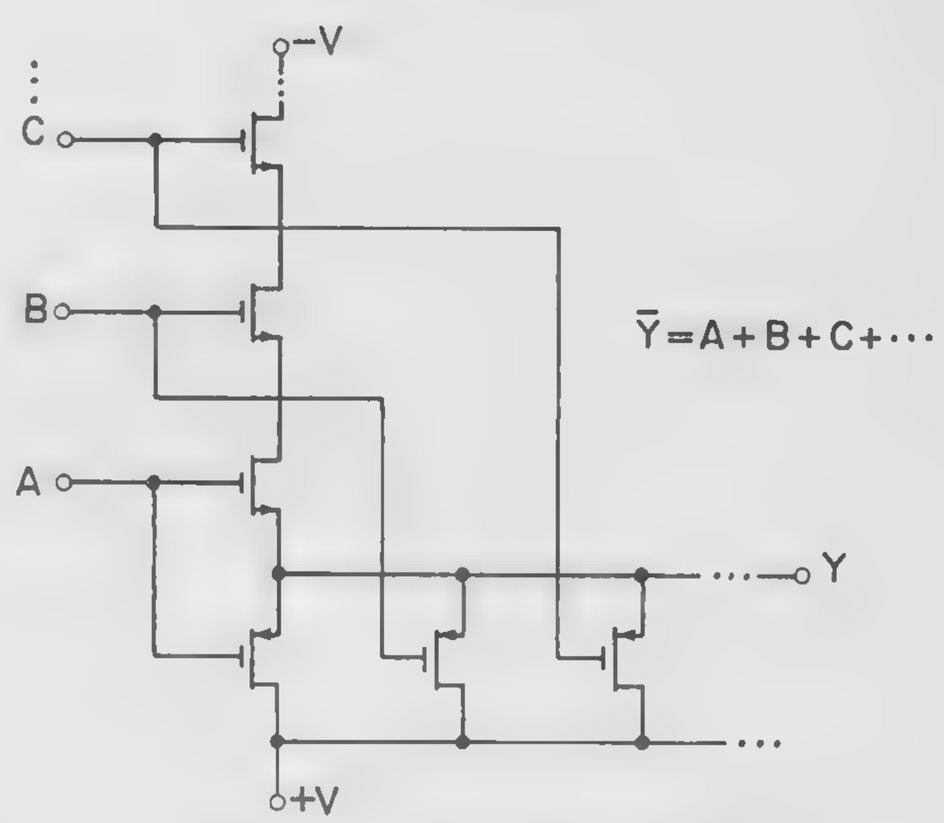


FIGURE 7—NOR logic circuit. If any of the inputs are $+V$ then the output will be $-V$.

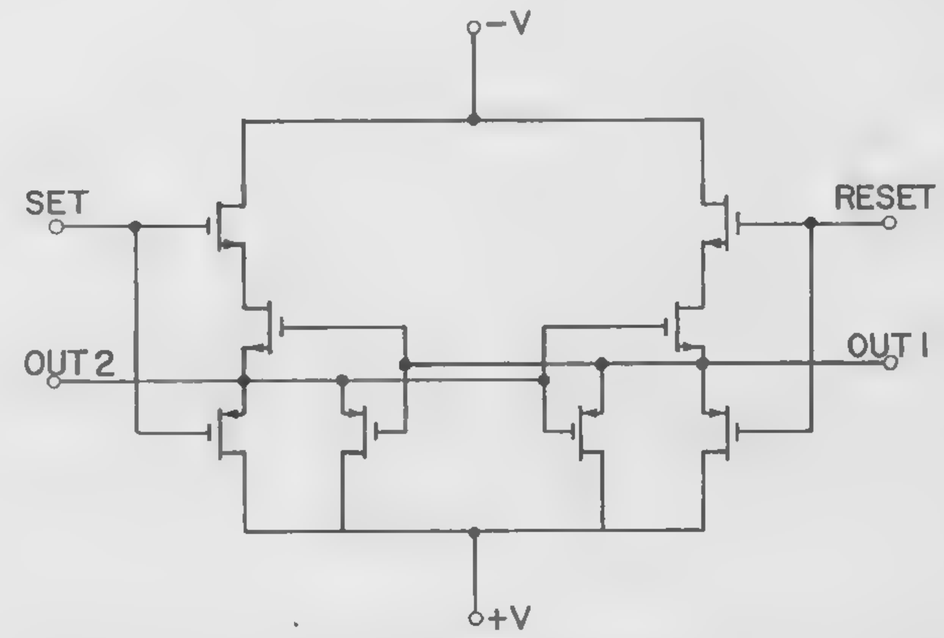


FIGURE 8—Set-reset flip-flop. A positive pulse on the set input will put output *1* at $+V$ and output *2* at $-V$; a positive pulse on the reset input will reverse the output voltages.

SESSION IV: Low-Frequency Circuits

Chairman: R. L. Bright
Westinghouse Electric Corporation, Pittsburgh, Pa.

WPM 4.1: A Novel Method of Polyphase Sine-Wave Generation with Silicon Controlled Rectifiers

R. H. Murphy and K. P. P. Nambiar

Transitron Electronic Ltd.

London, England

Recent investigation* of an electronic analog of the conventional rotary alternator, in which the current inducing magnetic field was sequentially switched rather than mechanically rotated, has resulted in a new technique of polyphase sinusoidal waveform synthesis. In fact, it would now appear that any rotary sequential switch (electronic or mechanical) can be made to produce across diametrically opposite nodes or contact points polyphase repetitive waveforms that closely approximate the sinusoidal.

The circuitry associated with the switch requires the special network geometry illustrated in Figure 1. This can be viewed as a cyclic ladder of RC differentiating networks on which the point of the step-function excitation is moved progressively round the loop at a constant switching speed. The waveform generated on any contact of the switch then comprises a series of exponentially-recovering segments between abrupt voltage transitions of constant magnitude K (expressed as a fraction of supply voltage E) as illustrated in Figure 5*a*. The waveform on the diametrically opposite contact is displaced in time relative to this as shown in Figure 5*b*.

With correct choice of the time-constant parameter RC, the boundaries of these waveforms closely approximate $E\cos^2\left(\frac{\theta}{2}\right)$ and $E\ (\cos^2\left(\frac{\theta}{2}\right)+K)$ in the case of Figure 5*a* and $E\sin^2\left(\frac{\theta}{2}\right)$ and $E\ (\sin^2\left(\frac{\theta}{2}\right)+K)$ in the case of Figure 5*b*, where K depends only on the number of stages in the ring.

From the following identities:

$$E\cos^2\left(\frac{\theta}{2}\right)-E\sin^2\left(\frac{\theta}{2}\right)=E\cos\theta,$$

and $$E\ (\cos^2\left(\frac{\theta}{2}\right)+K)-E\ (\sin^2\left(\frac{\theta}{2}\right)+K)=E\cos\theta$$

the algebraic sum of the voltages across diametrically opposite stages conveniently cancels the abrupt transitions, yielding an approximately sinusoidal waveform of half-cycle peak magnitude E and frequency equal to the frequency f_o of revolution of the count. The process may be illustrated by means of polar diagrams, Figure 4, which not only represent the time variation of voltage during one cycle on one contact, but also sets of voltage variations with time during one triggering period on all contacts. Hence, the foregoing argument also describes the production of $N/2$ sine waves having relative phase relationships determined solely by the geometrical relationship of the pairs of opposed stages, i.e., distributed $\frac{360^\circ}{N/2}$ to each other and thus representing a set of $N/2$ phase waveforms. Here the analogy with the mechanical alternator is apparent, since the phase relationship in switched mechanism depends on a network geometry which is analogous to the spacial geometry in the rotating machine.

The network geometry is ideally suited to the use of silicon controlled rectifiers as the switch contacts because the capacitors can be used for commutation purposes. In fact, the circuit was developed from an *scr* ring-counter switching numerical indicator units, when it was realized that circuits of this kind could switch currents of *20a* or more at frequencies in the kc region, and thus cover the power and frequency range desirable for static inverters. This is envisaged to be the basic potential use of the technique; a prototype six-stage three-phase design, Figure 7, has been built and undergone extensive testing. In this model, the resistors in Figure 1 were replaced by center-tapped primary windings of three standard single-phase transformers, the secondaries of which were connected in Y to supply a balanced three-phase load. The prototype illustrated the predicted ultra-stable frequency and phase characteristics, which depend solely on the stability of the low-power trigger circuit and the passive network geometry of the commutation network, respectively, together with the significant advantage over most contemporary three-phase *scr* inverter designs, since but one set of trigger pulses is required by virtue of the simple ring-counter system employed.

Acknowledgment

The authors wish to acknowledge the very useful discussions with *A. R. Boothroyd* of the Imperial College of Science and Technology, University of London, during the investigation of the problem.

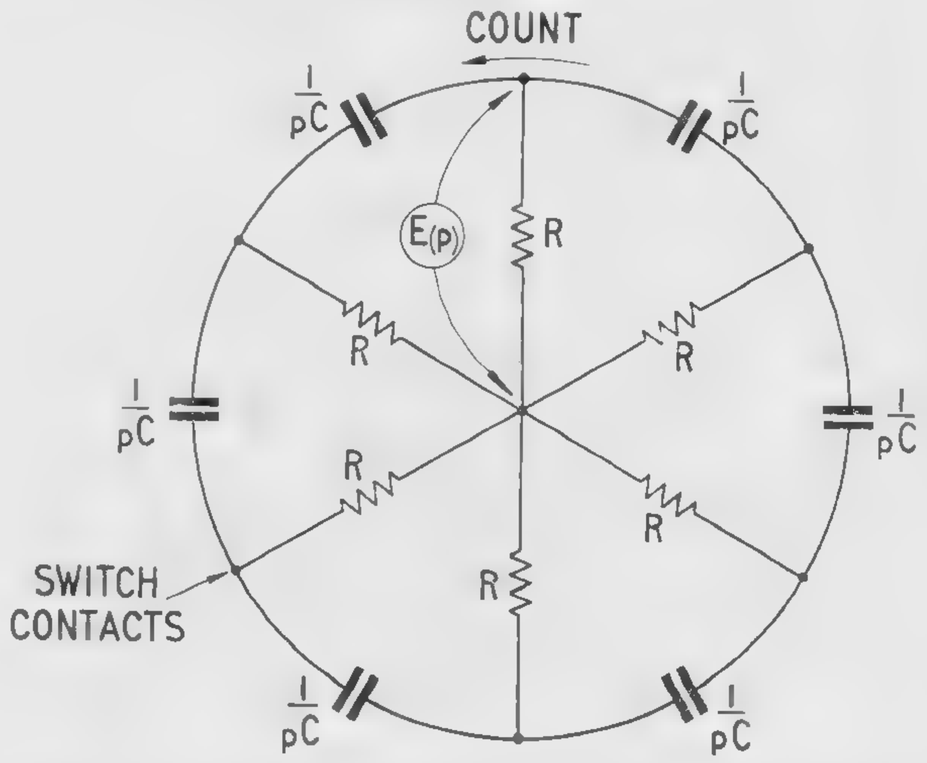


***FIGURE 1*—Network geometry associated with six-stage polyphase sinewave generator. The midpoint is one supply rail, and the switch contacts are sequentially connected to the other.**

* Murphy, R. H., and Nambiar, K. P. P., "Silicon Controlled Rectifier Static Alternators," to be published.

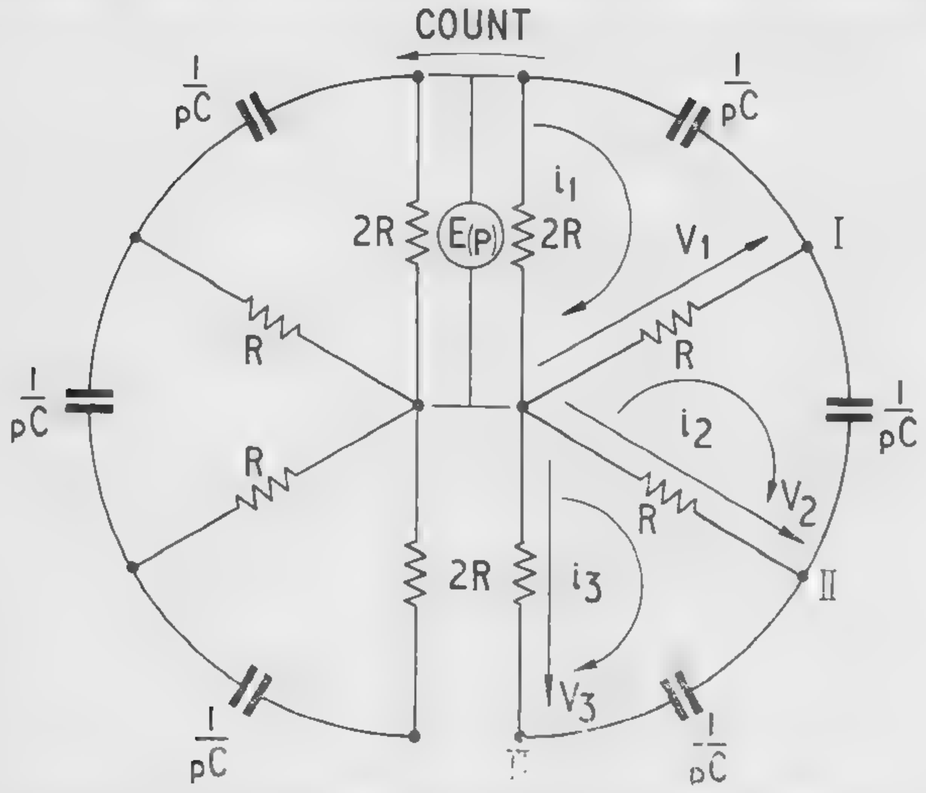


FIGURE 2—**Equivalent circuit in a form suitable for loop analysis. The waveform segments on contacts *I, II* and *III* are found to be of the form:**

$$V(t) = [V\,A \exp(\alpha \frac{t}{CR}) + B \exp(\beta \frac{t}{CR}) + C \exp(\gamma \frac{t}{CR})]$$

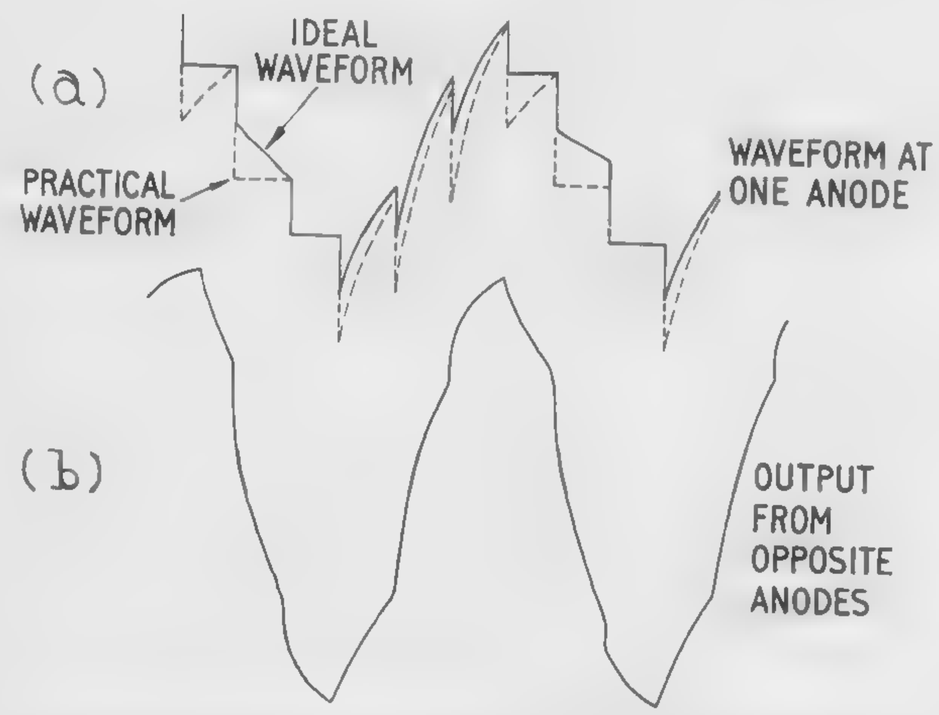
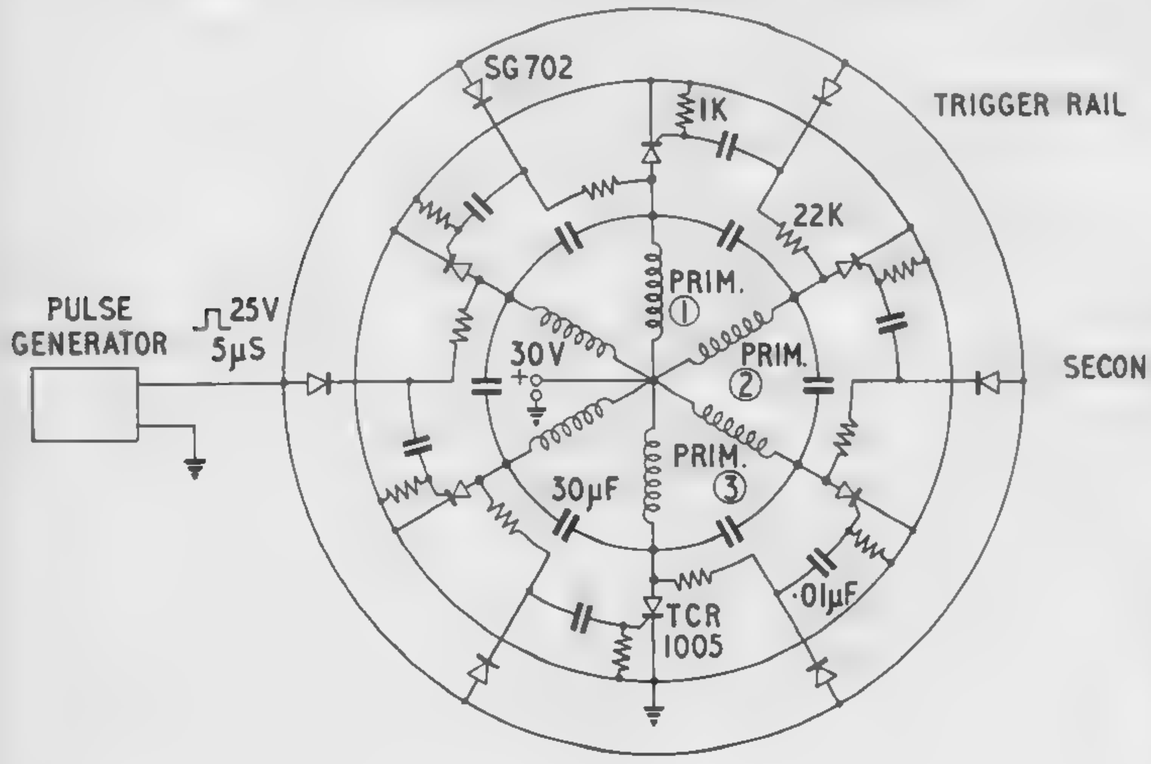


FIGURE 3a **and** *b*—**A waveform at one switch contact is shown in** *(a)*. **The ideal waveform cannot occur in practice because all exponential segments must recover towards the positive supply, *E*. In** *(b)* **is the waveform across diametrically opposite contacts.**



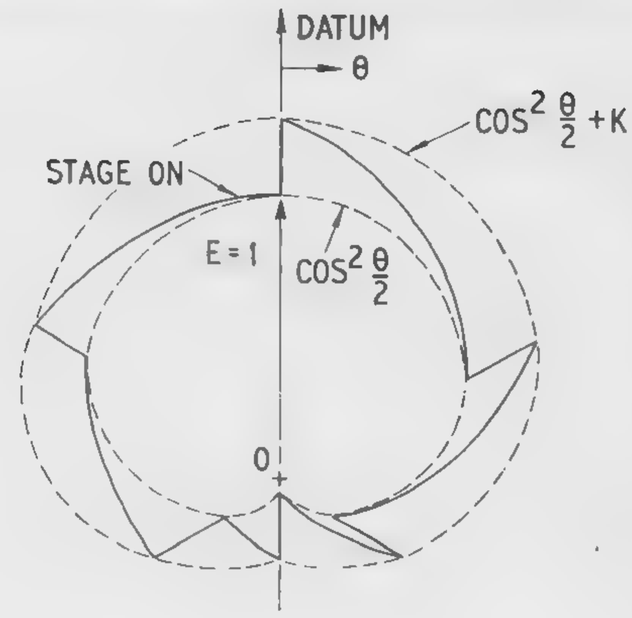


FIGURE 4—**The ideal waveform of Figure *3a* drawn with polar coordinates. The analysis yields $f_o \approx \frac{1}{4CR}$, where f_o is the optimum output frequency.**

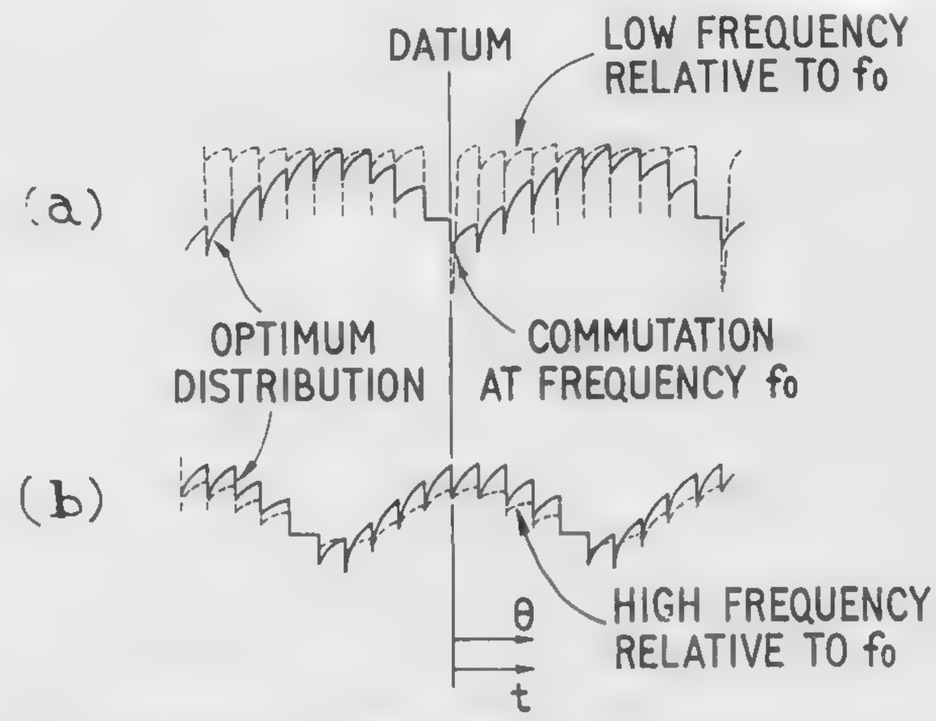


FIGURE 5a **and** *b*—**Waveforms for a ten-stage generator showing the relationship of diametrically-opposite voltage distributions and the effect of changing the frequency; time scale not constant.**

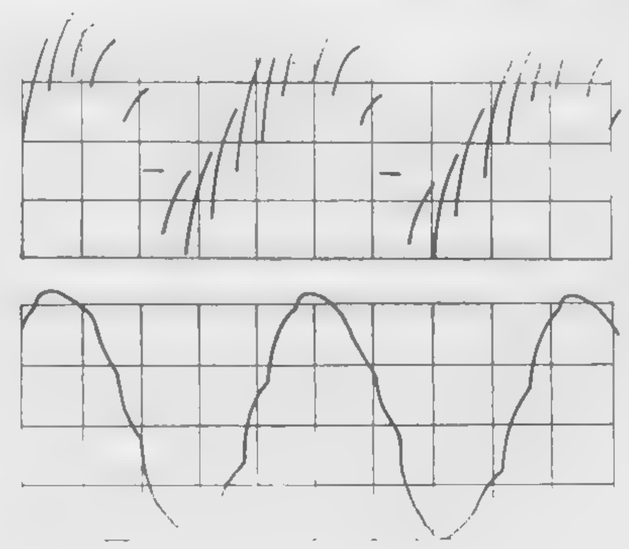


FIGURE 6 — **Oscillograms for the ten-stage generator. Notice the reduction in harmonic content of the output compared with that of the six-stage circuit.**

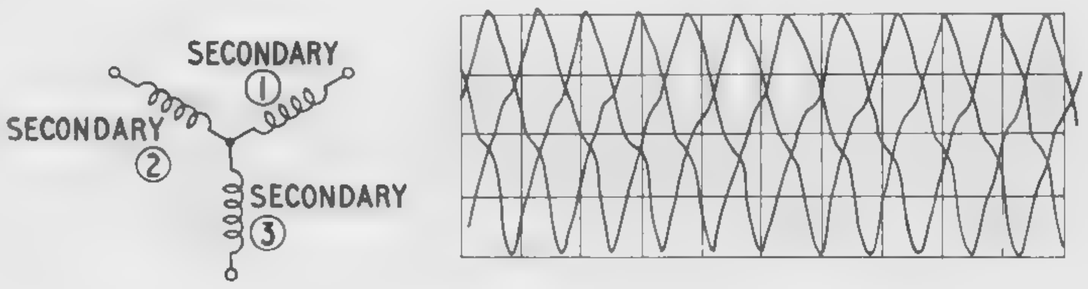


FIGURE 7—**Circuit diagram and oscillograms of output waveforms for the prototype *250 va, 30 v dc* to *80 v* 3-phase, *400 cps* inverter. The center-tapped transformer primaries replace the load resistors of Figure 1.**

SESSION IV: Low-Frequency Circuits

WPM 4.2: A SCR Regulated Power Supply with High-Speed Transient Response

B. Kruger

Martin Marietta Corporation

Baltimore, Md.

THIS PAPER will describe a silicon controlled rectifier regulated power supply which consists of a full-wave rectifier employing *scr*'s, a *LC* filter and a control and firing circuit. The control and firing circuit uses only one active element, a transistor. This supply circuit has the following properties:

(1)—High regulating accuracy.
(2)—Fast transient response and small transients; Table 1.
(3)—Wide range of stable operation; Figure 4.
(4)—High reliability.
(5)—High power range, up to *20 kw*.

Stability problems often occur in regulated power supplies with *LC* filters because of the close to *180°* phase shift these filters introduce. From linear network theory, it is known that phase advancing (differentiating) rather than phase-delaying (integrating) feedback networks should be used to obtain stability. Although *scr* networks are not linear, the linear theory is a fruitful approach to *scr* network stability problems and has yielded excellent results.

In the linear network in Figure 1, representing a regulated supply, the system gain is lumped into one amplifier with gain F and low output impedance. With phase-advancing capacitor C_2 a gain-independent stability condition is obtained which, however, is difficult to satisfy as C_0 is large. The system is always stable if $g = 0$. As the *dc* output voltage has to be sensed, unfortunately we always have $g \neq 0$. By adding a loop with less phase shift to the system, Figure 2, these difficulties are overcome. The stability condition is satisfied for *0* and infinite gain because a_0 and a_3 are always positive. The conditions $a_1 > 0$ and $a_2 > 0$ are easily met, in which case the stability condition is satisfied for all values of F.

A blocking oscillator is used as an error signal amplifier and firing circuit. Ample power is available from a blocking oscillator for firing one or more *scr*'s in parallel under worst-case conditions.

The foregoing ideas are implemented in the circuit in Figure 3. The *scr*'s are used in a bridge circuit, but any other full-wave rectifier could equally well have been employed. Three feedback loops are used, one *dc* loop for controlling the *dc* output voltage and two *ac* loops with phase-advancing networks.

It should be noted that the phase-advancing *ac* feedback loops feed the output ripple voltage directly into the blocking oscillator. The firing of the *scr*'s is thus controlled by the output ripple, giving the circuit very fast response. During start, the output voltage will rise like a ramp due to the *ac* feedback loops, thus limiting the charge current of the filter capacitor. Saturation of the filter inductor L is therefore avoided, and current-limiting protection circuits for rectifiers and *scr*'s are not needed.

Overcurrent protection is easily incorporated in the circuit, as only the triggering of the blocking oscillator needs to be prevented.

The stability diagram in Figure 4 was obtained from a variable supply for *5* to *20 v* and *12 a*. For a given *dc* setting, the *ac* input voltage can be varied over a 1:2 range; and for a given *ac* voltage, the *dc* voltage can be varied 1:4. A variation of ± *20%* in the component values in the feedback loops changes the range of stable operation insignificantly.

The transient response for a *20* to *140-v* supply (two ranges; *20* to *80 v* and *70* to *140 v*) and *10-a* supply is shown in Table 1. At *140 v* output, transients are measured to be less than *1%* for a *30%* load change. Figures 5*a* and b show two typical oscillograms.

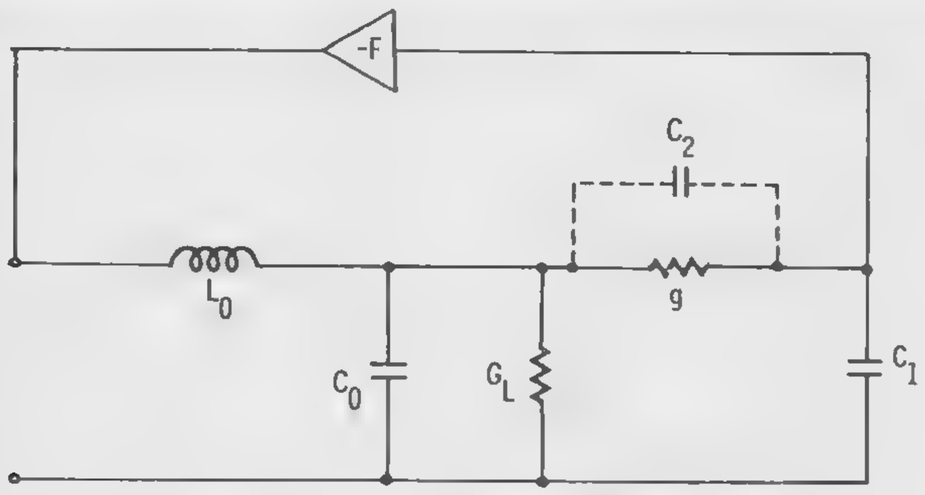
The regulation and peak-to-peak ripple is shown in Table 2. The load regulation is better than ± *0.1 v* over the entire output voltage range.

Output Setting (volts)	*Load Change (step) (amperes)*	*Transient Peak Value (volts)*	*Duration (msec)*
20	0 to 10	6	300
	10 to 0	4	100
	6.7 to 10	1.3	50
	10 to 6.7	1.0	30
80	0 to 10	3	300
	10 to 0	8	300
	6.7 to 10	0.8	40
	10 to 6.7	1.2	40
140	0 to 10	3	300
	10 to 0	6	400
	6.7 to 10	0.6	40
	10 to 6.7	1.0	50

TABLE 1—Measured transient response.

Output Setting (volts)	*Measured Output (volts)*	*Load Current (amperes)*	*Peak-to-Peak Ripple Voltage (millivolts)*
20	20.00	0	20
	19.90	5	50
	19.85	10	75
60	60.00	0	25
	59.85	5	110
	59.82	10	150
100	100.00	0	80
	100.00	5	180
	100.00	10	240
140	140.00	0	110
	139.90	5	200
	139.90	10	300

TABLE 2—Measured regulation and ripple voltage.



L_0C_0: LC FILTER
G_L: LOAD
g C_1C_2: FEEDBACK NETWORK
F: SYSTEM GAIN

STABILITY CONDITIONS:

IF $C_2 = 0$

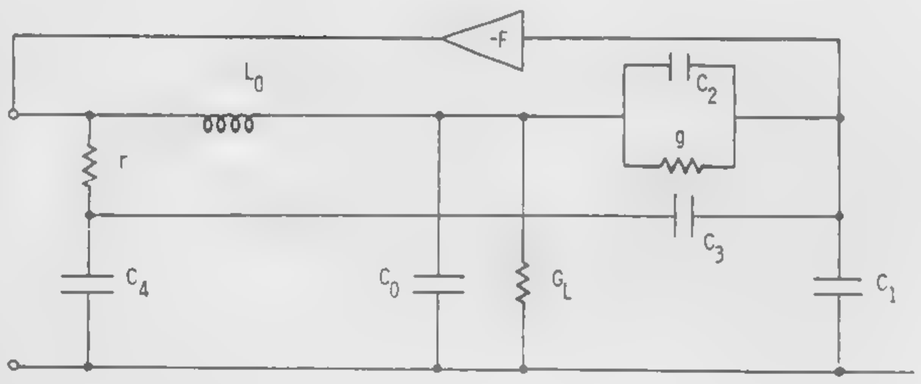
$$F < G_L\left(G_L \frac{L_0}{C_0} + g \frac{L_0}{C_1} + \frac{C_1}{g C_0}\right)$$

IF $C_2 \neq 0$

$$C_2(C_1 + C_2) \geq \frac{g}{G_L} C_0C_1$$

ALWAYS STABLE IF g = 0

FIGURE 1—Stability conditions.



L_0C_0: LC FILTER
G_L: LOAD
g r C_1 C_2 C_3 C_4: FEEDBACK NETWORK
F: SYSTEM GAIN

STABILITY CONDITION:

$$a_0 + a_1F + a_2F^2 + a_3F^3 > 0$$

FIGURE 2—Stability conditions; improved feedback network.

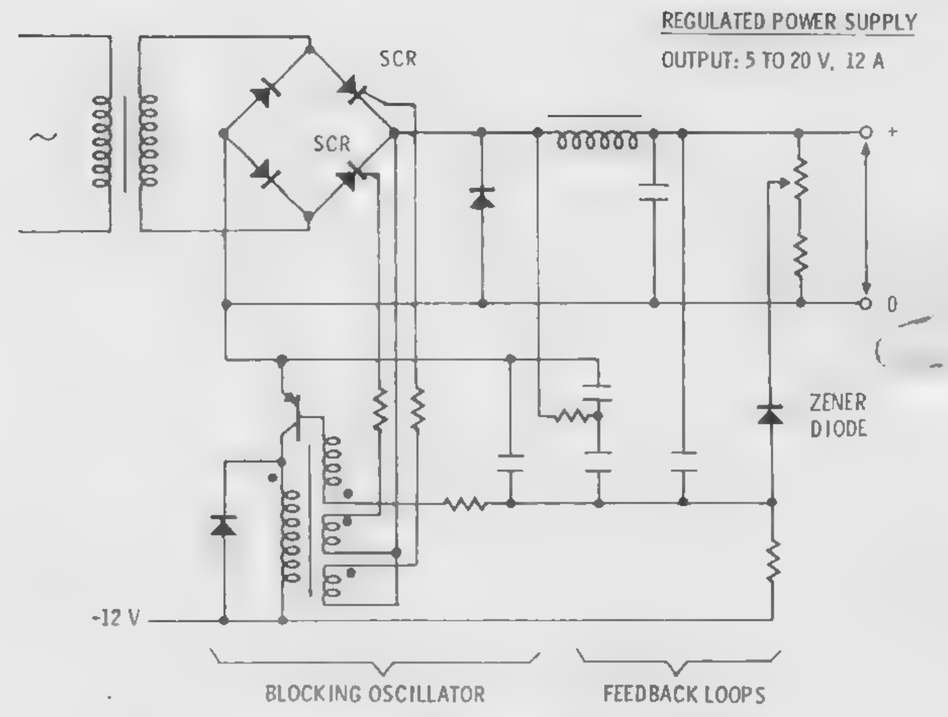


FIGURE 3—Typical circuit diagram.

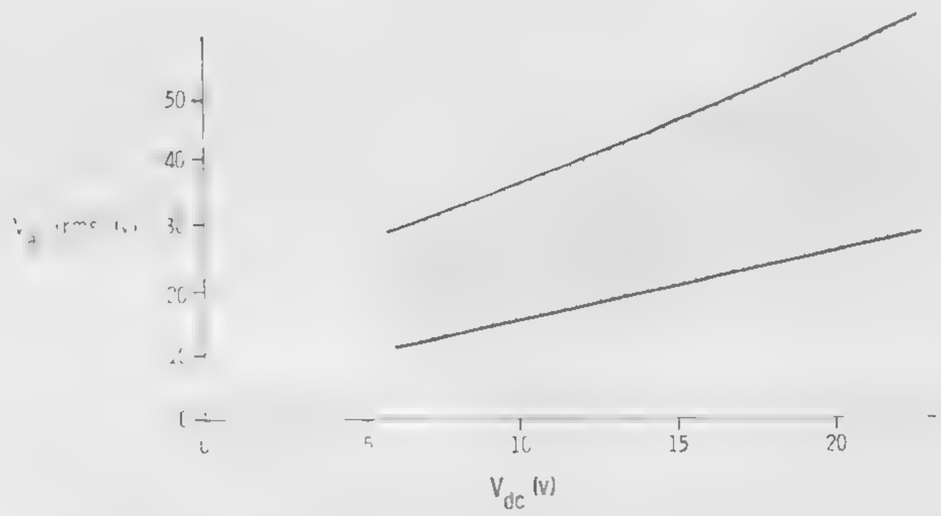


FIGURE 4—Range of stable operation.

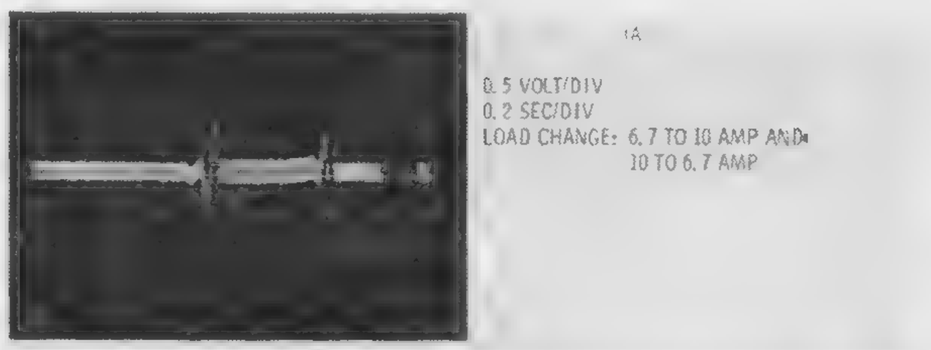


FIGURE 5—Transient response at *140-v* output of variable *(20-* to *140-v)* power supply.

WPM 4.3: A Circuit with Logarithmic Transfer Response Over 9 Decades

J. F. Gibbons and H. S. Horn

Stanford University

Stanford, Calif.

In many different types of analog circuits, one frequently needs to perform the nonlinear operations.

$$y = \log_a x \qquad (1)$$
$$y = a^x \qquad (2)$$

with a usually equal to *10* or e. These operations can be accomplished effectively by using a silicon transistor as the feedback element or input element of an operational amplifier. This paper will describe such a system whose transfer response can be represented by equations *(1)* or *(2)* over a dynamic range of nine decades with an error of less than *1%*. The dynamic range and accuracy of the circuit far exceed typical circuits which use a *pn* diode for the logorithmic device.

The transfer response time of the circuit is limited by the speed of the operational amplifier over a range of approximately five decades, and by stability and noise considerations over the full nine-decade range.

If a transistor is operated with zero volts on the collector-base junction, the collector current-versus-emitter voltage relation is

$$I_c = I_1\left(e^{\frac{aV_E}{kT}} - 1\right) \text{ where } I_1 \text{ is a constant} \qquad (3)$$

The validity of equation *(3)* is independent of parasitic resistances; it is also independent of carrier-trapping phenomena and other uncontrollable effects which usually cause the emitter current in the transistor (or the total current in a diode) to vary as $[\exp qV_E/nkT - 1]$, where n varies from unit to unit and is a function of I within a given unit.

Experimental verification of equation *(3)* over a range of nine decades is given in Figure 1; similar plots can be obtained for most silicon transistors*. The slope of the plot is kT/q per neper to within the accuracy of the measurements.

Exponential Operation

A convenient way to utilize the characteristic given in Figure 1 for taking logarithms is to use the transistor as the feedback element in an operational amplifier, as shown in Figure 2*a*. The collector is tied to the summing point and the emitter to the output, so that the output voltage is proportional to the logarithm of the input voltage. Exponential operation is obtained by utilizing the transistor as the input element of an operational amplifier, the emitter being driven from an operational scaling of the input voltage or current, the collector being tied to the summing point; Figure 2*b*. Combinations of these two schemes permit multiplication, division, raising to a constant power, raising to a functional power, etc.

In all of these circuits, the amplifier A must be designed to have extremely low-input current, high-input impedance, extreme dynamic range, low noise and high speed to utilize fully the *logging* transistor's capability. Amplifier designs which meet these requirements will be described.

* Sah, C. T., "Effect of Surface Recombination and Channels on PN Junctions and Transistors," *IRE Trans. PGED*, vol. ED-9, p. 94-108; January, 1962.

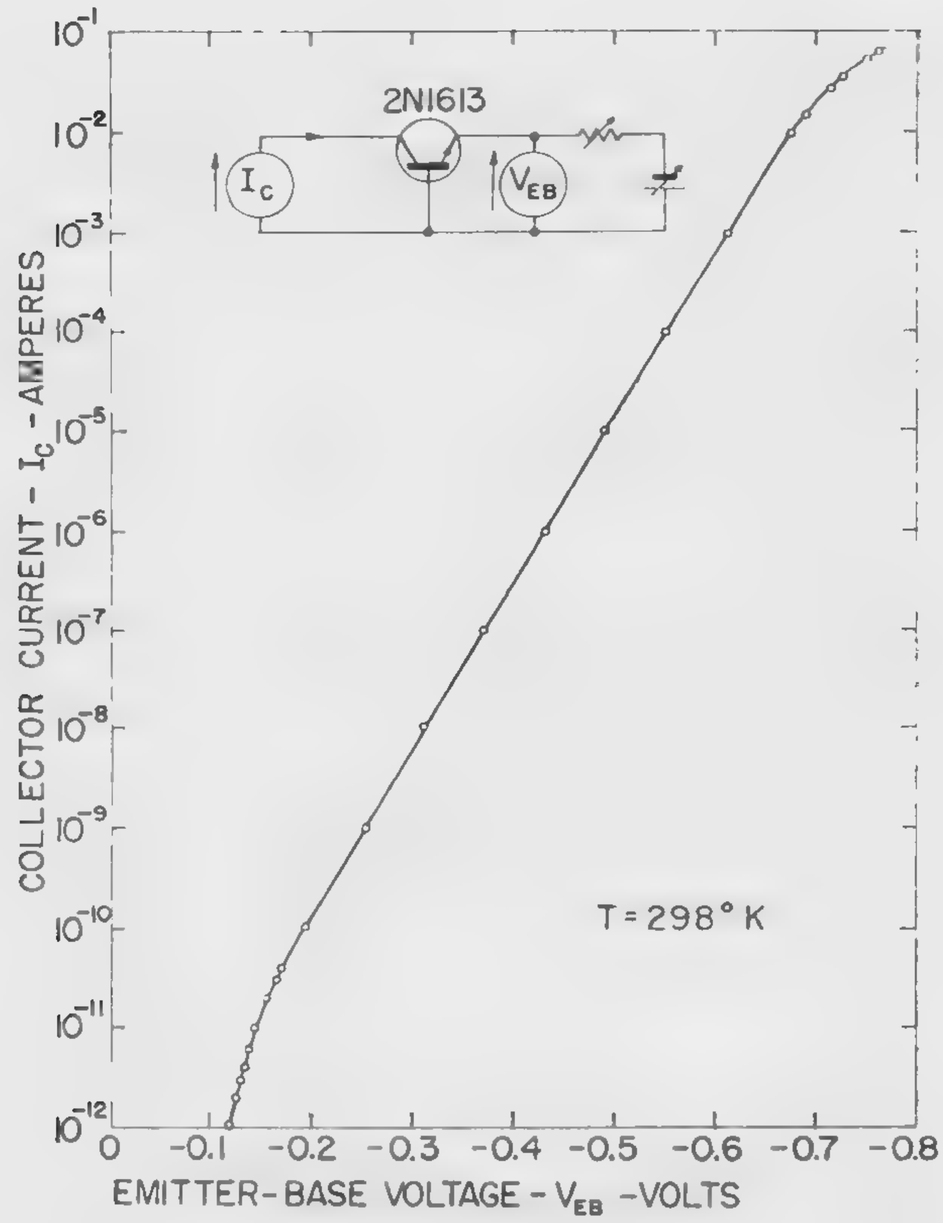
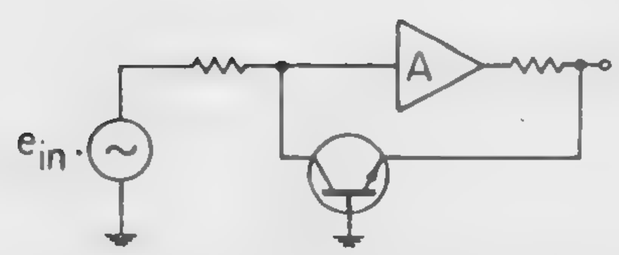
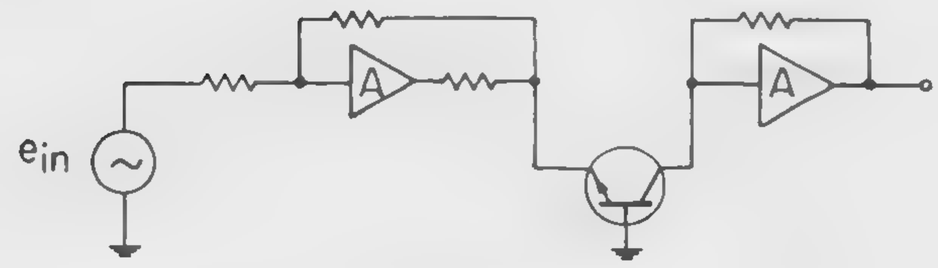


***FIGURE 1*—Log I_C-V_{EB} characteristic for a 2N1613 transistor.**



(a) Circuit for performing $y = \log x$



(b) Circuit for performing $y = a^x$

***FIGURE 2*—Basic circuit arrangements for taking logarithms and exponentials.**

SESSION IV: Low-Frequency Circuits

WPM 4.4: A High-Performance Universal Operational Amplifier

D. Hilbiber and D. Leistiko, Jr.

Fairchild Semiconductor Div., Fairchild Camera-Instrument Corporation

Palo Alto, Calif.

THE RECENT ADVENT of the planar field-effect transistor‡ has led to the design of an operational amplifier that represents a good compromise of all the requirements for this class of circuit. Typical performance of this amplifier provides

Gain-bandwidth product	~ 2 *Mc*
Open-loop voltage gain	$\sim 10^5$
Residual input current	$\sim 3 \times 10^{-11}$ *a*
Incremental input impedances	$\sim 10^{11}$ ohms in parallel with 2 *pf*
Equivalent input drift	< 5 *μv/°C* $(0°C < T < 60°C)$
Common mode rejection	> 80 *db*

With proper shielding the amplifier can be operated from source impedances greater than *10 megohms* with a slight degradation of frequency response.

The amplifier is relatively simple and straightforward; Figure 1. Briefly, the differential field-effect transistor pair drives a differential *pnp* stage, with the signal output taken single-ended at this point. Sufficient stages follow to provide the current gain needed to realize the desired output capability. The input stage must be designed in such a way as to minimize the load seen by the signal source, and to provide the greatest possible common mode rejection. The amplifier input capacitance will limit the maximum frequency response when operating from a high source impedance. From the equivalent circuit of the field-effect transistor (Figure 2), the effective input capacitance is given by $C_{input} = C_{SG} + \mu' C_{DG}$, where μ' is the stage amplification factor and the capacity is from gate to source and drain. For the devices employed, $C_{SG} \approx C_{DG} \approx 5$ *pf*, and thus the net input capacitance can be quite large. The *Miller* effect can be readily overcome by applying the same remedy as used for vacuum tubes; namely, the tetrode configuration. Such a *device-block* is shown in Figure 3. The drain voltage excursion of Q_{1a} is effectively reduced from the output voltage by the factor $\mu = g_m r_D$ of Q_{1b}. Hence, $C_{input} \approx C_{SG} + C_{DG}$. In a similar sense, the effect of r_{GD} is likewise reduced. Since the values of r_{GD} and r_{SD} are typically on the order of 10^9 *ohms*, it is fairly easy to obtain input resistances of 10^{12} *ohms* when operating in the unity gain buffering configuration. The upper frequency limit of the amplifier is primarily determined by the *pnp* stage, as a result of low current f_T and the load seen by the field-effect transistor arising from emitter-base associated capacitances. Figure 4 shows the response of the amplifier to a *1-kc* square wave: *(a)* operating with a *600-ohm* source, and *(b)* with a *1-megohm* resistive source.

To obtain a good common-mode signal rejection figure, the operating bias point of the field-effect pair must remain nearly constant. That is, since the common mode voltage is seen as a change of V_D, then ideally,

$$\frac{dI_D}{dV_D} \to 0$$

For a given temperature, the drain current is

$$I_D = I_{D_0} + g_m (V_G - V_{G_0}) - g_D (V_D - V_{D_0})$$

where the zero subscripts indicate quiescent values, and g_D is the channel conductance. Hence, if I_D is forced to remain constant by the circuit, then

$$g_m (V_G - V_{G_0}) = g_D (V_D - V_{D_0})$$

Thus, for a given drain voltage excursion $\Delta V_D = V_D - V_{D_0}$, a change of gate voltage $\Delta V = V_G - V_{G_0}$ will follow:

$$\Delta V_G = \frac{g_D}{g_m} \Delta V_D$$

It is obvious that unless g_D and g_m of the field-effect transistor pair are well matched, $\Delta V_{G1} \neq \Delta V_{G2}$, and the difference is the common mode induced error signal. The situation is improved considerably by using the field-effect tetrode mentioned, and by maintaining a constant-drain bias current by a feedback loop from the second stage to the current source.

‡ FET.

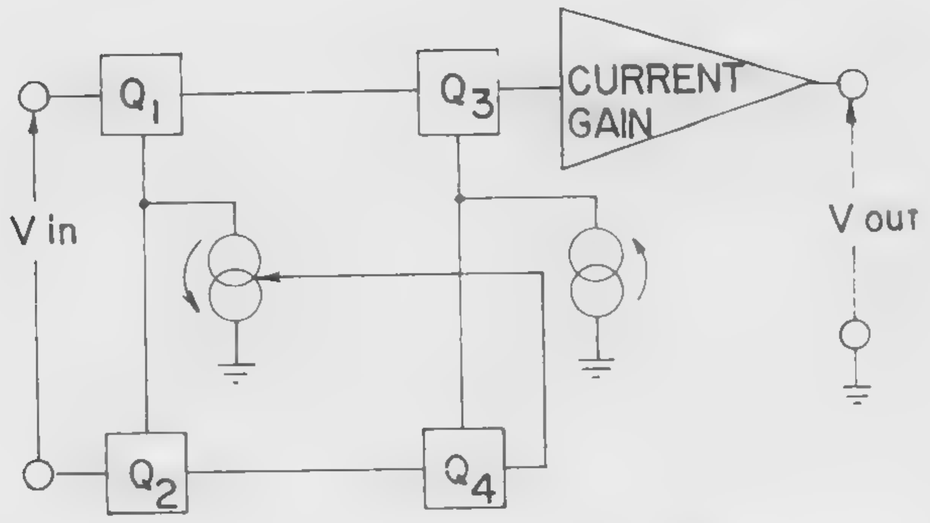


FIGURE 1—**Block diagram of the differential-input operational amplifier.**

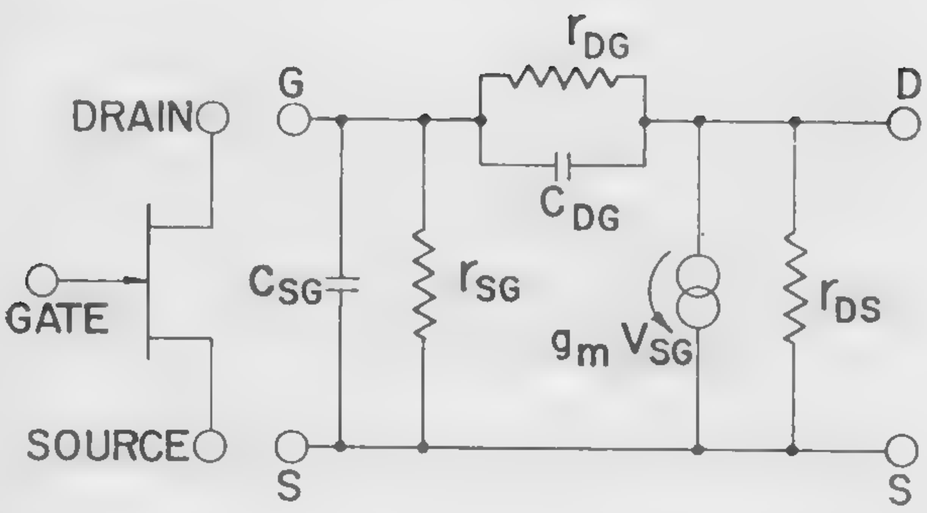


FIGURE 2—**Approximate equivalent circuit of a field-effect transistor.**

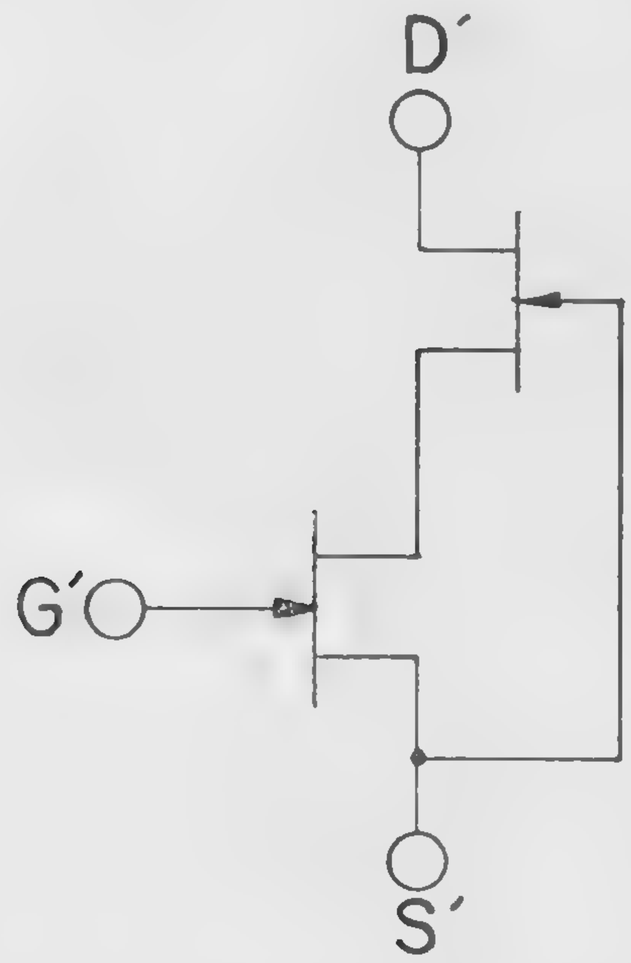


FIGURE 3—**Field-effect triode device block.**

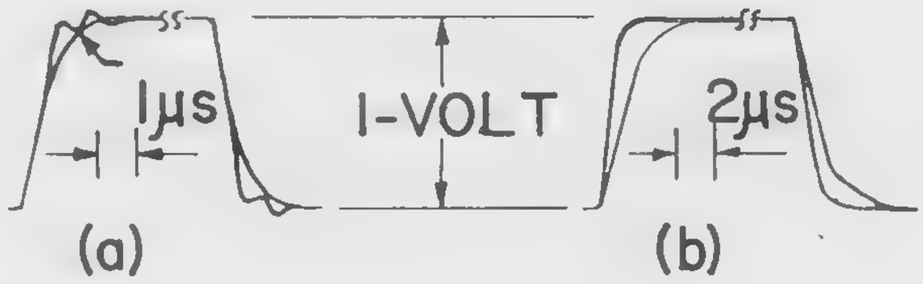


FIGURE 4—**Amplifier response to a *1-kc* square wave from: *(a)* 600-ohm source, and *(b) 1-megohm* resistive source.**

SESSION IV: Low-Frequency Circuits

WPM 4.5: A Low-Level DC Amplifier Using Solion Tetrodes

J. D. Merryman

Texas Research and Electronic Corporation

Dallas, Tex.

Amplifiers for low-level *dc* signals must generally be chopper stabilized because of the drift associated with transistors and vacuum tubes. A new amplifying element, the solion tetrode, has been found to have drift, noise, and temperature characteristics superior to those of both semiconductors and vacuum tubes. *DC* amplifiers built with solion tetrodes can achieve high performance, are less expensive, and consume less power than chopper amplifiers.

The solion tetrode is a hermetically-sealed electrochemical device consisting of four metallic electrodes in an aqueous solution. It is commercially available in a small pulse-transformer case that fits a seven-pin miniature socket.

The solion (Figure 1) may be regarded as a triode in which an input voltage, E_i, controls the output current, I_o, drawn from a supply of E_o volts. The input electrode (pin *1*), the readout electrode (pin *5*), and the common electrode (pin *7*), correspond respectively to the grid, plate, and cathode of a vacuum tube. The function of the fourth electrode, called the shield (pin *3*), will not be discussed in this paper, except to state that the shield must be maintained slightly negative with respect to the input electrode.

The solion has previously been described as an integrator[1,2], because the output current is directly proportional to the charge moved in the input circuit. Its static characteristics (Figure 1) show high output impedance, and a high transconductance that increases with output current. The transconductance may be shown theoretically to equal $2I_oF/RT$, where F is the Faraday, R is the universal gas constant, and T is absolute temperature.

Static input impedance of the solion is high. Spurious input current required to maintain a fixed operating point is 10^{-10} to 10^{-9} *a*.

Usefulness of the solion as a low-level *dc* amplifier is based on the excellent stability of the static characteristics with time and temperature. Production model solions show drifts in operating point of *3* μv per-day, referred to the input voltage, E_i. The temperature coefficient of solion input voltage is about one-seventh that of transistors, and is highly reproducible; random pairs match to within *1* μv per degree *C*.

The basic solion amplifier, Figure 3, is similar to typical differential arrangements used with vacuum tubes and transistors. R_1 sets the operating point. Common base transistors, Q_1 and Q_2, serve to limit the solion voltage to *0.5 v* while allowing use of large load resistances for high gain. Voltage gain of this circuit is *500*. The location of R_4 in the circuit is selected on the basis that two solions will have equal bias voltage, E_i, rather than equal operating currents, I_o. This is a criterion for low temperature coefficient.

Figure 4, the complex response of the basic solion stage, shows a *−3-db* point at about 10 *mcps*. This cutoff frequency and the input impedance of the amplifier may both be increased considerably by employing feedback around the solion stage. According to the equivalent circuit of Figure 2, this polar plot should lie entirely in quadrant *IV*. It does not, because of two effects not indicated in the simplified equivalent circuit: *(1)*—a transit-time effect similar to that occurring in transistors, and *(2)*—a feed-through capacitance between input and output electrodes, resulting in the *hook* in quadrant *III*. These effects must be considered in design of the rolloff network when applying feedback to the solion.

Solion Instrument Amplifier Design

Figures 5 and 6 show a solion instrument amplifier that uses feedback to improve frequency response and input impedance. Added transistor stages raise open-loop gain to about *650,000*, and provide a high-level, single-ended output. Closed-loop gain is *2500*, set by the feedback network, R_{18} and R_{19}.

Preliminary studies show that noise in solions is very low. The equivalent input noise of the Figure 5 amplifier is *3* μv *rms*. Even if the solions were noiseless, this much noise could be expected from the second stage transistors, because low gain of the solion between *0.1* and *3 cps* makes noise of the transistors important. A similar amplifier built with experimental high-K solions had a bandwidth of *40 cps* and equivalent input noise under *1* μv. (*K* is a controllable parameter of the solion that varies with the spacing between readout and common electrodes. The SE 110 units described throughout this paper have a *K* of *2.6;* the experimental units had a *K* of *40*. Higher *K* reduces the value of C_i in Figure 2.)

Drift performance of solions improves with age. Life test units now passing 5,000 hours exhibit drift reduced a factor of four from initial performance. This suggests an equilibrium which can be attained early by an accelerated pre-aging.

Theoretical considerations indicate that present performance does not constitute a limit. In particular, it appears that a ten-fold improvement in drift and noise is likely.

---

[1] "An Introduction to Solions," *Texas Research and Electronic Corp.;* Feb., 1962.

[2] "Solion Principles of Electrochemistry and Low-Power Electrochemical Devices," *U. S. Dept. of Commerce* publ. PB 131931; August, 1958.

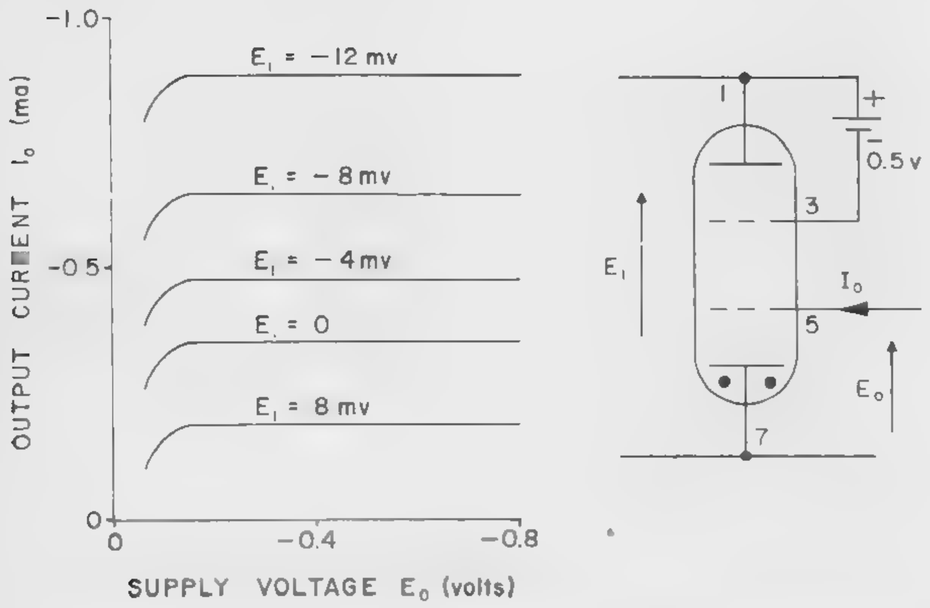


FIGURE 1—**Static characteristics of solion tetrode which resemble those of vacuum tube pentode. Output impedance is high.**

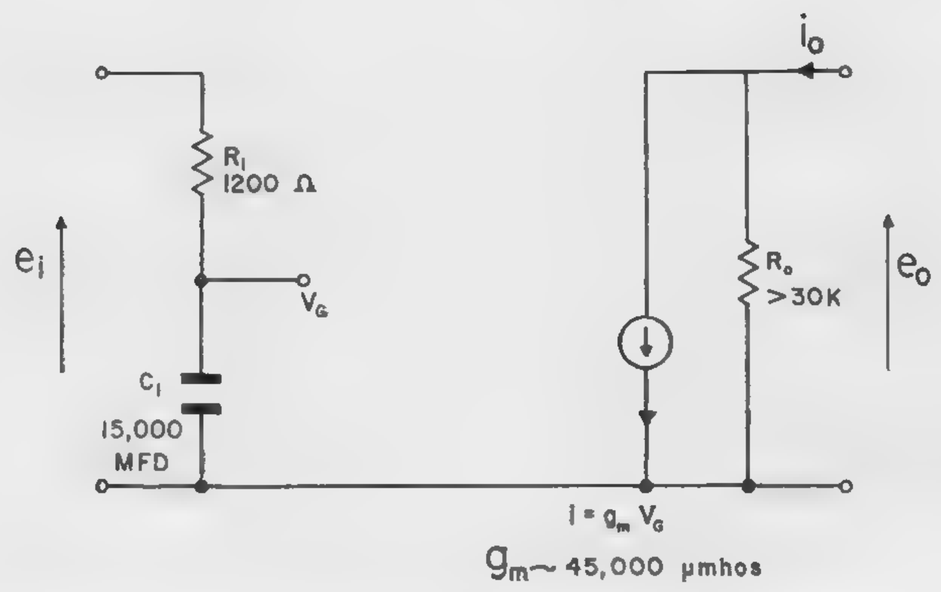


FIGURE 2—**Simplified equivalent circuit of solion. Note similarity to vacuum tube with low-pass filter in grid circuit. Values are typical of SE 110 solion tetrode at $I_o = -0.55$ ma.**

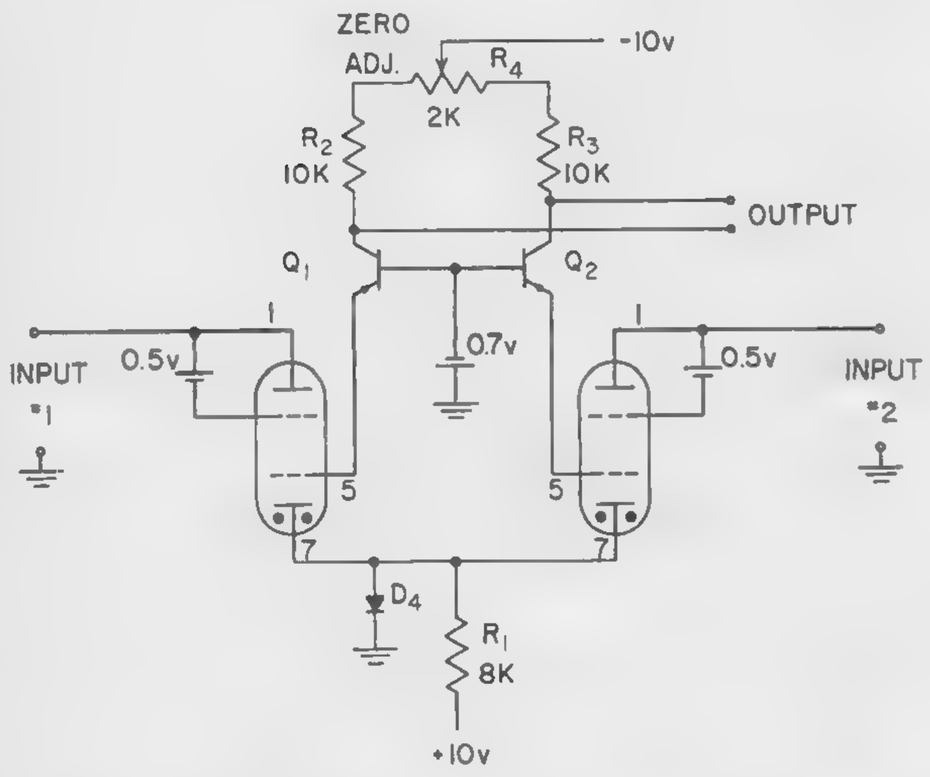


FIGURE 3—**Solion differential *dc* amplifier stage which has low drift and noise; voltage gain is *500*.**

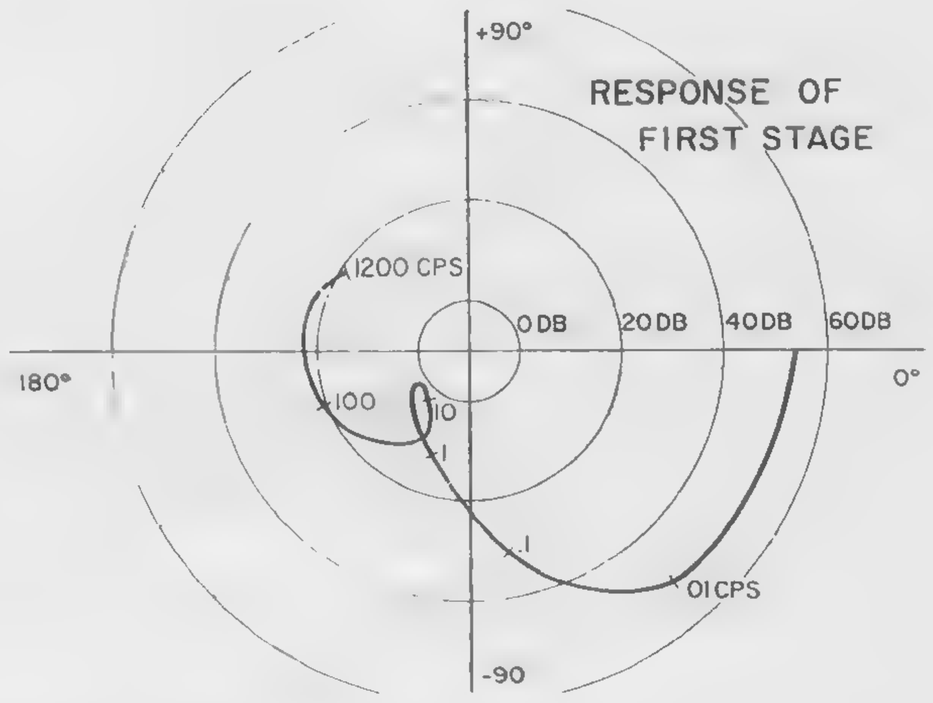


FIGURE 4—**Complex response of the Figure 3 circuit. Feedback factor of several hundred may be applied to flatten frequency response.**

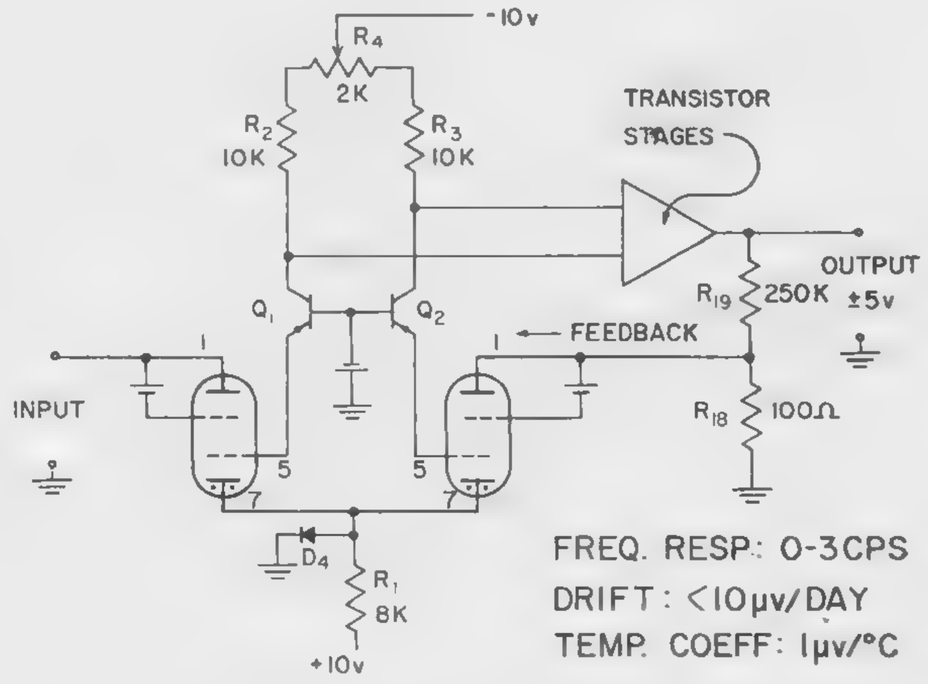


FIGURE 5—**The solion amplifier with feedback. Frequency response is increased to *3 cps*, and input impedance is increased to *25 kohm* at *0.1 cps*.**

Informal Discussion Sessions

WE 1: Integrated Linear Circuits

[West Ballroom]

Moderator: J. G. Linvill, Stanford University, Stanford, Calif.

Panel Members: A. P. Stern, Martin Marietta Corp., Baltimore, Md.

R. F. Pepper, University of California, Berkeley, Calif.

J. Narud, Motorola Semiconductor Products, Inc., Phoenix, Ariz.

G. Luecke, Texas Instruments, Inc., Dallas, Tex.

J. P. Ferguson, Fairchild Semiconductor, Div., Fairchild Camera-Instrument Corp., Palo Alto, Calif.

WE 2: Nanosecond Switching Circuits

[East Ballroom and Assembly]

Moderator: P. B. Myers, Martin Marietta Corp., Baltimore, Md.

Panel Members: O. H. Bartlett, National Security Agency, Washington, D. C.

B. E. Sear, Martin Marietta Corp., Baltimore, Md.

F. K. Buelow, IBM Corp., Poughkeepsie, N. Y.

C. N. Winningstad, Tektronix, Inc., Beaverton, Ore.

J. J. Gibson, RCA Laboratories, Princeton, N. J.

W. Peil, Electronics Lab., General Electric Co., Syracuse, N. Y.

WE 3: Magnetic Thin-Film Memories

[Pennsylvania West]

Moderator: W. E. Proebster, IBM Corporation, Yorktown Heights, N. Y.

Panel Members: A. V. Pohm, Iowa State University, Ames, Iowa

E. E. Bittman, Burroughs Corp., Paoli, Pa.

S. M. Rubens, Remington Rand Univac, St. Paul, Minn.

Q. W. Simkins, IBM Corp., Poughkeepsie, N. Y.

J. I. Raffel, MIT Lincoln Laboratory, Lexington, Mass.

I. W. Wolf, General Electric Co., Syracuse, N. Y.

A. H. Bobeck, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

E. M. Bradley, ICT, Ltd., London, England

D. A. Meier, National Cash Register Co., Hawthorne, Calif.

R. J. Petschauer, Fabri-Tek Inc., Hopkins, Minn.

Informal Discussion Sessions

WE 4: Statistical and Computer Techniques in Circuit Design

[Pennsylvania East]

Moderator: E. U. Cohler, Sylvania Electric Products Inc., Needham, Mass.

Panel Members: **L.** Hellerman, IBM Corp., Poughkeepsie, N. Y.

A. F. Malmberg, Los Alamos Scientific Lab., Los Alamos, N. M.

L. Spandorfer, Remington Rand Univac, Blue Bell, Pa.

G. H. Goldstick, Northrop Corp., Palos Verdes, Calif.

WE 5: Packaging and the Measurements Problem

[Independence-Constitution]

Moderator: R. P. Rafuse, Research Laboratory of Electronics, MIT, Cambridge, Mass.

Panel Members: N. Houlding, The National Co., Malden, Mass.

A. E. Bakanowski, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

R. L. Pritchard, Texas Instruments, Inc., Dallas, Tex.

K. E. Mortenson, Microwave Associates, Inc., Burlington, Mass.

V. Grinich, Fairchild Semiconductor, Div. Fairchild Camera-Instrument Corp., Palo Alto, Calif.

WE 6: Special Circuit Design Considerations for the Nuclear Environment

[Delaware Valley Suite]

Moderator: F. T. Lynch, Burroughs Corp., Paoli, Pa.

Panel Members: S. Sedore, IBM Corp., Owego, N. Y.

T. Hallman, Northrop Corp., Van Nuys, Calif.

D. Navon, Transitron Electronic Corp., Wakefield, Mass.

A. L. Long, Jr., Burroughs Corp., Paoli, Pa.

M. L. Embree, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

SESSION V: Microwave Circuits

Chairman: K. E. Mortenson

Microwave Associates, Inc., Burlington, Mass.

THAM 5.1: A Wideband High-Gain Transistor Amplifier at L-Band*

J. Hamasaki†

Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

RECENT PROGRESS in microwave transistor manufacturing technology has stimulated the application of transistors to microwave devices. This paper will describe a wideband high gain *L*-band transistor amplifier which consists of six common-emitter stages on a printed circuit board.

The transistor amplifier has several major advantages over the tunnel-diode amplifiers; among these are its intrinsic unilateral characteristic and higher power handling capability. With respect to noise performance, the tunnel-diode amplifier is still superior to the transistor amplifier, but it is felt that the noise performance of transistors will eventually be improved to become competitive with the tunnel diode.

The microwave transistor loses, to some extent, its intrinsic unilateral characteristics, partly because of parasitic elements. A simple calculation, based on measured parameters of microwave transistors, reveals that the output impedance shows a negative resistance if the transistor is used in a common-base configuration and operated at a relatively high gain. Therefore, to obtain matched input and output impedances and also to obtain cascaded amplification, the common-emitter configuration is considered more suitable for microwave amplification than the common-base configuration. Another analysis shows that if the external circuit is not properly designed, instability may occur at relatively low frequencies for both common-base and common-emitter configurations. To prevent this instability, it is desirable to load down the transistor at low frequencies by connecting a filter and a resistor to its collector.

There is an experimental transistor‡ capable of providing *5-db* gain per stage out to almost *2 Gc*. Figure 1 shows the circuit diagram of a single-stage common-emitter amplifier. The emitter is grounded for *rf* frequencies by means of a large capacitance, and the input signal is applied to the base through a series capacitance. The collector is grounded for *dc* through an *rf* choke. To prevent *rf* leakage to bias circuits, the *dc* voltages of the emitter and base are applied through low-pass networks shown in Figure 1. A series combination of a resistor and a parallel resonant circuit in the collector circuit secures low-frequency stability, and a low-pass type output network improves output impedance matching and peaks up the gain at the high-frequency edge of the band. Figure 2 shows the experimental results for this amplifier. The amplifier has a forward gain higher than *5 db* from *0.25 Gc* to *1.7 Gc*. The low frequency limit is determined by the *rf* chokes used in the amplifier. The input and output circuit have reasonable positive resistances over the entire band.

A six-stage *L*-band amplifier was built in the common-emitter configuration on a printed circuit board. Figures 3 and 4 show a photograph and circuit diagram of the amplifier. The input, output and interstage networks, except the first and third interstages, consist of low-pass type stripline structures which transform impedance and, at the same time, peak up the gain at the high frequency edge. The first and third interstages have bandpass type structures which suppress low frequency gain to prevent instability. The series combinations of a resistor and a parallel tuned circuit at the fifth interstage and output stage provide resistive loading at low frequencies and prevent instability. The bias circuitry is almost the same as shown in Figure 1, and all *dc* voltages are obtained from a single *dc* source. The emitter currents of the first and second transistors are smaller than normal to improve noise performance.

The gain and the input and output *vswr* characteristics versus frequency are shown in Figure 5. The gain is almost flat at *32 db* over a *450-Mc* bandwidth, and the input and output *vswr* are less than *1.3* over a *350-Mc* band. The measured noise figure is *6.5 db* at *1.25 Gc* and increases up to *8.8 db* at *1.6 Gc* as shown in Figure 6. The output power level at which the gain is *1 db* less than the small signal gain is *+2 dbm*. The amplifier uses *6 v* × *30 ma* = *180 mw* of *dc* power.

Acknowledgment

The author wishes to express his sincere thanks to *A. E. Bakanowski* and *M. Uenohara* for their advice, *L. D. Gardner* for design of the printed circuit construction, *R. G. Voss* for design of the low-inductance transistor socket for printed circuit use, *A. G. Foyt* for his help in measuring transistor parameters and *J. P. Beccone* for his help during the course of the experiments.

* Work partly supported by the U. S. Army Materiel Command.

† Assistant Professor, University of Tokyo, Japan, on leave of absence since October, 1961.

‡ BTL L 2254.

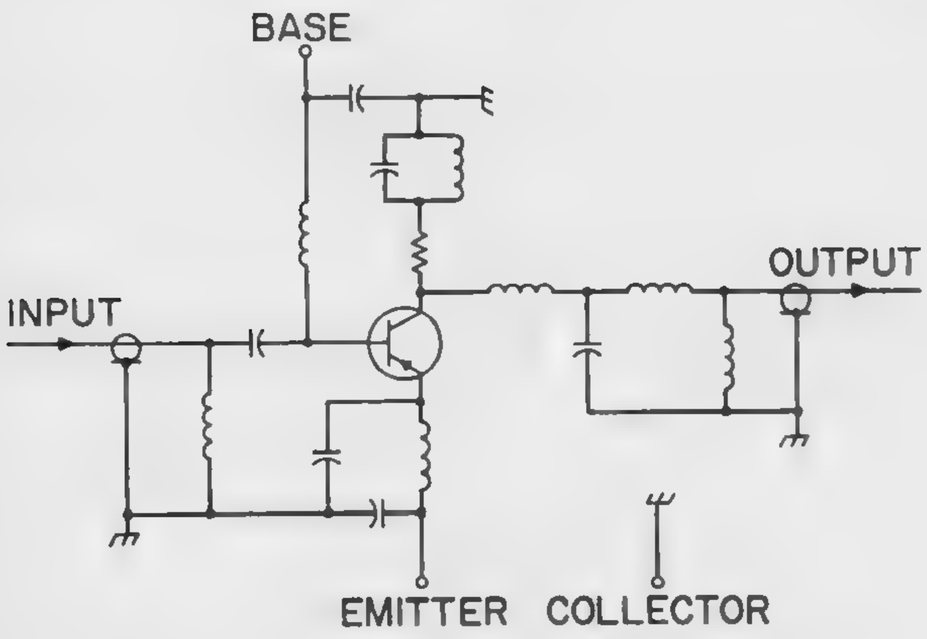


FIGURE 1—**Circuit diagram of a single-stage common-emitter amplifier.**

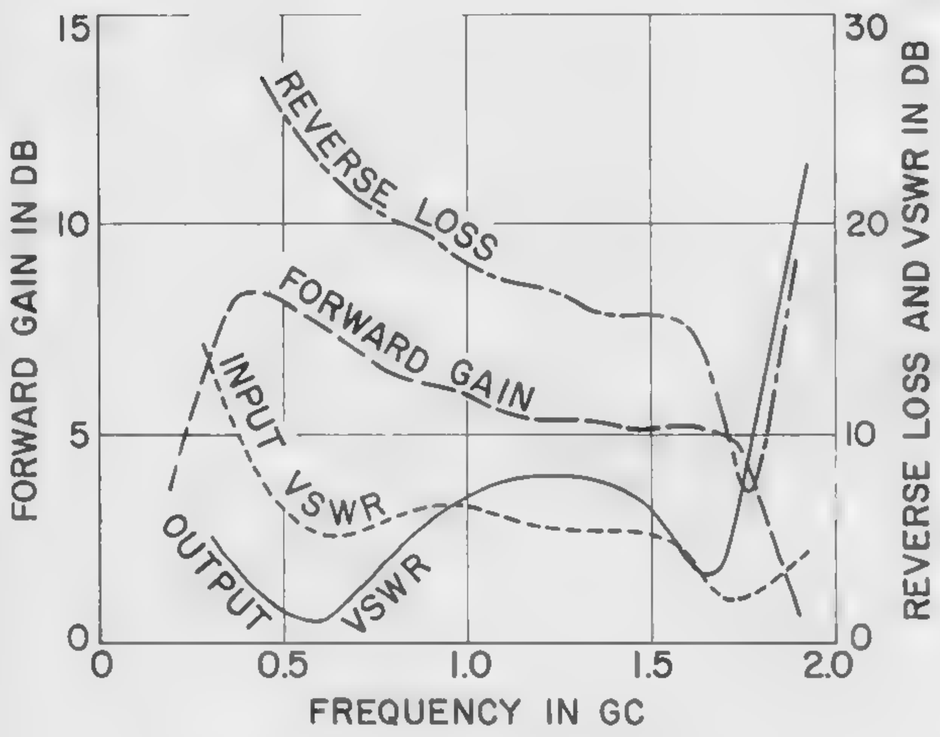


FIGURE 2—**Frequency characteristics of the single-stage common-emitter amplifier.**

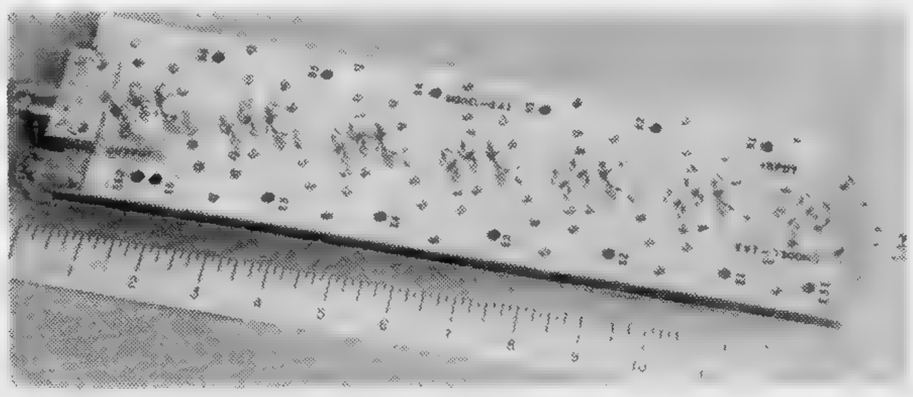


FIGURE 3—**Photograph of six-stage common-emitter amplifier. Outside dimensions are: *14.5"* x *3.4"* x *0.9".***

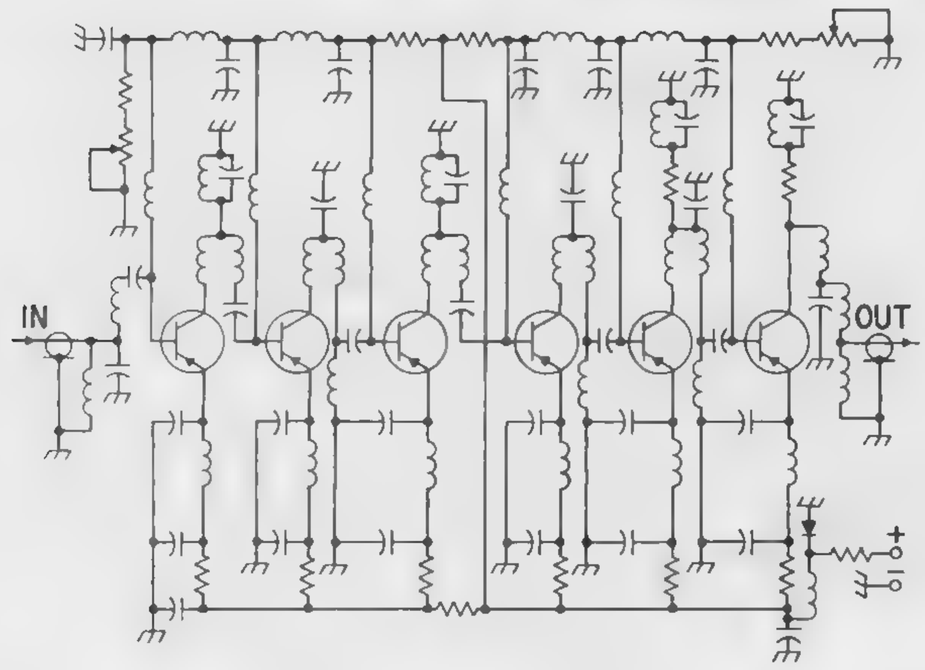


FIGURE 4—**Circuit diagram of six-stage common-emitter amplifier.**

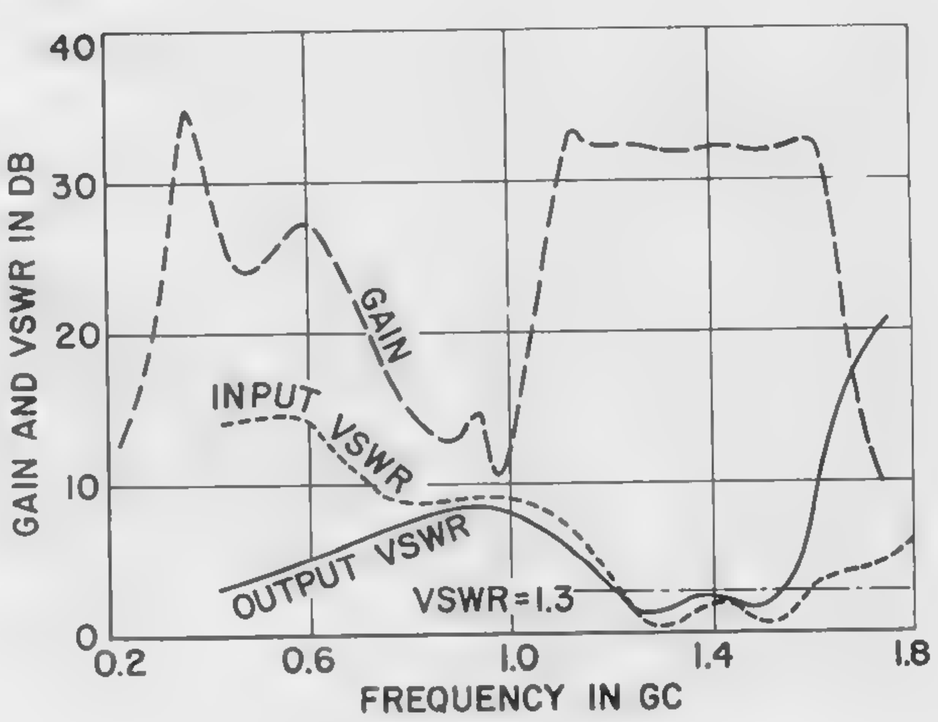


FIGURE 5—**Frequency characteristics of the common-emitter amplifier.**

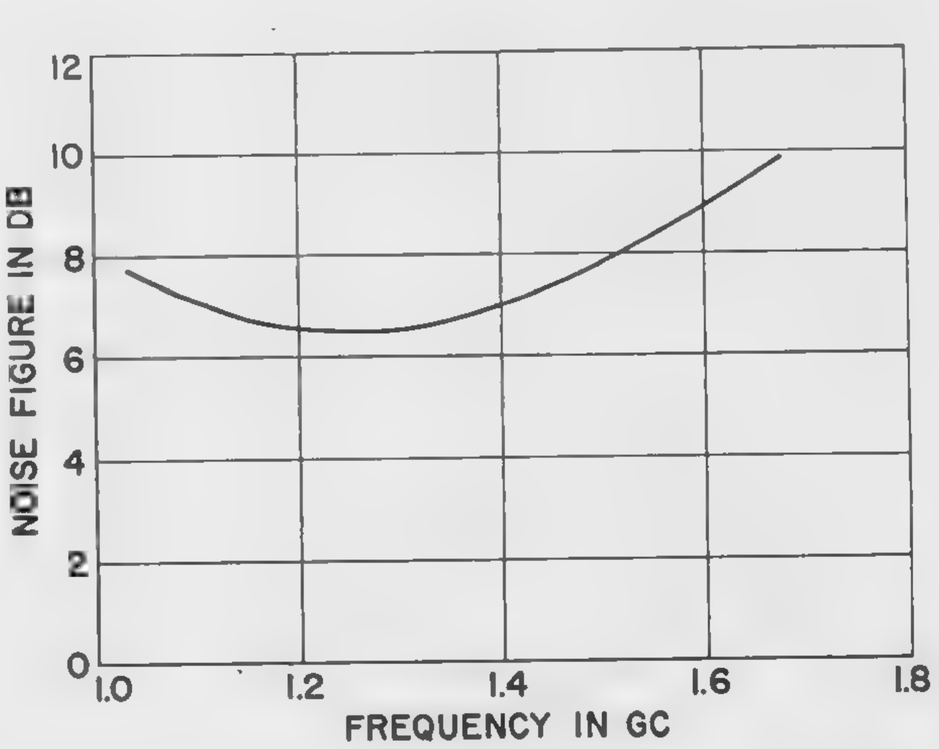


FIGURE 6—**Noise figure of the common-emitter amplifier.**

SESSION V: Microwave Circuits

THAM 5.2: A "Goodness' Criterion for Any Varactor Diode as a High-Order Frequency Multiplier

L. K. Staley

The Bendix Corporation

Towson, Md.

THEORY PREDICTS that a varactor pumped at some fundamental frequency can produce an output at any desired harmonic with *100%* efficiency. In practice, however, the conversion efficiency decreases very quickly with increasing harmonic number, due to the looseness of the coupling mechanism as illustrated by the decrease in the optimum resistances reflected to the input and output terminals of the circuit by the conversion process. The optimum input and output resistances can be increased beyond the value for direct conversion by allowing idler currents to exist at selected intermediate harmonic frequencies, but not allowing real power to flow at these intermediate frequencies, thereby increasing conversion efficiencies.

Earlier analyses‡ have approached this problem using two different techniques, but the end results have been in fair agreement. The former approach is the technique which will be probed here to derive the design equations needed to define a *goodness* for a particular varactor for a given multiplication. In this analysis flow graphs are drawn for the various multiplying and mixing processes involved and conversion resistances are identified with each process. However, only those frequencies which are terminated in real loads can deliver real power.

The resistances involved have been derived in an analysis by the author. The input and output resistances of a two frequency device can be expressed as

$$R_{in} = R_{out} = R_s \sqrt{1 + (k_1 Q_1)^2}$$

where:

R_s is the spreading resistance of the varactor
$k_1 = \frac{C_o}{C}$ is the modulation factor at the input frequency
C is the effective dynamic capacity
C_o is the static capacity at the *dc* bias point (half-charge point)
Q_1 is the figure of merit at the *dc* bias point and input frequency

This expression is the same as that derived for a parametric up-converter in a similar analysis, except for the frequency terms contained within Q_1. Therefore, this same expression with modification by the addition of frequency ratios can be useful for either multiplying or mixing processes.

The only remaining problem is to determine k_1 for each process. For doubling or mixing at the fundamental frequency, we have the following expression:

$$k_1 = \frac{1}{\frac{(\phi - V_o)}{\Gamma(V_1/2)} - \frac{2\Gamma(V_1/2)}{(\phi - V_o)}}$$

when C is given by

$$C = C_o(\phi - V_o)^{-\Gamma}$$

The ratio k_1 is easily evaluated when the applied voltages are known.

The maximum value for k_1 occurs when $(\phi - V_o) = V_1$ where V_1 is the one-half total charge voltage. For each frequency of interest,

$$k_n = \frac{1}{\frac{(\phi - V_o)}{\Gamma(V_1/2n)} - \frac{\Gamma(V_1/n)}{(\phi - V_o)}}$$

where k_n is now the modulation factor for the frequency n. For $V_1 = (\varphi - V_o)$, where V_o is the one-half maximum charge voltage, then

$$k_n = \frac{\Gamma n}{2n^2 - \Gamma^2}$$

Evaluation of these maximum values for k_n are given for $\Gamma = 0.5$, 0.4 and 0.33 in Figure 1.

Construction of a flow graph for the desired multiplier then permits expressions to be written for the input and output resistances of any type of multiplier involving multiplying or multiplying and mixing processes. Typical expressions for triplers, quadruplers and quintuplers appear in Figure 2. With these resistances efficiencies can now be calculated as outlined in Figures 3 and 4. The effect of variations in Γ are shown for triplers and quintuplers in Figures 5 and 6. For comparison, the results of the MIT analysis are shown as dotted lines.

Using these *goodness* criteria, multipliers have been constructed, and excellent correlation has been achieved. For a typical quintupler the measured efficiency was *52.4%* after subtracting circuit losses, agreeing with calculations within 2.2%. The output frequency of this multiplier was *1830 Mc.* A schematic of the device is shown in Figure 7.

k_n			
n	Γ=0.5	Γ=0.4	Γ=0.33
1	.286	.208	.177
2	.129	.102	.085
3	.085	.067	.056
4	.063	.050	.042
5	.050	.040	.034
6	.042	.033	.028

FIGURE 1—Maximum values for the modulation factor k_n.

‡ Columbia and MIT projects.

[1] Leeson, D. B., and Weinreb, S., "Frequency Multiplication With Nonlinear Capacitors," Proc. of IRE; Dec., 1959.

[2] Utsunomiya, T., and Yuan, S., "Theory, Design and Performance of Maximum Efficiency Variable Reactance Frequency Multipliers," *Columbia University Electronics Research Laboratories Technical Report* T-1/64; June, 1960.

[3] Penfield, P., and Rafuse, R., "Varactor Applications," *MIT Press;* 1962.

[4] Staley, L. K., "Design of a High Performance S-Band Varactor Frequency Multiplier," *NEC Proc.;* 1962.

MULTIPLICATION	R_{in}/R_s	R_{out}/R_s
TRIPLER (1, 2, 3)	$\sqrt{1+(k_1Q_1)^2}$ + $\sqrt{1+\frac{1}{3}(k_3Q_1)^2}$	$\sqrt{1+\frac{1}{6}(k_1Q_1)^2}$ + $\sqrt{1+\frac{1}{3}(k_3Q_1)^2}$
QUADRUPLER (1, 2, 4)	$\sqrt{1+(k_1Q_1)^2}$	$\sqrt{1+\frac{1}{4}(k_2Q_1)^2}$
QUINTUPLER (1, 2, 4, 5)	$\sqrt{1+(k_1Q_1)^2}$ + $\sqrt{1+\frac{1}{5}(k_5Q_1)^2}$	$\sqrt{1+\frac{1}{20}(k_1Q_1)^2}$ + $\sqrt{1+\frac{1}{5}(k_5Q_1)^2}$

FIGURE 2—Series equivalent resistance ratios for the input and output to harmonic multipliers.

DOUBLER (1,2)

$$\epsilon = n_1 n_2$$

$$n_1 = n_2 = \frac{R_{12}}{R_{12}+R_S}$$

QUADRUPLER (1,2,4)

$$\epsilon = n_1 n_2 n_4$$

$$n_1 = \frac{R_{12}}{R_{12}+R_S} = \frac{R_{in}}{R_{in}+R_S}$$

$$n_2 = \left(\frac{R_{12}}{R_{12}+R_S}\right)\left(\frac{R_{24}}{R_{24}+R_S}\right)$$

$$n_4 = \frac{R_{24}}{R_{24}+R_S} = \frac{R_{out}}{R_{out}+R_S}$$

TRIPLER (1,2,3)

$$\epsilon = \frac{3 n_1 n_2 n_3}{2+n_2}$$

$$n_1 = \frac{R_{12}+R_{13}}{R_{12}+R_{13}+R_S} = \frac{R_{in}}{R_{in}+R_S}$$

$$n_2 = \left(\frac{R_{12}}{R_{12}+R_S}\right)\left(\frac{R_{23}}{R_{23}+R_S}\right)$$

$$n_3 = \frac{R_{13}+R_{23}}{R_{13}+R_{23}+R_S} = \frac{R_{out}}{R_{out}+R_S}$$

FIGURE 3—Expressions for the loop and total efficiencies of doublers, triplers and quadruplers.

QUINTUPLER (1,2,4,5)

$$\epsilon = \frac{5 n_1 n_2 n_4 n_5}{4+n_2 n_4}$$

$$n_1 = \frac{R_{12}+R_{15}}{R_{12}+R_{15}+R_S} = \frac{R_{in}}{R_{in}+R_S}$$

$$n_2 = \left(\frac{R_{12}}{R_{12}+R_S}\right)\left(\frac{R_{24}}{R_{24}+R_S}\right)$$

$$n_4 = \left(\frac{R_{24}}{R_{24}+R_S}\right)\left(\frac{R_{45}}{R_{45}+R_S}\right)$$

$$n_5 = \frac{R_{15}+R_{45}}{R_{15}+R_{45}+R_S} = \frac{R_{out}}{R_{out}+R_S}$$

FIGURE 4—Expressions for the loop and total efficiencies of quintuplers.

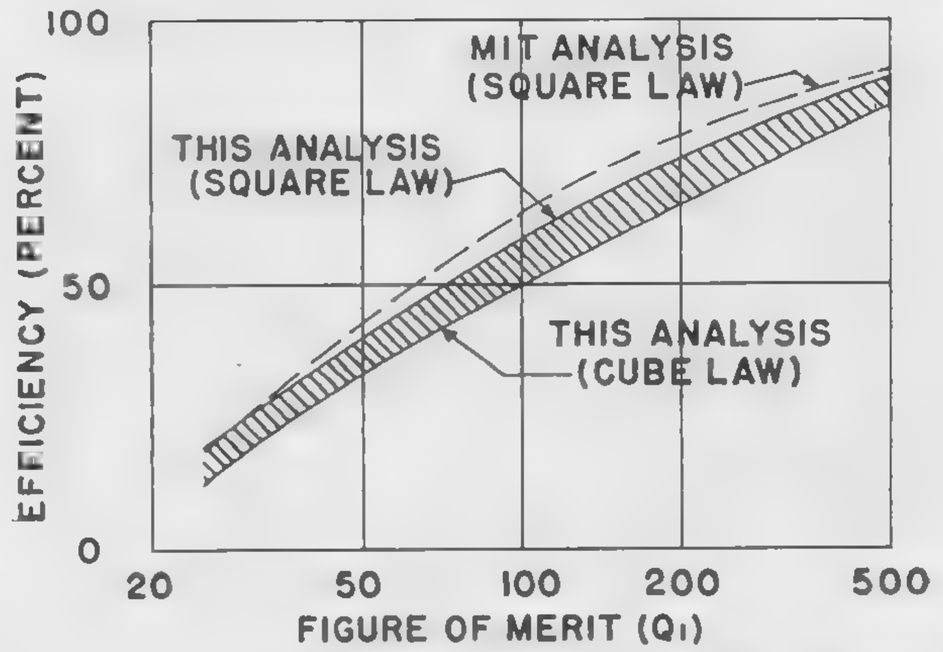


FIGURE 6—Maximum efficiency limits for any varactor as a *1, 2, 4, 5,* quintupler; hatched area represents the extremes in non-linearity of currently available varactors.

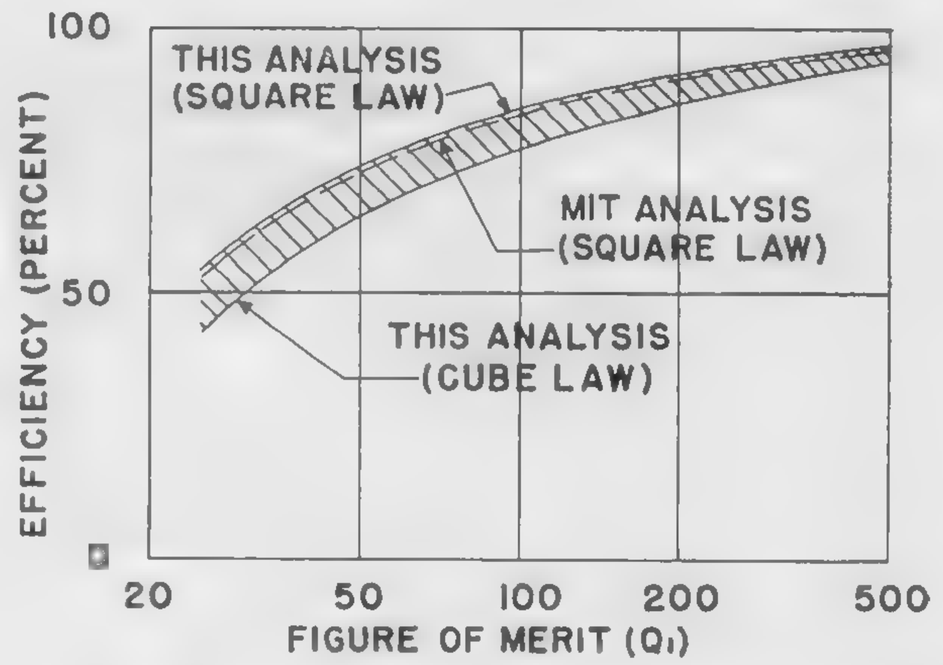


FIGURE 5—Maximum efficiency limits for any varactor as a *1, 2, 3* tripler; hatched area represents the extremes in non-linearity of currently available varactors.

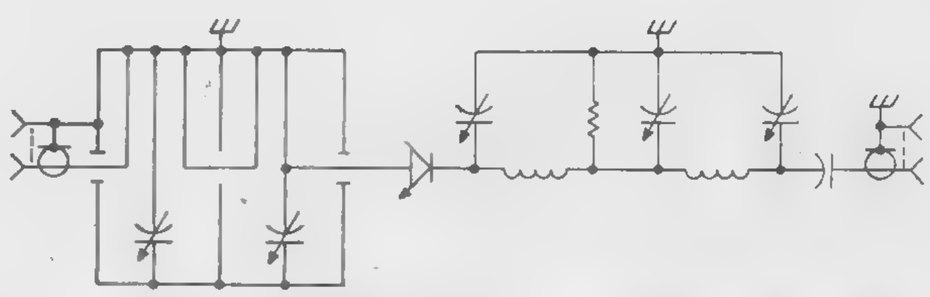


FIGURE 7—Schematic of an experimental quintupler.

SESSION V: Microwave Circuits

THAM 5.3: Operating Characteristics and Design Criteria of an All Solid-State 13.3-Gc 50-mw Microwave Source*

L. D. Baldwin, F. P. Collins, S. L. Johnson, W. Priest

Microwave Associates, Inc.

Burlington, Mass.

IT HAS RECENTLY become possible to construct solid-state microwave sources consisting of a multiplier chain excited by transistor driver, capable of generating significant amounts of microwave power.

Multiplier Design[1, 2]

One type of frequency multiplier circuit which has been used with good success up to *L*-band (Figure 1) uses lumped-circuit elements and contains bandpass filters for frequency separation. The varactor is connected in shunt and is operated self-biased. With shunt mounting the chassis can be used as an effective heat sink for one end of the varactor. In the higher order, multipliers (x 3, x 4, etc.) it has been found necessary to use idlers[3] to achieve efficient operation.

Some typical circuits which have been used for the higher frequencies above *L*-band (Figure 7) use distributed circuit techniques. Here, also, the varactor is connected in shunt.

For the successful chain operation, the individual stages have to be designed to be compatible in bandwidth, impedance level and operating power level. To accomplish these objectives the parameters of the varactors (such as breakdown voltage, cutoff frequency, capacitance at zero bias) have to be chosen carefully.

Parametric oscillations of various kinds are possible when a strongly pumped varactor is imbedded in a circuit containing many reactive elements. The conditions for oscillation, it is believed, can be predicted from parametric amplifier theory. In the case of a multiplier containing a number of resonant circuits, the problem is complex and is not in general amenable to simple analysis.

As predicted by parametric-amplifier theory, oscillations can occur if the circuit has a sufficiently high resistive impedance at two frequencies whose sum is the drive frequency or a harmonic of the drive frequency. Such impedances may be found when the circuit is resonant at these frequencies. In the circuit shown in Figure 1, oscillations can occur when the input or output double-tuned circuit is not properly tuned.

In many instances a multiplier stage, which is stable when connected to a resistive source and load, will become unstable when connected in the chain. These instabilities can be explained by examining the impedances presented to the intermediate stage outside the operating band. The preceding and following stages are usually mismatched in this region and can present impedances of the correct character to cause oscillation. The interstage coupling networks should be so designed that the intermediate stage is decoupled outside the operating band. For narrow-band chains it is usually possible to design the stages and the coupling networks so that stable operation can be achieved without resorting to the use of ferrite isolators between stages. In chains having appreciable bandwidth (*10%* or more), it has been found expedient to use isolators between stages; Figure 4.

At some levels of input drive and frequency, two possible stable operating modes of a multiplier are possible[4]. One mode is characterized by a low power output and the other by a high power output. The presence of this condition in the stages can give rise to chain *starting* problems. The use of a resistor in shunt with the varactor has been found helpful in reducing the effects of dynamic detuning in the case of self-bias operation.

The use of interstage filters is particularly important for the suppression of spurious harmonics in chains. Figure 2 shows the type of spectrum which is generated by a simple nonlinear element, such as a varactor, which is driven strongly by a signal contaminated with a weak signal of another frequency. In a frequency multiplier, analysis shows that the undesired signal will be enhanced, relative to the desired output signal, the effect increasing with the multiplication ratio; Figure 3. For a high order of multiplication, suppression of the $n-1$ and $n+1$ harmonics of the fundamental requires a higher degree of filtering between the lower frequency stages than between the higher frequency stages.

The multiplier chain of the solid-state source contains two triplers and two quadruplers and is driven by *5 w* at *92.5 Mc*; Figure 6. The transistor driver consists of a crystal oscillator followed by three stages of amplification. The chain is designed to provide better than *40 db* of undesired harmonic suppression and has a *3-db* output bandwidth of *130 Mc*. The individual stages are operated in saturation to provide stable power output over an extended temperature range.

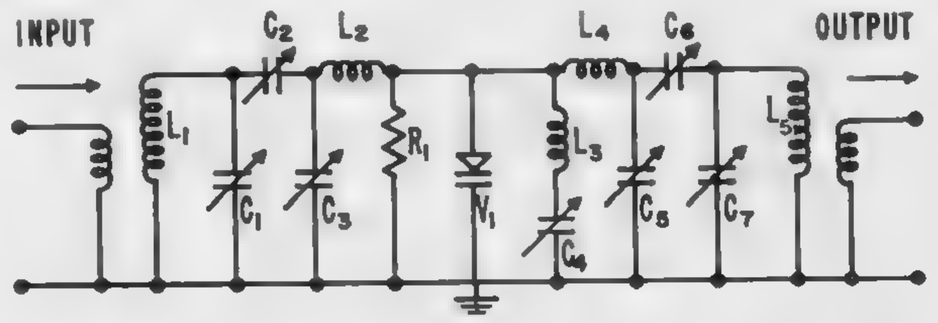


***FIGURE 1*—Typical circuit for *2 X*, *3 X*, and *4 X* multipliers, circuit consisting of a double-tuned filter tuned to input frequency (L_1C_1 *and* $L_2C_3V_1$ coupled through C_2); second filter tuned to output frequency ($L_4C_4V_1$ and L_5C_7 coupled through C_6); and an idler circuit (not required in *2 X*) tuned to second harmonic.**

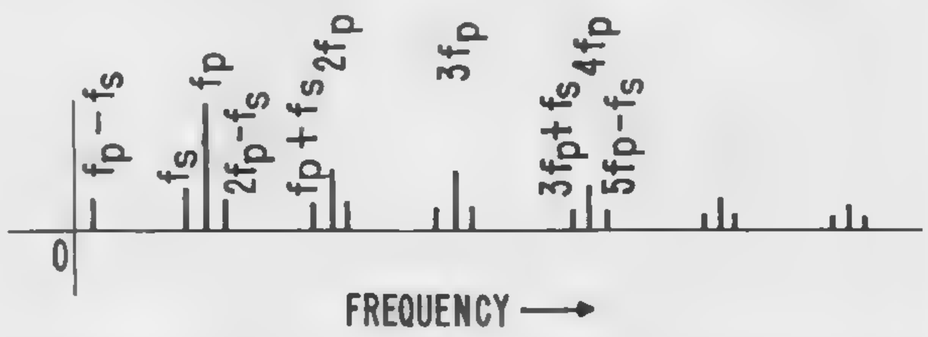


***FIGURE 2*—First-order spectrum of a general nonlinear device driven by two frequencies.**

* This work was supported in part by Wright Patterson Air Force Base under U.S.A.F. Contract No. AF33(616)-8117.

[1] Panfield, Jr., P., and Rafuse, R. P., "Varactor Applications," *MIT Press*, Chapter 8; 1962.

[2] Leeson, D. B., and Weinreb, S., "Frequency Multiplication with Nonlinear Capacitors—A Circuit Analysis," *Proc. IRE*, p. 2076-2084; Dec., 1960.

[3] Diamond, B. L., "Idler Circuits in Varactor Frequency Multipliers," *MIT Lincoln Laboratory Report No.* 47G-0012; Dec., 1960.

[4] McDade, J. C., "Jump Phenomena in Varactor Diode Circuits," *Diamond Ordnance Fuze Laboratories Report TR*-1008; Jan., 1962.

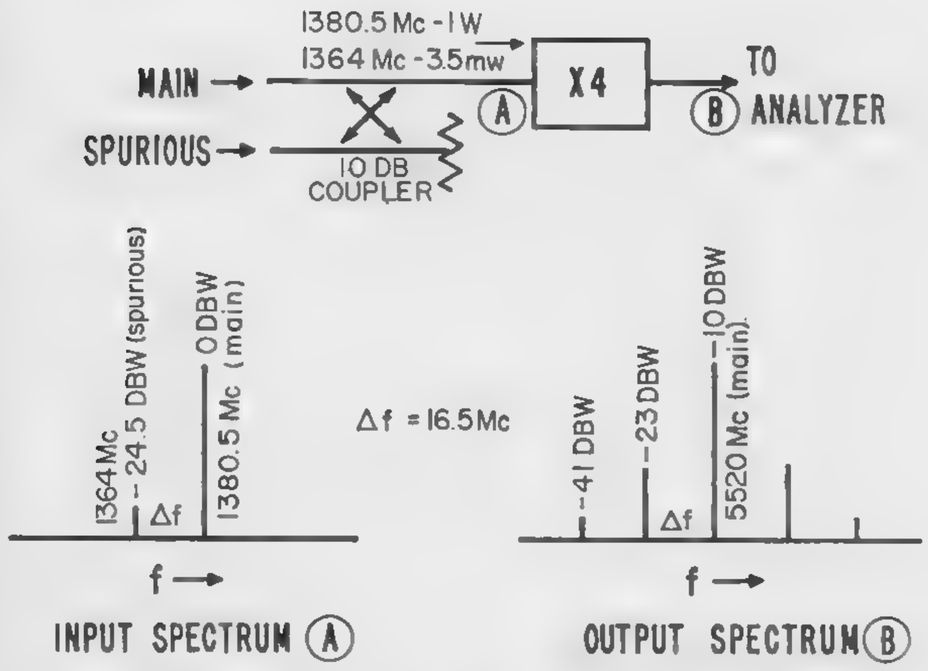


FIGURE 3—Measured spurious signal enhancement in a *1.4 Gc* to *5.6 Gc 5%* bandwidth quadrupler: *(A)* shows input spectrum; *(B)* output spectrum. In passing through multiplier, spurious signal is amplified *11.5 db* relative to main signal.

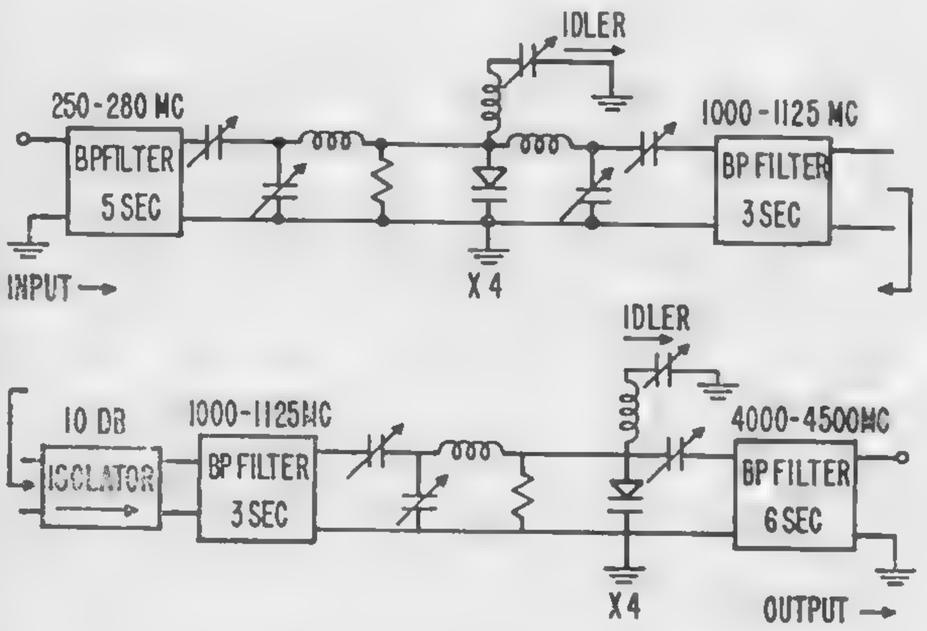


FIGURE 4—Schematic of *11%* bandwidth chain with *16 X* multiplication ratio: chain consists of two quadruplers and covers the *250-280 Mc* band (input); chain has *60-db* suppression of undesired harmonics and uses an isolator between stages.

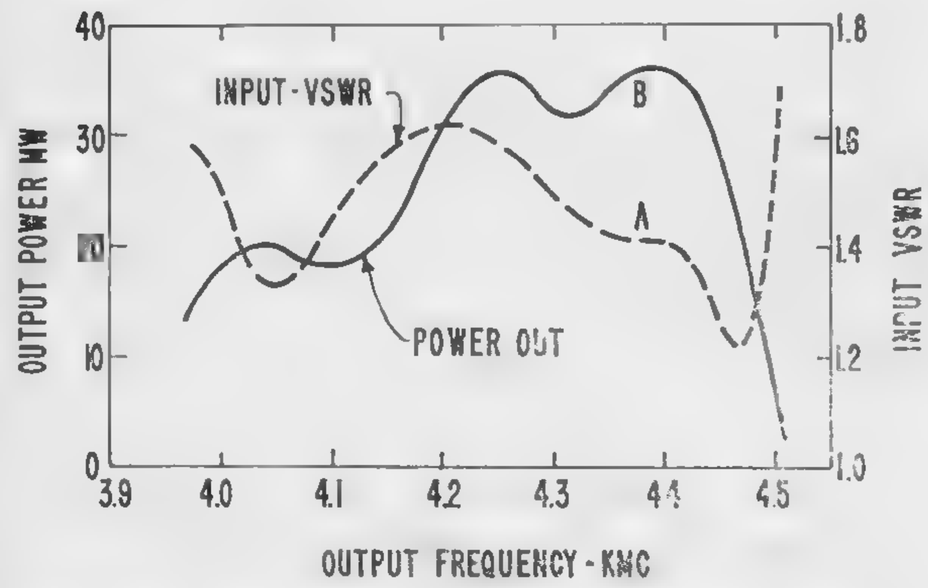


FIGURE 5—Performances of *11%* bandwidth chain of Figure 4: *(A)* input *vswr* versus output frequency; *(B)* output power versus output frequency. Drive level is constant at *0.5 w*.

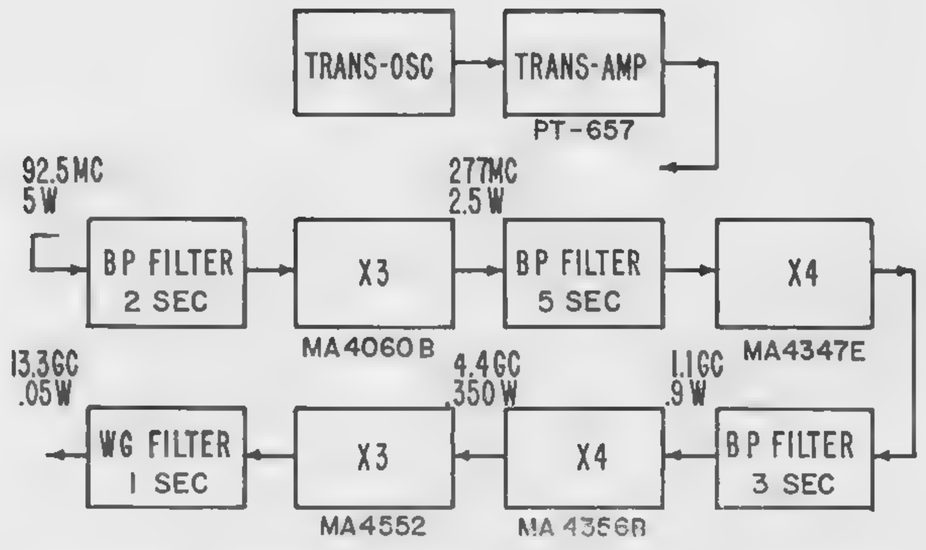


FIGURE 5—Block diagram of *13.3-Gc* solid-state source.

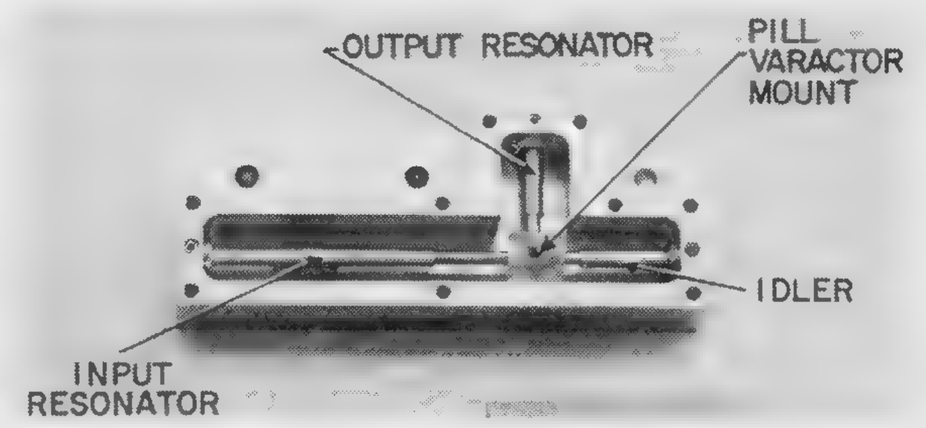


FIGURE 7—Photo showing construction of *1.1* to *1.4-Gc* quadrupler.

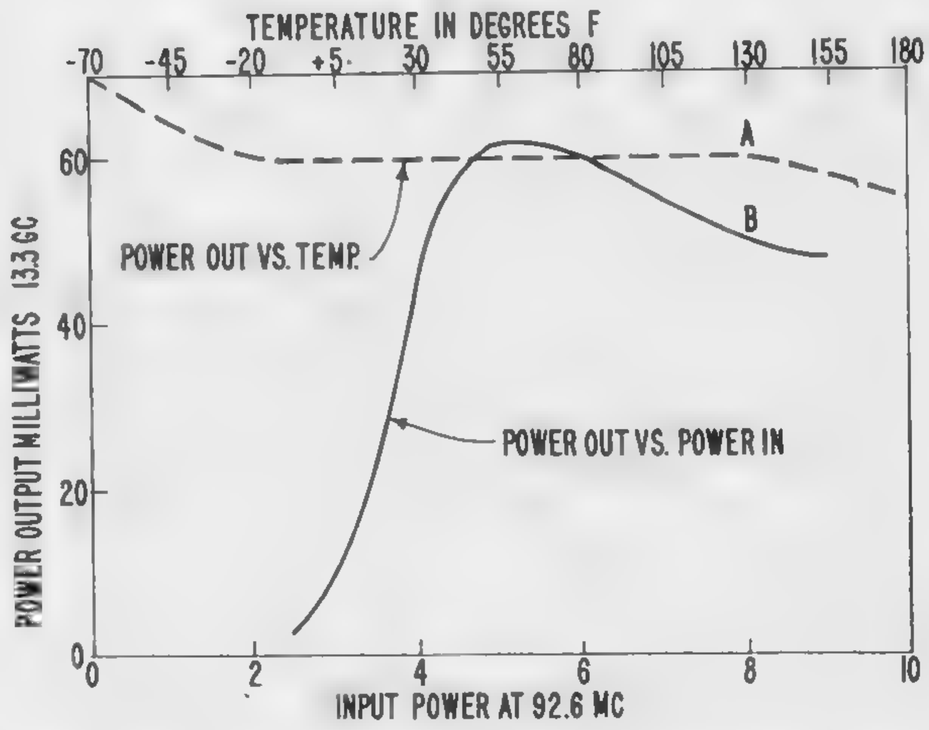


FIGURE 8—Performance of *13.3-Gc* multiplier chain: *(A)* output power versus temperature with fixed input power of *5 w*; *(B)* output power versus input power.

SESSION V: Microwave Circuits

THAM 5.4: Low-Noise Nonreciprocal Parametric Amplifier with Power Matching at the Input and Output

R. Maurer and K-H. Locherer

Telefunken G.m.b.H.

Ulm (Donau), Germany

THE NONRECIPROCAL effects of isolators and circulators can be produced by means of a two-stage parametric amplifier[1-7]. By pumping the diodes in phase quadrature, and delaying the signal by a quarter wavelength between the first and second diode, signal power is transmitted in the forward direction with considerable gain, whereas signals in the reverse direction are transmitted without amplification. This results because the currents at the idler frequency are combined in phase for signals in the forward direction, and out of phase for signals transmitted in the reverse direction[5-7]. Moreover, backward transducer gains can be reduced to zero by adding a passive feedback network[2-4]. Instead of two parametric diodes, two conductances with nonlinear characteristics, or one conductance and one susceptance with nonlinear characteristics, may be used to obtain nonreciprocal transmission properties[2-4, 8].

This paper will report on a nonreciprocal parametric amplifier constructed with two parametric diodes as the active components. This amplifier theoretically fulfills the following requirements: transducer forward gain $\vec{G}_t > 1$, transducer backward gain $\overleftarrow{G}_t = 0$, matched input and output circuits; and noise figure $NF < 3db$.

The amplifier (Figure 2) consisting of two parametric converters M_1 and M_2, in cascade, acts as a nonreciprocal four-terminal network $(1'; 1')$-$(2'; 2')$ because the diodes are fed with out-of-phase pump voltages U_{b1}, U_{b2}, of frequency $f_b = \frac{b}{2\pi}$. According to *A. K. Kamal*[1], phase nonreciprocity functions in the following way. The upper sideband $f_b + f_s$ (f_s = signal frequency) generated by the converter M_1 has a phase angle $\phi_{b1} + \phi_{s1}$, where ϕ_{s1} is the phase angle associated with the signal and ϕ_{b1} is the angle associated with the pump voltage U_{b1}. According to the equation $(f_b + f_s) - f_b = f_s$, the second converter M_2 converts the upper sideband back to the signal frequency with a phase angle $(\phi_{b1} + \phi_{s1}) - \phi_{b2} = (\phi_{b1} - \phi_{b2}) + \phi_{s1}$. Considering the transmission in the opposite direction from right to left we will get the *output* signal frequency at a phase angle of $(\phi_{b2} + \phi_{s2}) - \phi_{b1} = -(\phi_{b1} - \phi_{b2}) + \phi_{s2}$ which demonstrates the phase nonreciprocity due to the phase shift $\phi_{b1} - \phi_{b2}$. A similar argument is valid for the lower sideband f_b-f_s.

By means of a passive feedback admittance Y nonreciprocity, with respect to the absolute value, can be achieved additionally. According to theory, with $\phi_{b1} - \phi_{b2} = -\frac{\pi}{2}$ the network *(1; 1)-(2; 2)* can be made unilateral at resonance by means of a feedback network consisting of a simple capacitor. The input and output signal circuits (admittances Y_1 and Y_2) are tuned to the average signal frequency $f_s = \frac{\Omega_1}{2\pi}$. The idler circuit (admittance Y_1) is tuned to $f_b + f_s = \frac{b + \Omega_1}{2\pi}$ (upper sideband) and also to $f_b - f_s = \frac{b + \Omega_1}{2\pi}$ (lower sideband)[10, 6, 9, 11]. Power matching at the input and output, and forward transducer gains greater than unity are thereby made possible. If the upper (lower) sideband is suppressed, matching is impossible (possible); and the forward transducer gain is larger than unity (at best equal to unity).

When the signal and idler circuits are tuned to resonance, the transducer forward gain under matched conditions, neglecting the losses due to g_{c1} and g_{c2}, equals $\vec{G}_t$ as given in Figure 1, while $\overleftarrow{G}_t = O$. The quantities $(g_c)_{b+\Omega_1}$ and $(g_c)_{b-\Omega_1}$ are the conductances of the idler circuit at the resonant angular frequencies $b + \Omega_1$ and $b - \Omega_1$. Suppressing the idler resonance at $b - \Omega_1$ means that

$$(g_c)_{b-\Omega_1} = \infty$$

and $a = 0$. Then equation *(1)* yields $\vec{G}_t = 1$; the device acts as an isolator. The excess noise figure of the device under matched conditions, neglecting g_{c1}, g_{c2}, equals F_{ex}, also cited in Figure 1. F_{ex} increases monotonically with a. For isolator operation $(a = 0)$, $F_{ex} = 0$. For amplifier operation $(0 < a < 1)$, $F_{ex} < 1$, if a is not too large. This good noise performance is due to proper transformation of the idler noise within the converter cascade.

Figure 3 shows the equivalent-circuit-diagram of the test setup. The phase angles and the absolute values of the pump voltages feeding D_1 and D_2 are regulated by the narrow-band resonance circuit tuned to b at the amplifier input. The inductance in the signal circuit is tapped at P, the point of minimum pump voltage. The beating oscillator is connected to the series-resonant circuit branch of the idler circuit. This series arm is

[Continued on page 119]

---

[1] Kamal, A. K., "A Parametric Device as a Nonreciprocal Element," *Proc. IRE*, p. 1424-1430; August, 1960.

[2] Maurer, R., and Löcherer, K.-H., Nichtreziproke Verstärker-Anordnung, Deutches Bundes Patent, 1,112,140; Nov. 22, 1960.

[3] Maurer, R., and Löcherer, K.-H., "Theorie Nichtreziproker Schaltungen mit Gleicher Eingangs- und Ausgangsfrequenz unter Verwendung nichtlinearer Halbleiterelemente," *Archiv der Elektrischen Ubertrangung*, p. 71-73; Feb., 1961.

[4] Löcherer, K.-H., and Maurer, R., "Dispositifs Non-Réciproques à Diodes Paramétriques et a Diodes Tunnel," *L'Onde Electrique*, p. 381-385; April, 1960. Also "Nonreciprocal Reactance and Tunnel Diodes Circuits," *Electronics*, p. 21; March, 1961.

[5] Baldwin, L. D., "Nonreciprocal Parametric Amplifier Circuits," *Proc. IRE*, p. 1075; June, 1961.

[6] Korpel, A., and Desmares, P., "Experiments with Nonreciprocal Parametric Devices," *Proc. IRE*, p. 1582; October, 1961.

[7] Thompson, G. H. B., "Unidirectional Lower Sideband Parametric Amplifier Without Circulator," *Proc. IRE*, p. 1684-1685; Nov., 1961.

[8] Löcherer, K.-H., and Maurer, R., "Nichtreziproke Verstärkerschaltung, *Deutches Bundes Patent;* Nov. 22, 1960.

[9] Engelbrecht, R. S., "Parametric Energy Conversion by Nonlinear Admittances," *Proc. IRE*, p. 312-321; March, 1962.

[10] Maurer, R., and Bomhardt, K., Nichtreziproke Reaktanz-Verstärkeranordnung, Deutches Bundes Patent 1,120,525; March 24, 1961.

[11] Maurer, R., and Löcherer, K.-H., "Nichtreziproke Reaktanz- und Tunneldioden-Schaltungen," *Archiv der Elektrischen* Ubertragung; to be published.

TRANSDUCER GAIN

FORWARD BACKWARD

$$\rightarrow G_t = \left[\frac{1+a}{1-a}\right]^2 \geq 1, \quad \leftarrow G_t = 0, \quad a = \frac{b-\Omega_1}{b+\Omega_1} \cdot \frac{(g_c)_{b+\Omega_1}}{(g_c)_{b-\Omega_1}}$$

EXCESS NOISE FIGURE

$$F_{ex} = \frac{4\Omega_1}{b-\Omega_1} \cdot a \cdot \frac{1+\frac{b-\Omega_1}{b+\Omega_1} \cdot a}{(1-a)\cdot(1+a)^2}$$

***FIGURE 1*—Equations analyzing theory of cascade converter.**

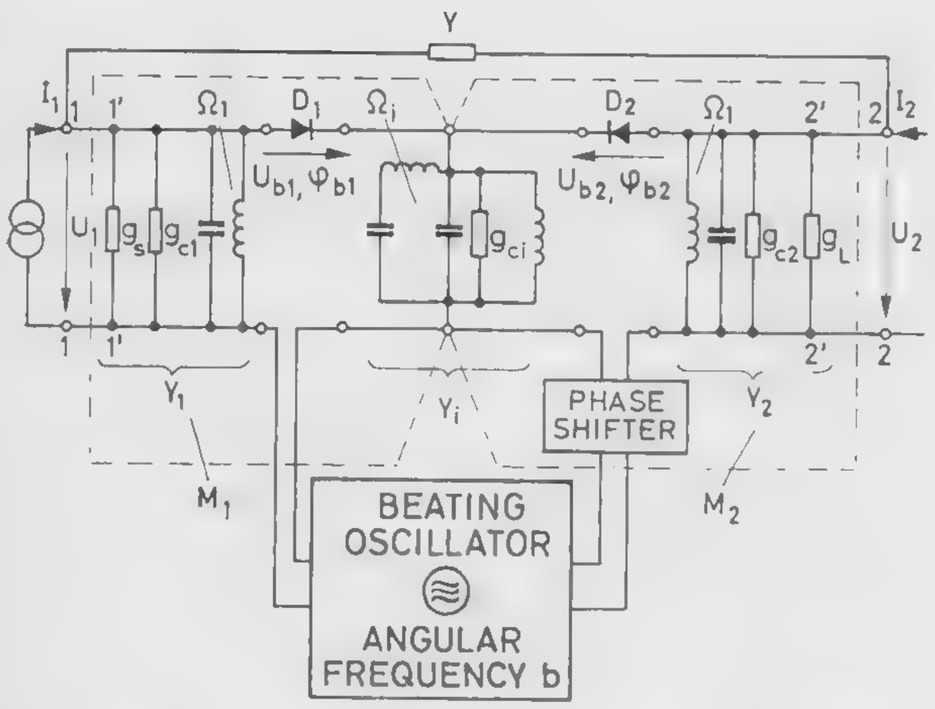


***FIGURE 2*—Schematic diagram of converter cascade with external feedback.**

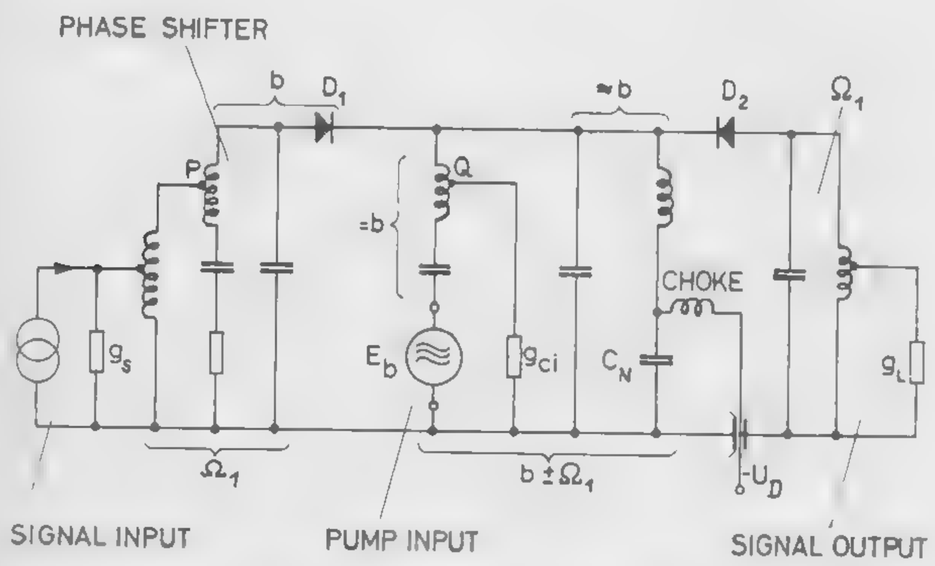


***FIGURE 3*—Equivalent-circuit diagram of test-setup.**

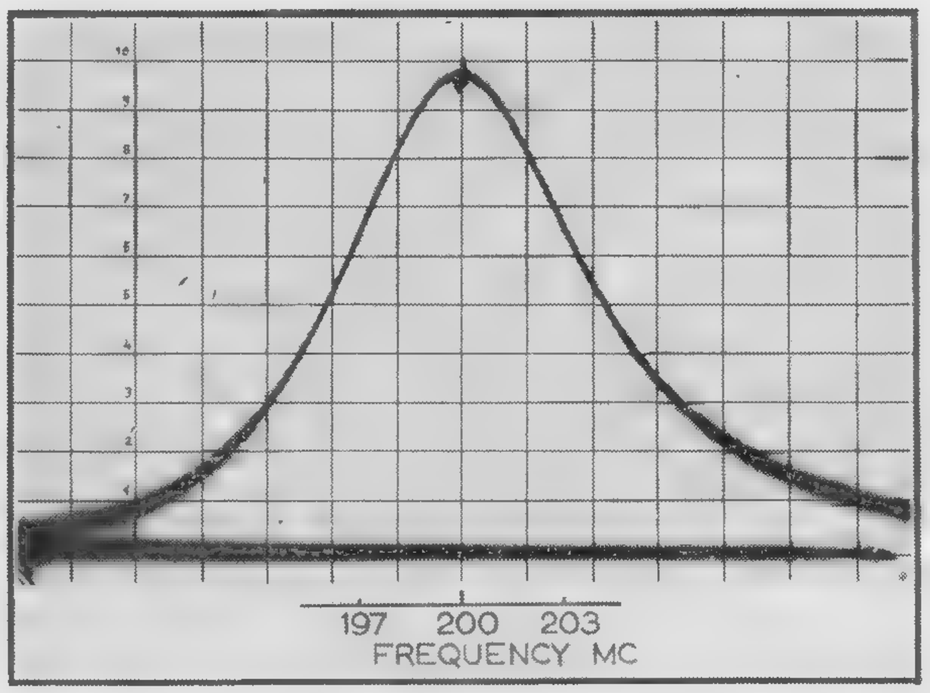


***FIGURE 4*—Forward transducer gain $\vec{G}_t$ versus frequency ($a = 0.5$). $\vec{G}_t = 8$ *db*, $NF = 2.55$ *db* at $\frac{\Omega 1}{2\pi} = 200$ *Mc*; total bandwidth $B_{total} = 6$ *Mc*.**

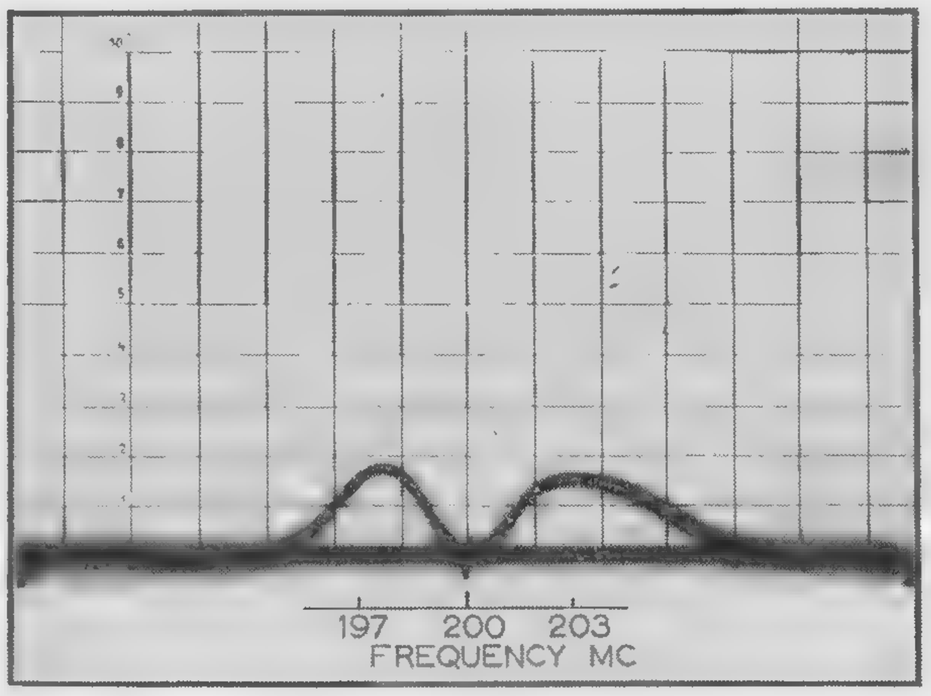


***FIGURE 5*—Backward transducer gain $\overleftarrow{G}_t$ versus frequency ($a = 0.5$). $\overleftarrow{G}_t \leq -40$ *db*, $NF = 2.55$ *db* at $\frac{\Omega 1}{2\pi} = 200$ *Mc*; $\overleftarrow{G}_t = -28$ *db at* band edges *197 Mc* and *203 Mc*.**

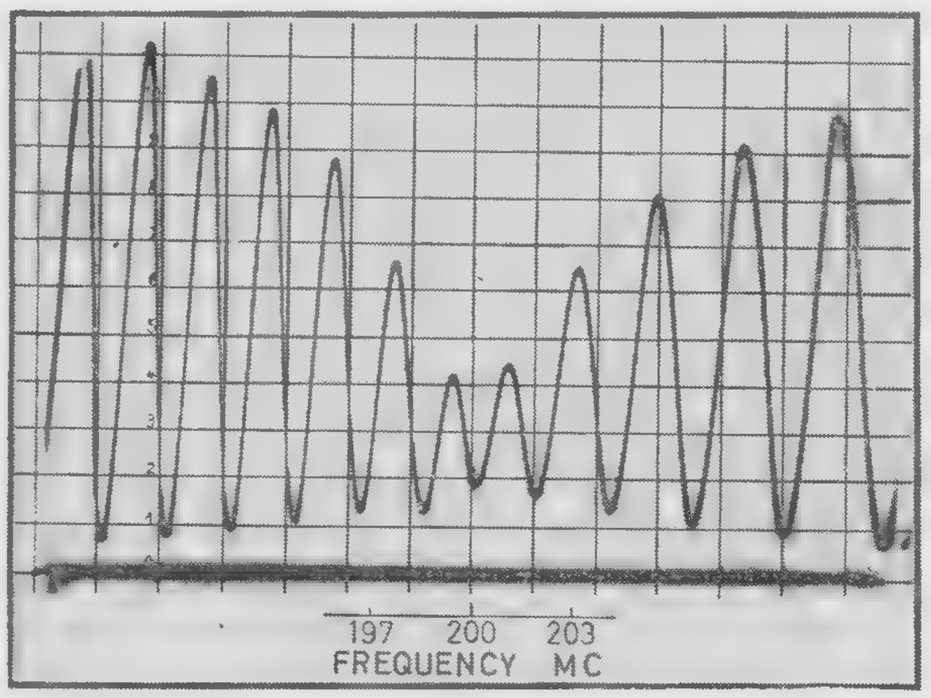


***FIGURE 6*—Input standing-wave-ratio m_{in} versus frequency ($a = 0.5$). $m_{in} = 1.35$ *at* $\frac{\Omega 1}{2\pi} = 200$ *Mc*.**

SESSION V: Microwave Circuits

THAM 5.5: Varactor-Diode Amplifier at Liquid Helium Temperature

D. C. Hanson, H. J. Fink and M. Uenohara

Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

PREVIOUS EXPERIMENTS with parametric amplifiers [1,2] have indicated that the effective input noise temperature can be substantially reduced by refrigerating the amplifier down to liquid nitrogen temperature. It was also found that the noise temperature or the amplifier with a gallium-arsenide diode decreased almost linearly as the amplifier temperature was lowered from room temperature to *40°K* [3]. Our recent investigations of the junction capacitance of gallium-arsenide diodes have shown that the change in junction capacitance from liquid nitrogen temperature to liquid helium temperature is much smaller than that from room temperature to liquid nitrogen temperature; similar results have also been obtained with some epitaxial silicon diodes. It has also been found that the dynamic quality factor $\tilde{Q}$ of gallium-arsenide diodes improves continuously down to liquid helium temperature. *Blake* and others at MIT Lincoln Laboratory have recently measured *10°K* excess noise temperature for an *L*-band parametric amplifier operated at liquid helium temperature[4].

This paper will present the experimental results of a *4-Gc* parametric amplifier operated at liquid helium temperature.

The input impedance loci of the *4-Gc* amplifier with a gallium-arsenide diode are shown in Figure 1. The impedance has been measured at three different temperatures; i.e., *298°K*, *77°K* and *4.2°K*. All three impedance loci were measured at *4.17 Gc* with all circuit conditions maintained constant for the entire experiment. It will be noted that the resonant bias voltage shifted from *−1.25 v at 298°K* to *−0.94 v* at *77°K*, and to *−0.85 v* at*4.2°K*. The series resistance R_s also decreased as the temperature was lowered to liquid helium temperature as is shown by the increase in the *vswr* at the resonant point as the temperature is reduced.

The temperature variation of the junction capacitance of GaAs point-contact diodes has been directly measured at *1 Mc*. Figure 2 shows such a plot of junction capacitance (C_j) as a function of bias voltage. As in the impedance loci shown in Figure 1, wherein the largest shift in resonant bias voltage occurred between *298°K* and *77°K*, Figure 2 shows that the capacitance decreases more in this temperature range than from *77°K* to *4.2°K*.

Figure 3 shows a plot of $\left(\frac{1}{C_j}\right)^2$ as a function of bias voltage. If a point-contact junction is ideally characterized as an abrupt junction, the expression for the junction capacitance is

$$C_j = \frac{C_o}{(V-V_o)^{1/2}}$$

where V_o is the diffusion potential of the diode. It is apparent from Figure 3 that the GaAs point-contact diode follows closely this relationship at each temperature. The zero intercept of $\left(\frac{1}{C_j}\right)^2$ gives the diffusion potential (V_o) as *0.8 v* at *298°K*. The increase in V_o to *1.07 v* at *4.2°K* accounts for the fact that in Figure 1 the forward diode current limit (i.e., *+2 μa*) occurs at *+0.9 v* at *4.2°K*, while at *298°K* it occurs at *+0.65 v*. This, along with the decrease in R_s, accounts for the increased dynamic quality factor ($\tilde{Q}_1$) at lower temperatures.

The *4-Gc* nondegenerate parametric amplifier has been operated at liquid helium temperature. The effective input noise temperature, including the insertion loss of the room temperature circulator and a *17"* input coaxial line, was less than *24°K*. Of this, only *2°K* is believed to be due to the amplifier itself. Figure 4 shows a photograph of the amplifier with a *17"* input coaxial line. The amplifier mount is identical to that of the amplifier for the Telstar ground station receiver. The input frequency is *4.17 Gc* and the pump frequency *23 Gc*. The external idler load is removed, however, to accommodate the amplifier to an available helium dewar. The *3-db* bandwidth is more than *20 Mc* without external idler loading. With a forthcoming larger-necked helium dewar, which will allow external idler loading, bandwidths greater than *50 Mc* will be obtainable. The varactor diode used in this amplifier is the gallium-arsenide point-contact diode originally developed by *Sharpless* and further developed by *Vanderwal*[5,6]. The experimental results are tabulated in Table 1.

The accuracy of noise temperature measurement is believed to be *±6°K*. The noise figure of the mixer and *if* amplifier was *8.3 db* and the theoretical noise temperature was calculated based on the measured R_g/R_s [7]. The input pump power required for *20-db* gain was *20 mw*. Since the pump circuit was tuned from outside the dewar, only a few milliwatts were dissipated in the amplifier.

In future experiments, the amplifier (with external idler loading) and the circulator will be refrigerated to liquid helium temperature. The first stage liquid helium amplifier will be followed by a room temperature stage of the same design[2]. We expect to obtain an overall effective input noise temperature of less than *10°K* (corresponding to the last entry in line *3b* in table *1*) with *40-db* preamplifier gain and more than *50 Mc* bandwidth.

We believe that the overall noise temperature of the parametric amplifier will be as good as that of the maser. The parametric amplifier has definite advantages over the maser, i.e., broader bandwidth, higher saturation power level, lower pump frequency and power, and a simpler cryogenic system, since the operating temperature is not critical.

---

[1] Uenohara, M., "An Extremely Low Noise 6-Gc Nondegenerate Parametric Amplifier, *Proc. IRE*, p. 208; Feb., 1962.

[2] Uenohara, M., etal, "4-Gc Parametric Amplifier for Satellite Communication Ground Station Receiver," *WESCON* paper 7.2; 1962.

[3] Uenohara, M., "Noise Characteristics of Refrigerated Degenerate Variable Capacitance Amplifier at 6 Gc," *BTL* internal memorandum; unpublished.

[4] Blake, C., et al, "Helium Cooled Parametric Amplifier," submitted for publication to *Appl. Phys. Letters*.

[5] Sharpless, W. M., "Gallium Arsenide Point Contact Diodes, *IRE* Trans. MTT, p. 6-10; Jan., 1961.

[6] Uenohara, M., "An Extremely Low Noise 6 Gc Nondegenerate Parametric Amplifier," *Int'l Solid-State Circuit Conf.* DIGEST of TECHNICAL PAPERS, p. 60-61; Feb., 1962.

[7] Uenohara, M., and Seidel, H., "961 Mc Lower Sideband Up-Converter for Satellite-Tracking Radar," *BSTJ*, p. 1183-1205; July, 1961.

	Amplifier Temperature (°K)		
	298	*77*	*4.2*
(1) Dynamic Quality Factor			
$\tilde{Q}_1$ at 4.17 Gc	9.4	11.6	12.0
(2) Normalized Generator Impedance R_g/R_s	5.0	5.4	5.9
(3) Noise Temperature (°K)			
(a) Measured overall at gain = 20 db	192	79	42.0
30 db			24.5
35 db			23.5
(b) Amplifier only (with 17″ input line)	154	46	9.0
(c) Calculated at 20-db gain (without 17″ line)	154	38	2.0

TABLE 1

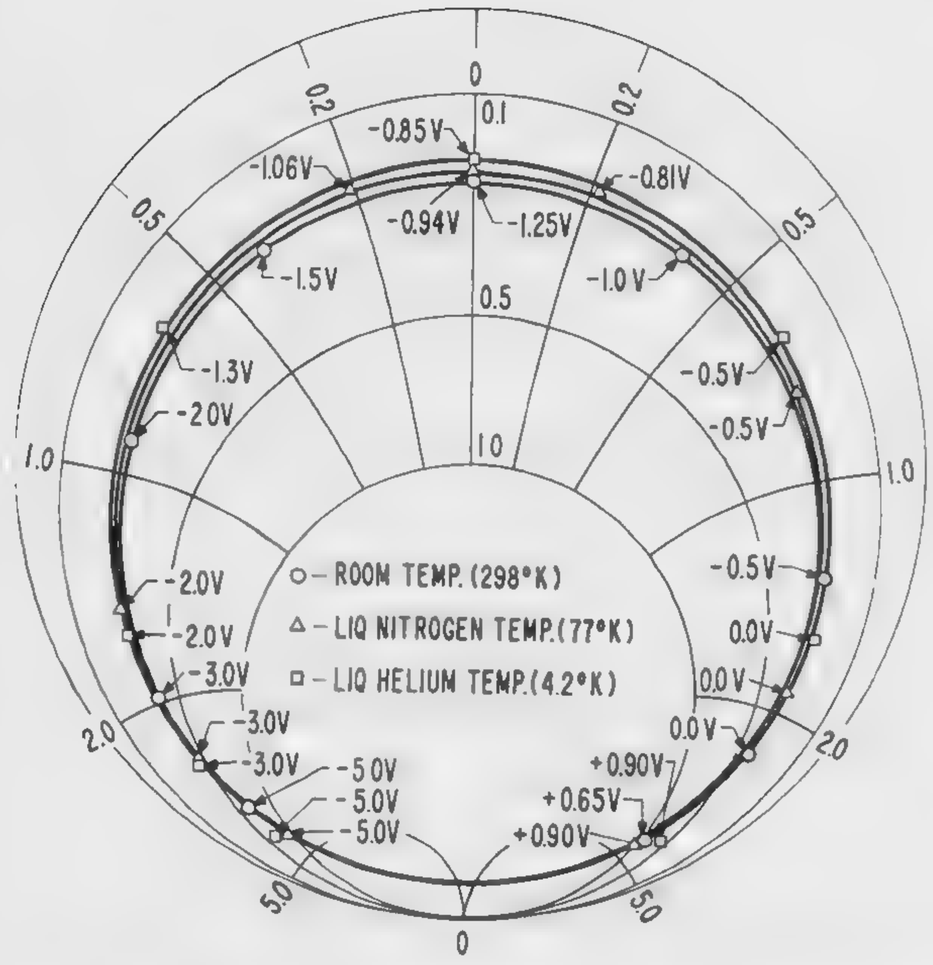


FIGURE 1—**Input impedance loci of *4-Gc* parametric amplifier as a function of temperature and bias voltage.**

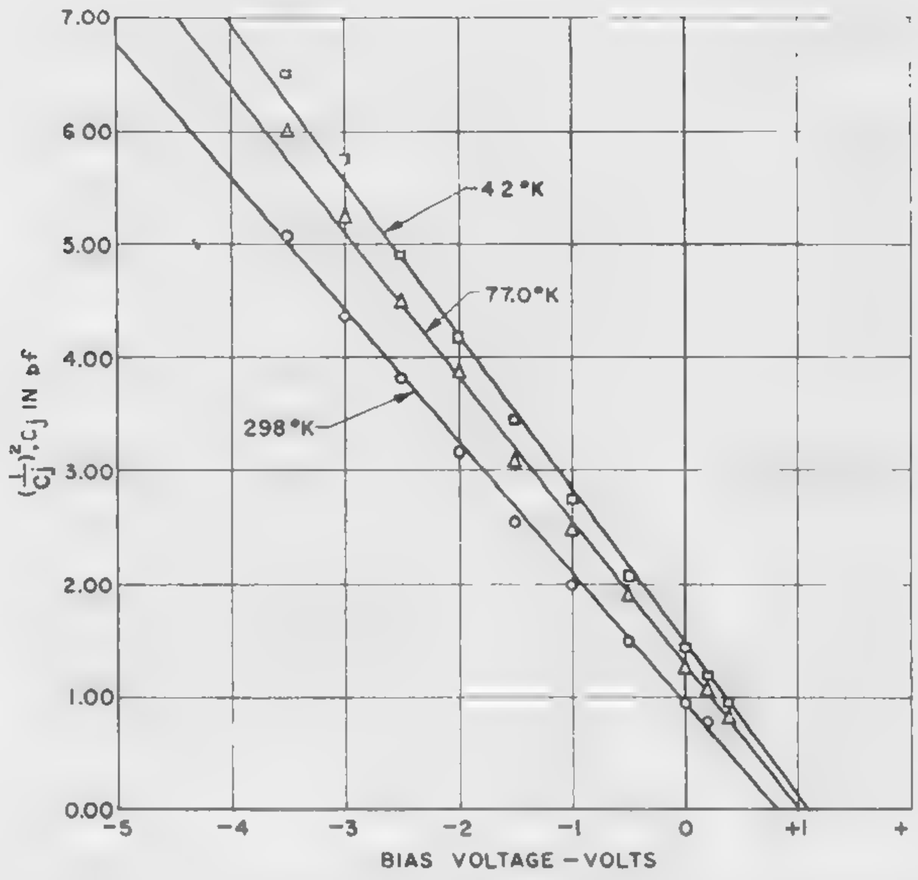


FIGURE 3—**Diffusion potential derived from $\left(\frac{1}{C_j}\right)^2$ as a function of temperature and bias voltage.**

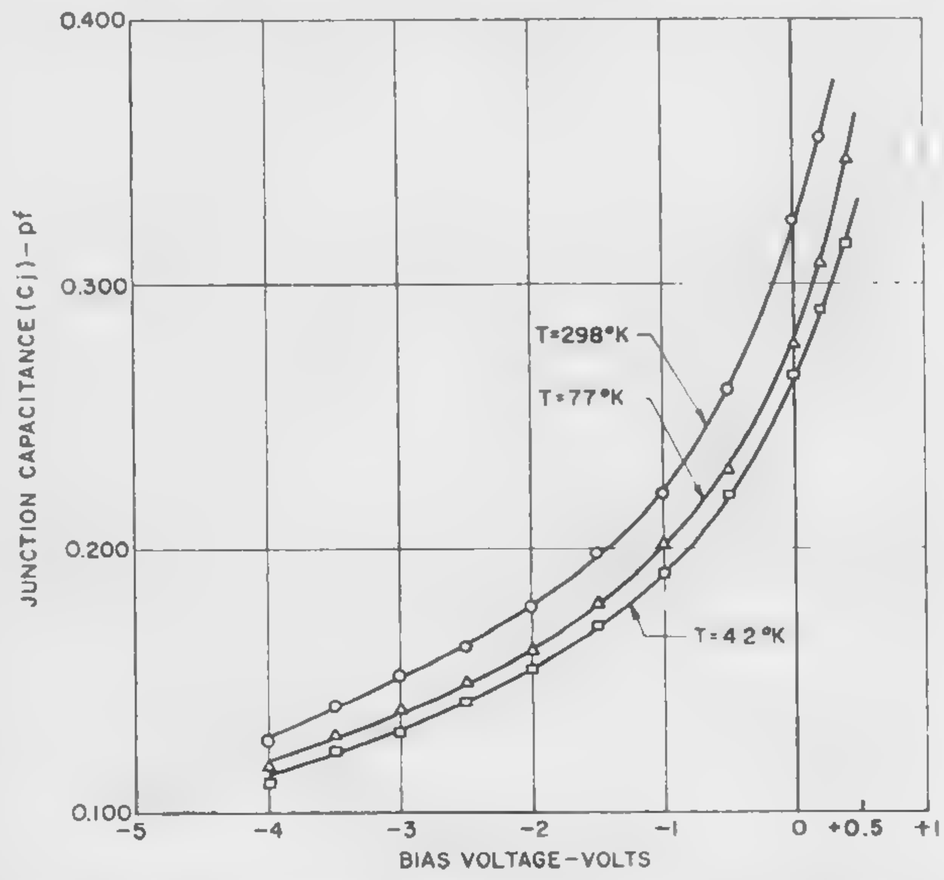


FIGURE 2—**Junction capacitance (C_j) of GaAs point-contact diode as a function of temperature and bias voltage.**

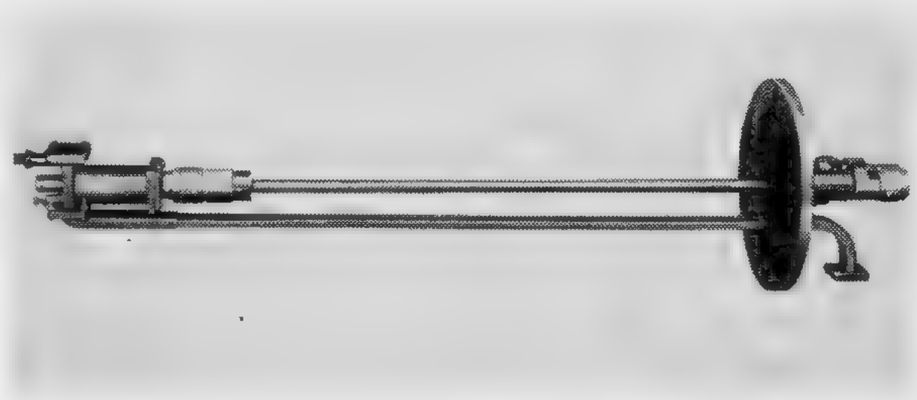


FIGURE 4—**Photograph of *4-Gc* parametric amplifier with *17″* input line.**

SESSION VI—TUTORIAL: Transistor Switching Circuits

Chairman: J. A. Narud
Motorola Semiconductor Products, Inc., Phoenix, Ariz.

THAM 6.1: Large Signal Models for Junction Transistors

J. A. Narud

Motorola Semiconductor Products, Inc.

Phoenix, Ariz.

D. J. Hamilton and F. A. Lindholm

University of Arizona

Tucson, Ariz.

THIS PAPER has been prepared to provide a tutorial analysis of three models for the large-signal behavior of the junction transistor: the *Ebers-Moll* model[1], the charge-control model[2], and the *Linvill* lumped model[3].

The scope of the talk will be limited to the fundamental principles involved in each of the models. Our principal objectives are: *(1)*—to derive, independently, each of the models, *(2)*—to show at what points equivalence among models exists, and *(3)*—to compare the models as tools for the analysis and physical understanding of transient performance.

Each of the models stems from a common mathematical model for the processes in a semiconductor material. Because of the distributed nature of the device, partial differential equations are used to describe the behavior of charge carriers. For simple cases, which, fortunately, are of considerable practical importance, exact solution is possible. Were it not for the complicated nature of the results, there would be no need for further modeling. All of the three models, then, are attempts to approximate the problem in such a way that the resulting degradation of accuracy is outweighed by the contribution to understanding and simplification.

In the *Ebers-Moll* model, certain measurable terminal quantities whose hyperbolic-function-representation is approximated by single-natural-frequency functions are defined. In the charge-control model, the partial differential equation of continuity is made an ordinary differential equation by integrating over the base region; further approximations are made to yield single-natural-frequency functions. The lumped-model approach serves to obtain an ordinary differential equation at the outset by eliminating the space variable through the use of difference equations. The *Ebers-Moll*, charge-control, and single-π-section lumped models are equivalent; however, the lumped model is most easily extended to yield more detailed results.

The Mathematical Model

The mathematical model common to all three models is a set of six basic equations for the base region, together with a description of conditions at the junctions. The six basic equations state that both hole and electron currents are the sum of drift and diffusion components; that continuity of both holes and electrons exists; that recombination is controlled by minority carriers; that net space charge is a function of hole, electron, and impurity densities; and that net space charge is the result of divergence of the electric field.

The principal function of the *pn* junctions is to determine the minority carrier densities at the boundaries of the base region, in accordance with the *law of the junction*. In addition, the junctions contribute space-charge regions resulting in capacitive effects. For the diffusion transistor, the following simplifying approximations are made: diffusion flow only, minority carrier flow only, and space charge neutrality within the base.

For convenience, regions of operation are defined. With one junction forward biased and one reverse biased, the transistor is operating in the active region; with both junctions forward biased it is in the saturation region.

The Ebers-Moll Model

The *Ebers-Moll* formulation relies upon some knowledge of the nature of the solution for the distributed base region. The solution is cast in two-port form where the port variables are collector current, emitter current and the excess densities at the boundaries of the base region. For the forward and inverse active regions, the measurable short-circuit current gains α_N and α_I are defined as single-pole functions of complex frequency. These represent approximations of the hyperbolic functions which make up the two-port parameters. Thus the forward and inverse active regions are each described by a first-order ordinary differential equation. The saturation region is considered to be the superposition of forward and inverse active region components; problems are solved by focusing attention on one or more components of current. The characteristic equation for the system in the saturation region yields two natural frequencies. For certain conditions of practical importance, one is dominant.

The Charge Control Model

In obtaining the charge control model, one removes the space variable of the partial differential equation of continuity by integrating over the base region. In the forward-active region, one thus obtains a first-order linear differential equation in time, relating base current I_{BF} and stored minority carrier charge Q_{BF}. Solution of transient problems is now straightforward; however, the variables are I_{BF} and Q_{BF}, rather than I_{BF} and I_{CF}.

In the steady state, the ratio I_{BF}/Q_{BF} is a constant, ω_{BF}. Since all currents result from diffusion, and are therefore related to the stored charge, additional constants ω_{EF} and ω_{CF} are defined as the ratios I_{EF}/Q_{BF} and I_{CF}/Q_{BF}, respectively, in the steady state. One next makes the key approximation that the spatial distribution of minority carriers in the base is at all times linear. We know, therefore, that when the continuity equation is integrated, the coefficients of the resulting ordinary differential equation will be ratios of charge control ω; i.e., constant (non time-varying) coefficients. Furthermore, the ratio $i_{CF}(t)/Q_{BF}(t)$ will be equal to the constant ω_{CF} defined previously for the steady state; thus one may conveniently use i_{CF} rather than Q_{BF} as the unknown function in the differential equation.

A similar procedure is used for the inverse active region; the ratio $i_{ER}(t)/Q_{BR}(t)$ is equal to the constant ω_{ER}, and i_{ER} may be used instead of Q_{BR} as the unknown function.

To complete the solution for a transient problem in either of the active regions, one determines the relationship of charge control ω to measurable qualities α_N, α_I, ω_N *and* ω_I, and then substitutes these into the differential equation, and solves.

In the saturation region, the same continuity equation describes the behavior of minority carriers; only the boundary conditions are different. Since the relationship between current density and minority charge density in the base is linear, and since the continuity equation is a linear differential equation, any saturation region

[Continued on page 119]

* This work was supported by Motorola Semiconductor Products, Inc.

[1] Moll, J. L., "Large Signal Transient Response of Junction Transistors," *Proc. IRE*, vol. 42, p. 1761; 1954.

[2] Beaufoy, R. and Sparkes, J. J., "The Junction Transistor as a Charge-Controlled Device," *Journal of Aut. Tel.-Elec. Co., Ltd.* (London), p. 310-327; Oct., 1957.

[3] Linvill, J. G., and Gibbons, J. F., "Transistors and Active Circuits," *McGraw-Hill Book Co.*; 1961.

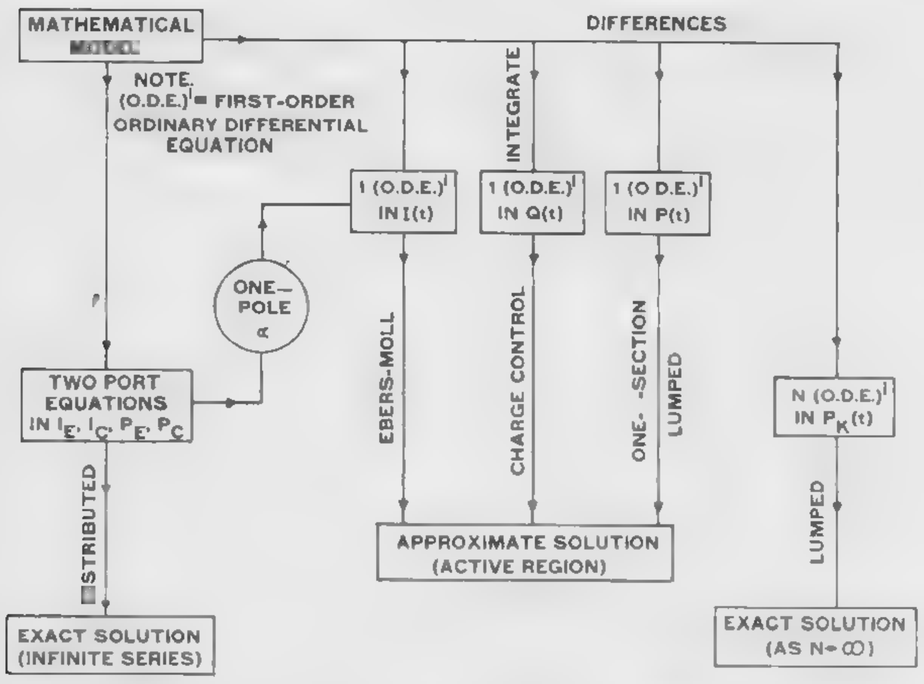


FIGURE 1—By various methods, all models avoid the cumbersome distributed solution. Superposition of active-region conditions may be employed to obtain a solution for the saturation region.

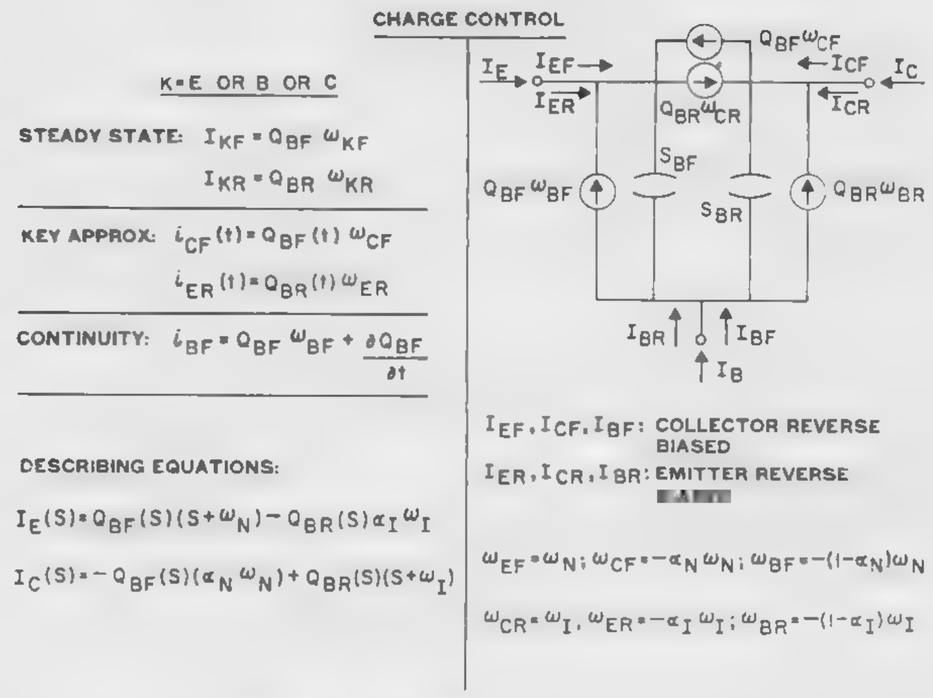


FIGURE 4—Space variables are removed by integrating the continuity equation over the base region. All currents are then related to forward and inverse stored minority charge.

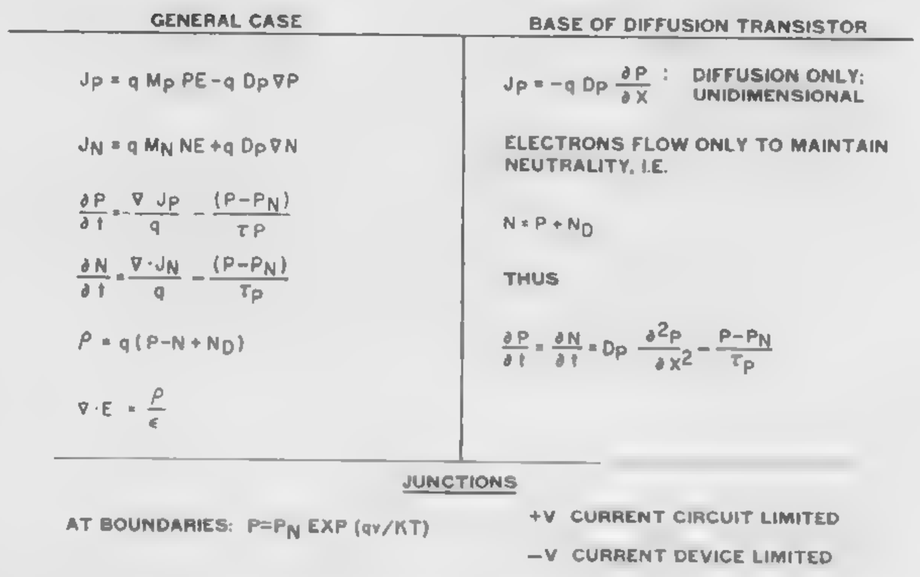


FIGURE 2—Mathematical model for *n*-type semiconductor, basic to all three large-signal models. For diffusion transistors, one dimensional minority carrier diffusion flow is assumed, together with space-charge neutrality.

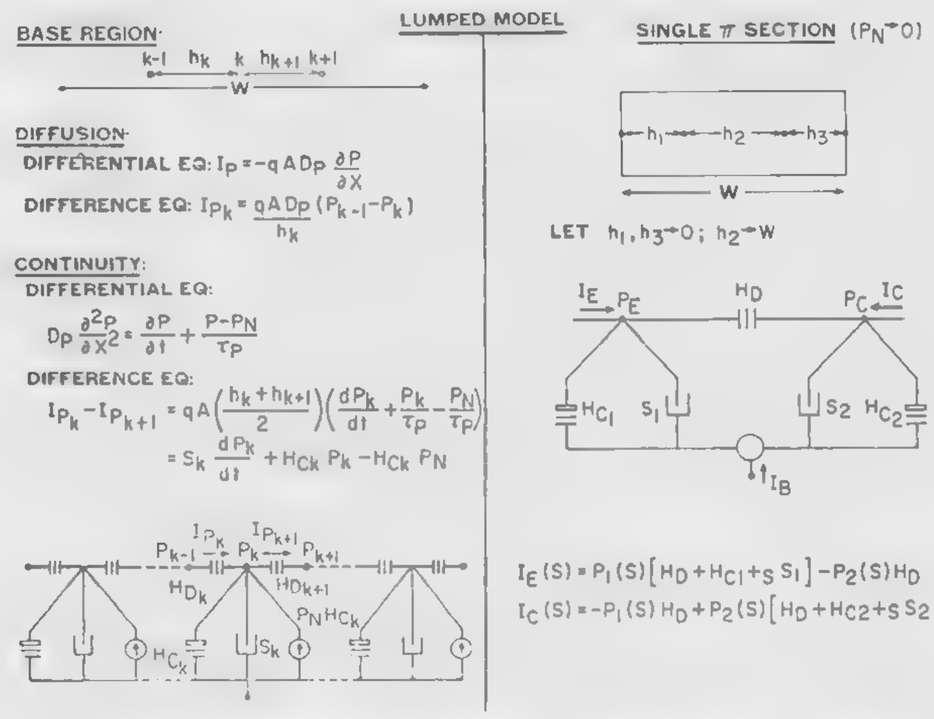


FIGURE 5—Space variables are eliminated by writing difference equations. Network-like lumped elements are defined which represent difference formulation and which exhibit *1:1* correspondence with physical processes.

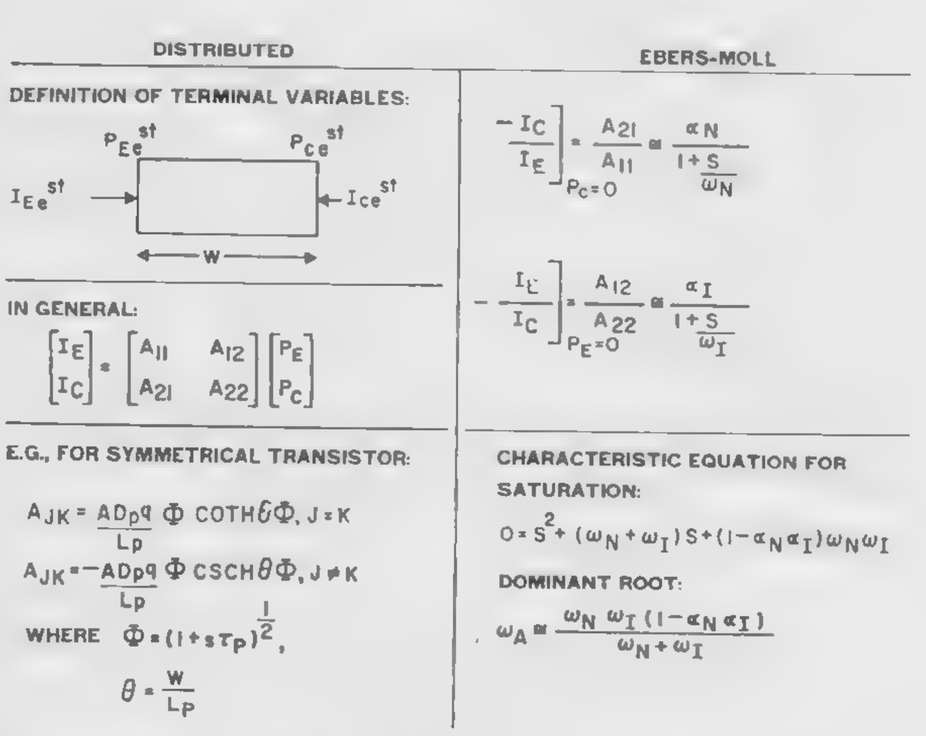


FIGURE 3—Transcendental functions are approximated by simple, algebraic functions for both normal and inverse active regions. The saturation condition is treated by superposition.

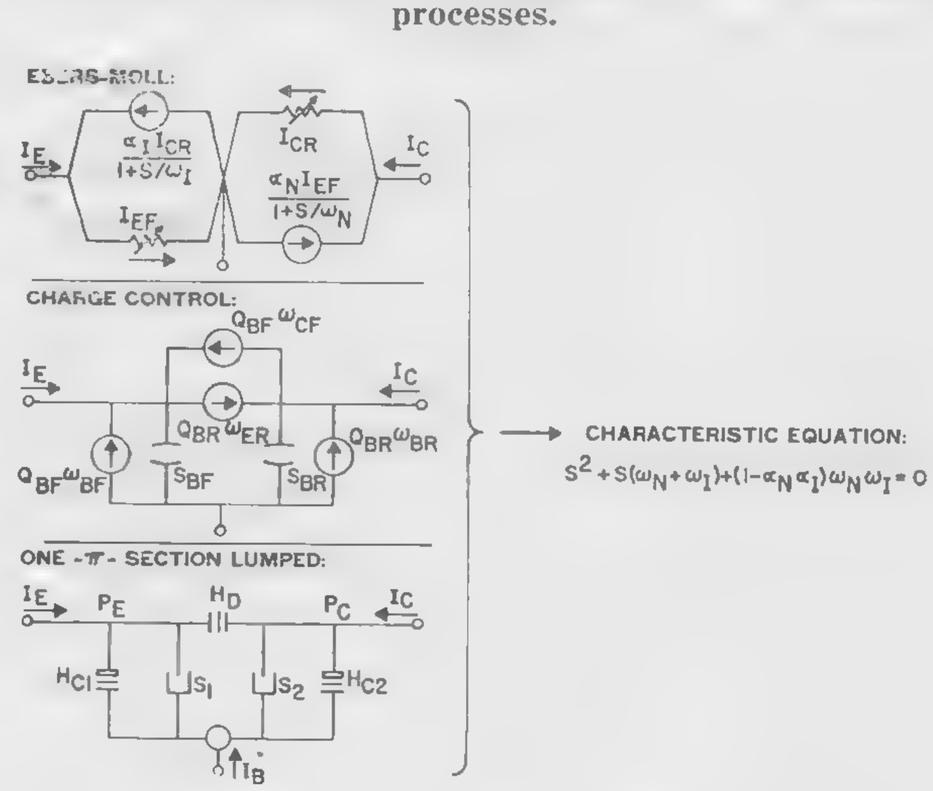


FIGURE 6—The three symbolic models lead to the same characteristic equation for the saturated condition. They differ principally in their ability to represent physical processes.

SESSION VI—TUTORIAL: Transistor Switching Circuits

THAM 6.2: Some Aspects of Digital Circuit Design

J. R. Turnbull

Components Div., IBM Corporation

Poughkeepsie, N. Y.

THIS PAPER will describe some of the basic tools employed by a circuit designer in the design of digital circuits. Because of the tutorial nature of this talk, some points will be treated in a rather basic manner, but it is hoped that the experienced designer will, nevertheless, find something of value.

A considerable portion of the body of knowledge of the circuit designer is *black art*, and as such is not easily generalized. Generalization will be attempted, where possible, but one should realize that the best techniques are those which are developed for the job at hand.

The design techniques to be described will be limited to those which apply specifically to level (base-band) circuits. One of the prime characteristics of any base-band circuit is that it exhibits a nonlinear *dc* gain curve. Figure 1 shows typical curves. Curve *1* intersects the unity gain line in three places and possesses stable *dc* levels *A* and *B*. Curves *2* and *3* are unsatisfactory since they exhibit only one stable *dc* level. A particular design technique must guarantee the existence of the unity gain points. To complete the design, one must accomplish two things. The best design technique must be found for a particular circuit, and the parameter limits determined to guarantee proper operation in the *worst case*. When a device has been in production a long time, this may not be difficult; but when a new device is to be used, the choice of parameter limits becomes somewhat subjective because complete information is lacking. A further problem is to determine the degree of conservatism to be used in design. That is, should all parameters be taken at their worst end-of-life limits? Perhaps this is too severe, and we need take only one (or possibly several) of the parameters at their end-of-life limits. It can be easily seen that this is an area in which considerable disagreement can (and does) arise. Suffice it to say that a common technique is to take the parameters of the most critical components at their worst-case limits, and all other components at a less conservative value. For example, we might use end-of-life transistor parameters and initial (or purchase) limits for the various resistors. This approach is quite conservative, and that the probability of the worst case occurring is very small. This suggests that statistical techniques could be used to considerable advantage to predict a failure rate and give a much better picture of the actual degree of conservatism.

Since the digital-switching circuit exhibits non-linear gain properties, the non-linear behavior of the transistor characteristics with current and voltage must, in general, be considered. There are circuits, however, for which linearization of the device characteristics is possible. This simplifies the procedure and permits moderately simple analytical equations to be used. For example, consider the resistor-coupled *NOR* circuit shown in Figure 2. The design is initiated by choosing a nominal collector current of *6 ma*. Since the transistor impedances are much lower than the expected resistances, we can make choices of the emitter-base and emitter-collector voltages which are virtually independent of the unknowns R_1 and R_b. Two inequalities can then be written, one of which guarantees the minimum base current needed to keep the transistor saturated, and the other of which guarantees a minimum *off* bias. From each of these equations R_b is obtained as a function of R_1. The resulting inequalities have the form:

on case:
$$R_b \geq \frac{1}{R_1 + aR_1 + b} \qquad (1)$$

off case:
$$R_b \leq \frac{1}{c + d/R_1} \qquad (2)$$

These equations are plotted in Figure 2 for a particular set of transistor parameters. We see that no unique pair of unknowns is satisfactory. Rather, any pair that intersects inside the area of solutions and thereby satisfies both *on*- and *off*-case equations will guarantee proper operation. One pair, $R_1 = 7.5\ k\Omega$, $R_b = 36\ k\Omega$ is shown. With the boundaries that give satisfactory *dc* performance defined, the actual choice may be determined through some other criterion, such as minimum power dissipation, maximum *off* drive, etc.

It is unfortunate that there are many circuits for which it is not possible to linearize the device characteristics. In these cases, analytical expressions for the minimum levels become somewhat complicated, and graphical procedures become useful. There are, however, disadvantages to graphical techniques. For example, cut-and-try procedures are frequently necessary, and the effects of changes in parameters, current operating levels, etc., are more difficult to determine.

A graphical procedure which is used to design a current switching circuit is shown in Figure 3. One begins by choosing a nominal operating current level. The maximum *off* and the minimum *on* output currents are then plotted as a function of the input voltage as shown. Load lines formed by the V_c, R_c combination are then drawn on these transfer characteristics. The load line which generates the minimum down level *D* has an intercept of $V_{c\ max}$, while the load line which guarantees the minimum up level *A* has intercept V_x, where

$$V_x = V_{c\ min} - I_b R_{c\ max} \qquad (3)$$

The satisfactory solution is the one which provides an adequate minimum noise tolerance. The usual definition of a maximum permissible noise pulse is that amplitude at the input which is transmitted through the circuit with unity gain. For negative pulses, this is V_A-V_B, and for positive pulses it is V_C-V_D. Equation *(3)* may be solved for I_b, which leads to the maximum number of loads, which may be driven. The gain curve which results from this procedure is shown in Figure 4.

Anyone who has tried to select a number of devices, each of which has all its parameters worst-case, can appreciate the extremely small probability of the occurrence of the worst-case circuit. Most circuit designs based on worst-case tolerances are extremely pessimistic, and the result is a degradation in circuit performance. There are also circuits which cannot be designed with a worst-case philosophy, but which are otherwise very attractive. A solution to this problem is to apply statistical techniques to the design and predict a failure rate. A satisfactory failure rate depends on the desired reliability of the machine in which the circuits are to be used.

A commonly-used statistical technique is the *Monte Carlo* method. This technique involves random sampling of each parameter which appears in the circuit design equations. After a set of parameters is selected, these are *plugged* into the equations, and the output parameter is calculated. This procedure is repeated a large number of times (typically *10,000*) to determine the distribution of the output parameter. Tolerable limits of the output parameter are defined, and the total number of cases which lie outside these limits then gives the failure rate. The *Monte Carlo* approach has the advantage that it can be programmed on a computer in such a fashion that it will handle a large number of different problems. It has the disadvantage that the failure rate cannot always be accurately assessed even with *10,000* samples. Because of this restriction, it is frequently possible to obtain better results with *hand* techniques.

An example of a graphical technique is shown in Figure 5. Here, we wish to solve for the distribution of the

[Continued on page 120]

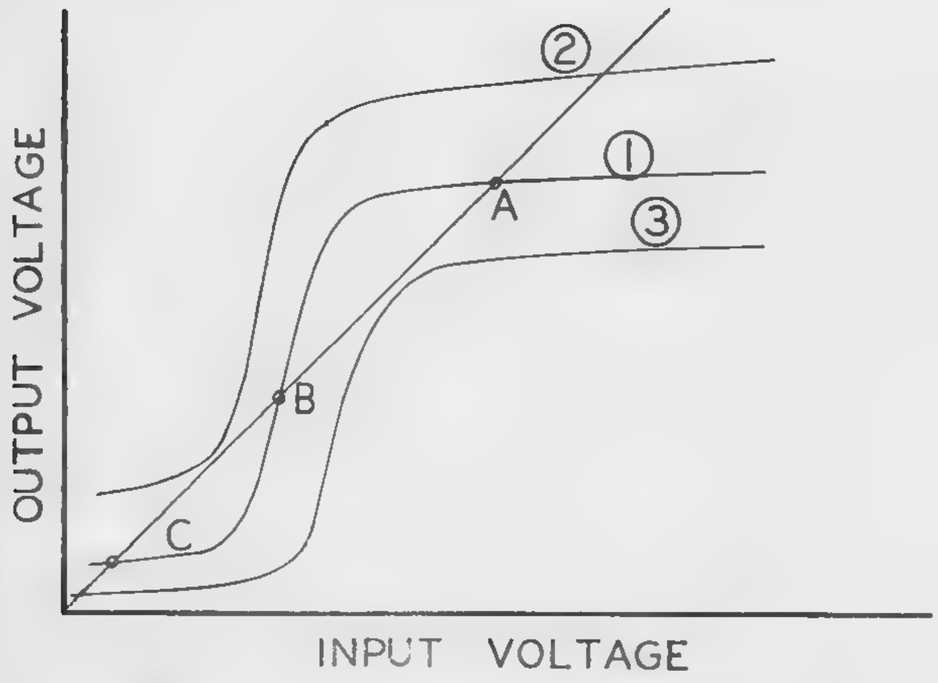


FIGURE 1—Examples of the nonlinear gain curve which typifies the digital switching circuit. Only curve *1* gives satisfactory operation.

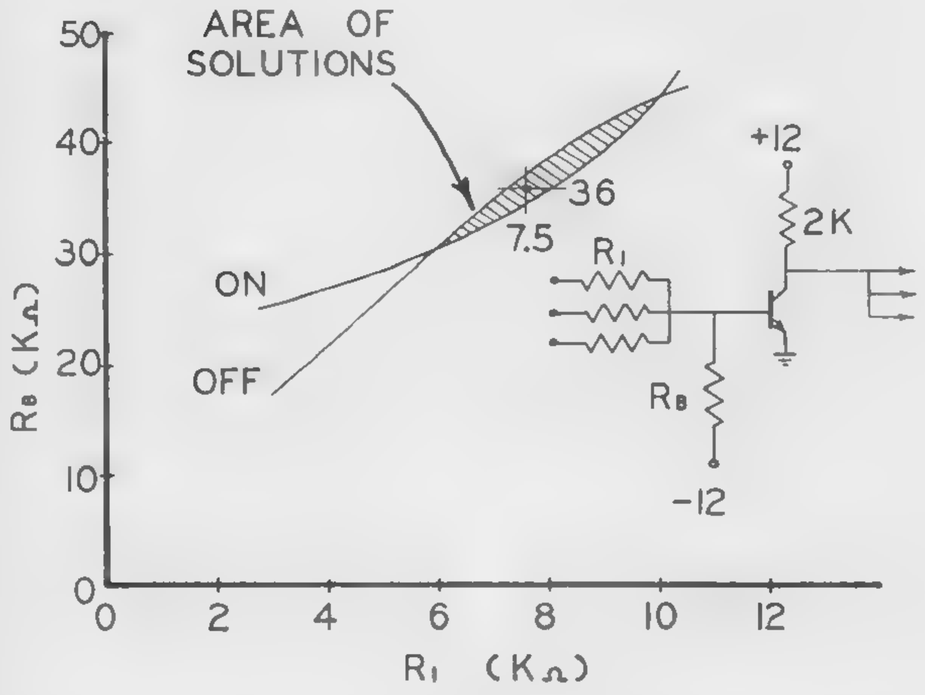


FIGURE 2—The *NOR*, an example of a circuit for which equations can be written to guarantee proper operation.

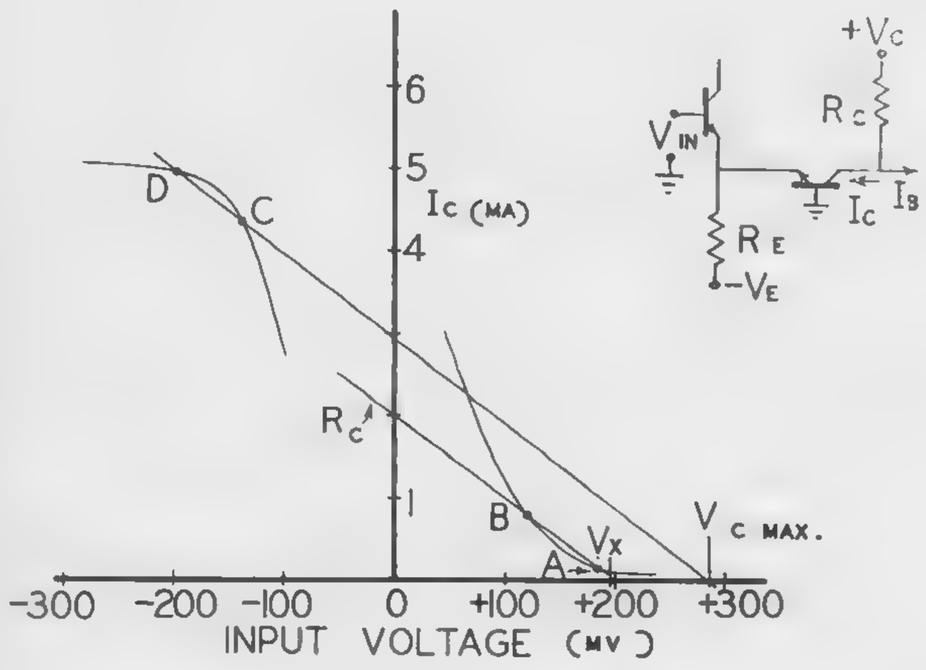


FIGURE 3—An example of a graphical technique used to guarantee the existence of three unity gain points in the worst case.

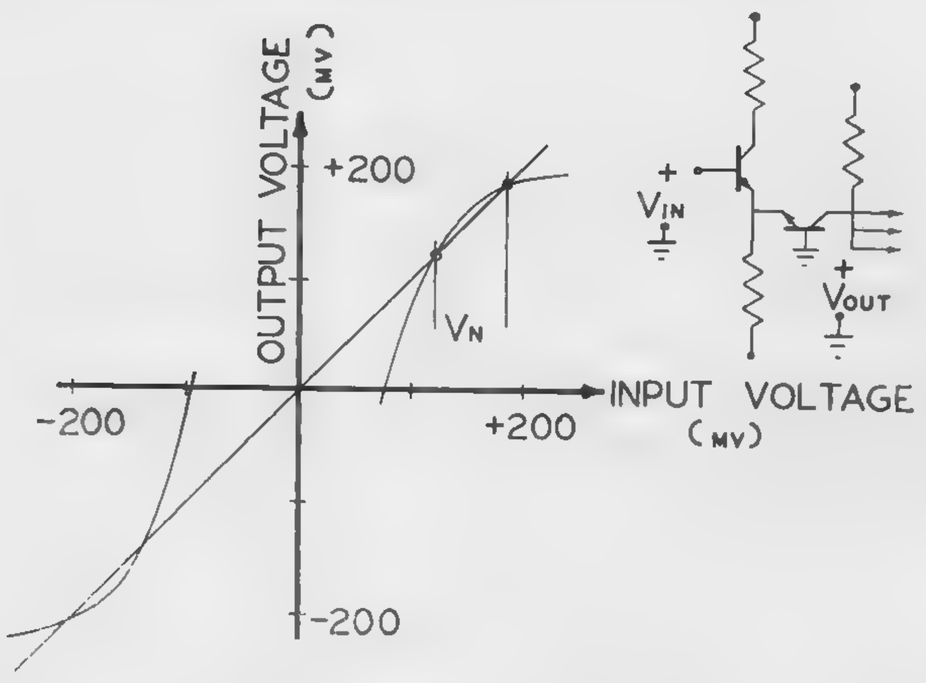


FIGURE 4—Gain curve which results from the design of Figure 3.

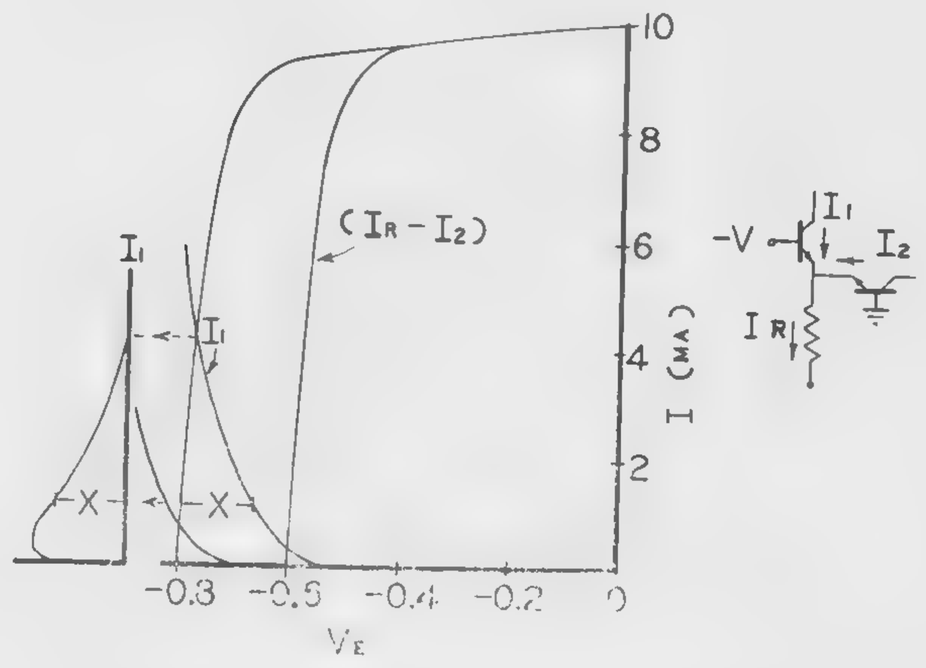


FIGURE 5—An example of a current distribution obtained from a graphical design technique.

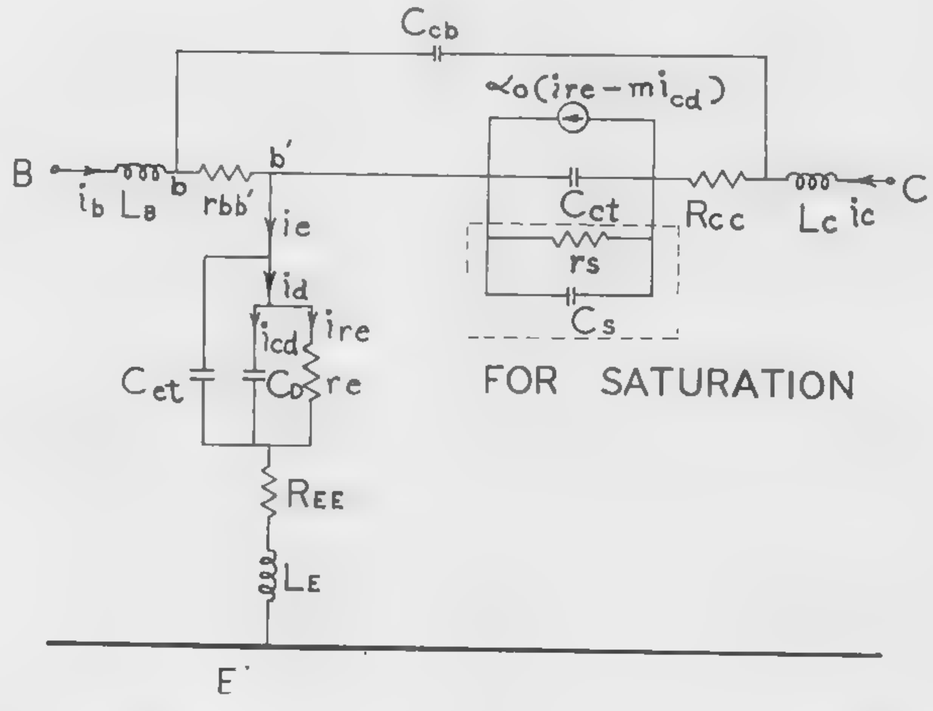


FIGURE 6—Piecewise-linear, small signal equivalent circuit.

SESSION VII—INVITED: Solid-State Sensing

Chairman: R. P. Rafuse

Research Laboratory of Electronics, MIT, Cambridge, Mass.

THPM 7.1: Solid-State Sensors for Process Control

E. Stern

Advanced Systems Development Div., IBM Corporation

Yorktown Heights, N. Y.

In recent years solid-state sensors have begun to take their place in the field of industrial instrumentation. The process is a slow one; however, as increasing numbers of industries become more control conscious, i.e., as high-speed digital computers are applied to the task of gathering and digesting process data, the need for improved sensing techniques reaches critical proportions.

Some of the requirements imposed upon sensors to make them compatible with the great speed and accuracy of the computer and the needs of the process are:

(1)—Fast response time; desire to monitor control points more frequently.

(2)—Accuracy; computer makes instantaneous decisions on the basis of acquired data. Improving process efficiency is a function of the accuracy of the data.

(3)—Sensitivity; the better the resolution, the finer the control which can be exerted by the computer.

(4)—Low cost; human operators not being required for meter reading, economically-priced units permit utilizing machine speed for sensing a large number of control points.

(5)—Common language; ideally one would like to have digital sensors for greater accuracy and compatibility with machine language. Alternatively, a language such as frequency, common to all transducers, should be employed to avoid the expense and complexity of a variety of analog-digital *(A-D)* conversion equipment. In addition, this language should be one that eliminates the need for handling low level signals with their inherent error content.

Solid-state devices come closest today to meeting the requirements outlined. Properly-prepared semiconductors, for example, can be made highly sensitive to most of the variables of interest in industrial applications: temperature, strain, light intensity, radiation, humidity, etc. Moreover, they respond to all these variables with a change in resistance, i.e., a common language. The single-crystal nature of semiconductor devices and the high sensitivity to environmental conditions, permit great accuracy in determining resistance. Cost is low, and smallness of the devices contributes to fast response times.

Having resistance as a common language still requires *A-D* conversion techniques. However, the nature of semiconductors is such that conversion would take place with high level signals. More compatible with conversion to digital form is the language of frequency; techniques for counting cycles are well developed. Frequency-modulated signals can be transmitted more readily over great distances and are less subject to some of the problems common to *dc* signal transmission. This suggests systems in which a change in sensor resistance is immediately translated into a corresponding change in frequency.

Examination of industrial sensor requirements reveals a number of interesting facts. In a typical industry, about *70%* of all measurements taken are of temperature. About *20%* may be strain and derived parameters such as pressure; the rest includes measurements of flow velocity, level, weight, and a host of analytical instruments.

Current techniques for temperature measurement used in process control seldom yield overall accuracies better than *±3%*. Thermocouples have an inherent inaccuracy compounded by calibration drift. Moreover, further inaccuracies can be introduced by associated detection equipment and faulty installation. Radiation detectors for temperature sensing are no better in this respect and have some additional problems unique to optical instruments; namely, varying emissivity of target area, absorption through intervening medium, and cleanliness requirement of optical elements. A number of different sensors is often required to cover an extended temperature range; some of these may not be compatible with each other. Finally, thermocouples respond rather slowly. A delay of minutes in signalling that temperature has risen can be very costly.

Pressure-measuring devices are available in even greater variety, each device limited to a particular range of pressure, a given set of environmental conditions, or a given accuracy requirement. Although individual strain-gage instruments may have accuracies as high as *0.1%*, few devices employed in process control show an overall system accuracy better than *1%-2%*. These gages also require frequent calibration to compensate for creep and aging.

A class of transducers, binary state indicators, perform *on-off* functions in a great variety of tasks; results include indications of limits in pressure, temperature, etc. The measurements of flow velocity, light intensity, and radiation, though less prevalent, also are vital tasks in process control.

Flow meters seem to be among the less accurate instruments; an accuracy of *±5%* is common. Yet, in some processes a *1%* variation in the flow rate of critical raw materials could wipe out thousands of dollars a day in profits.

A common procedure in process control is to take the analog signals from the sensor and convert these into digital form in an *A-D* converter. Sophisticated circuit techniques are required to handle the low-level sensor signals without loss of accuracy and to eliminate such undesirables as common mode signals, and noise. In many installations thermocouple extension leads are carefully shielded, and strain gage excitation is maintained with chopped *dc*.

Solid State Sensors

It appears as if use of already existing solid-state devices and techniques should serve to alleviate some of the difficulties mentioned.

Significant advances have been made in recent years in the thermistor, one of the most accurate, stable, and reliable temperature sensors available. Accuracies of *0.1%* or better with negligible drifts are possible. The devices are made in extremely small sizes, yielding very rapid response times. Temperature limitations are still severe; few thermistors are available with useful sensitivity above *300-400° C*. The logarithmic resistance-versus-temperature curve provides a high sensitivity at low temperatures which decreases rapidly at higher temperatures.

To offset this major disadvantage of thermistors, the positive temperature coefficient resistor *(PTC)* has been developed. Suitably-doped single-crystal semiconductors exhibit a positive temperature coefficient of resistance in the extrinsic portion of their conductivity curve. Several such devices have appeared on the market recently which employ boron-doped silicon to achieve a linear response from *−150° C* to *+200° C* with a sensitivity of about *0.7%* per degree C. These *PTC* resistors also have good manufacturing tolerances. The single crystal nature of these devices results in greater stability without the need for pre-aging, which is common to thermistors.

Research has been conducted in our laboratories to explore the feasibility of such devices with a much

[Continued on page 120]

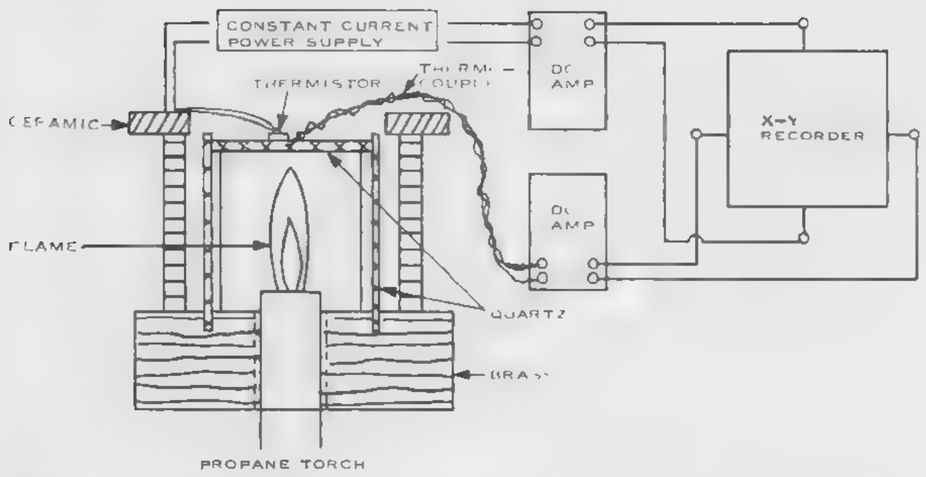


FIGURE 1—**Setup for rapid testing of SiC thermistors. The thermistor rests on a quartz plate located by a propane torch. A Pt-Pt *13%* Rh thermocouple is in intimate contact with the thermistor.**

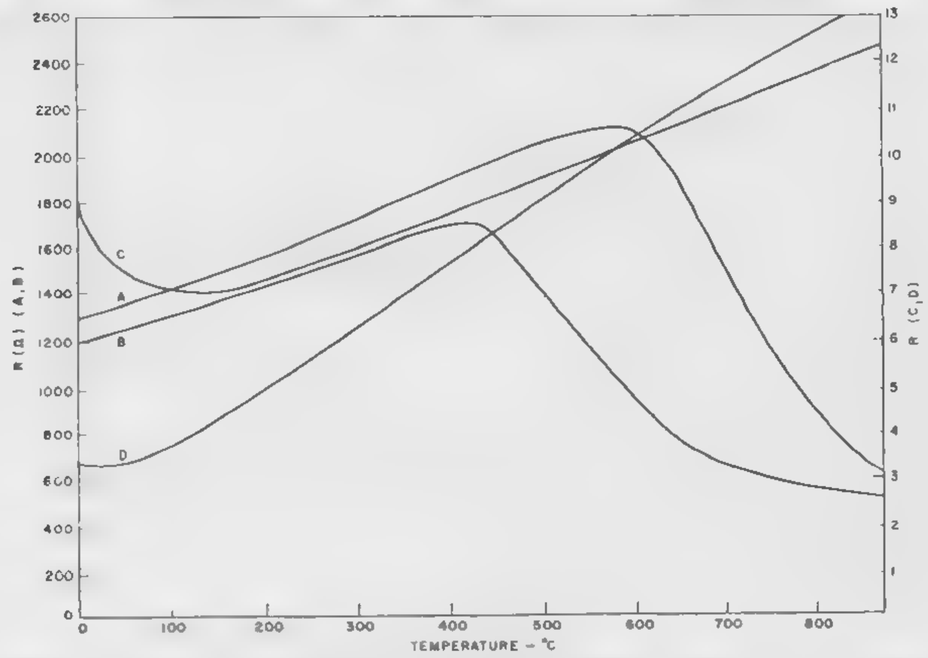


FIGURE 2—**Resistance versus temperature curves for a number of SiC thermistors. These curves were produced by using the setup of Figure 1; the time for a complete run from room temperature up to *900° C* and back down, took less than two minutes.**

(Above)
FIGURE 3—**Silicon carbide thermistor in the flame of a propane torch. No measurable change in characteristics was observed after repeated exposure to the torch flame.**

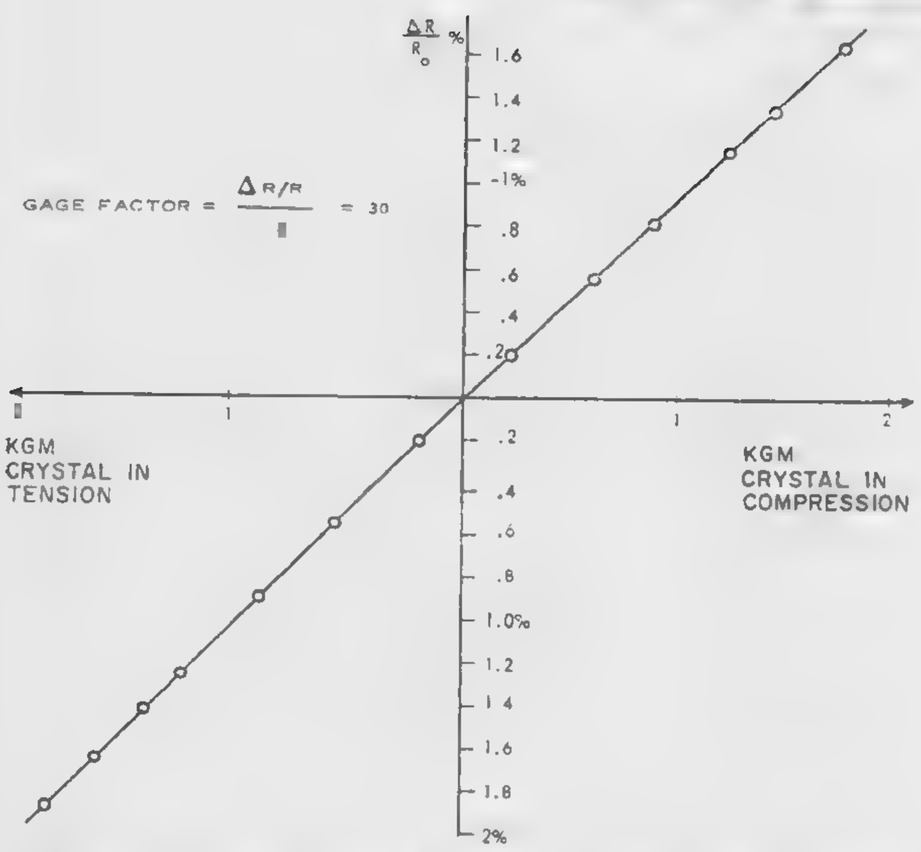


FIGURE 4—**The $\Delta R/R_o$ versus force for silicon-carbide strain gage. SiC filaments were mounted on a cantilevered beam and measurement taken with strain gage in tension and compression. The range displayed covers only $\pm$ *400* μ *strain.***

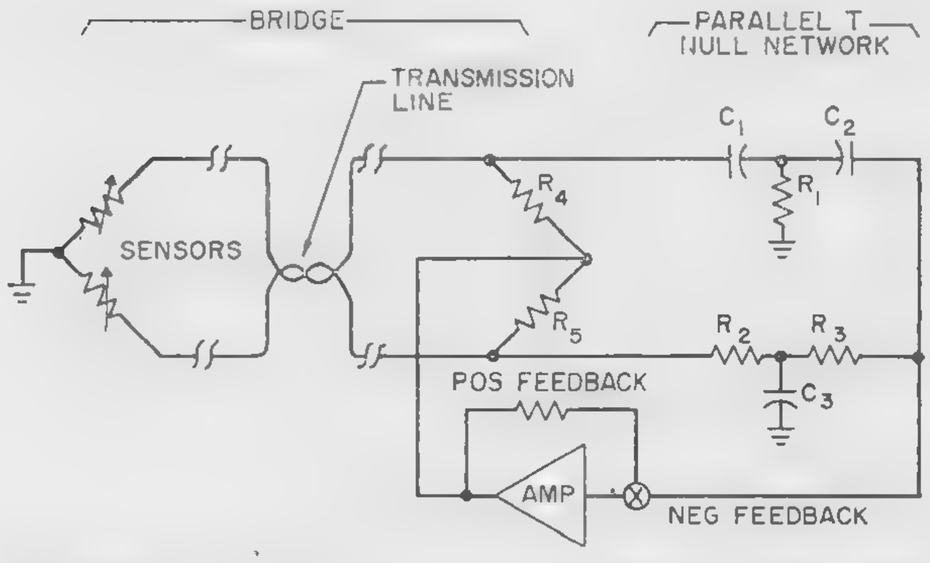


FIGURE 5—**Dual-input twin-T oscillator. Basic system, with sensor as part of the feedback loop of an oscillator, is illustrated. Many remote sensors may share the same amplifier-bridge.**

SESSION VII—INVITED: Solid-State Sensing

THPM 7.2: Considerations Underlying the Study of Sensory Elements*

J. Y. Lettvin

Dep't of Biology and Research Laboratory of Electronics, MIT

Cambridge, Mass.

A SENSE ELEMENT is a nerve cell modified to respond to a definite kind of energy or information, and is usually shielded from other influences. In a way, every neuron is sensory, for it must detect the activity in some other neurons and ignore the rest. But *sensation* can be reserved to mean that process whereby signals from outside the nervous system are transformed into nervous signals. This process involves amplification, for nervous action is powered independently of those events it represents.

The action of the world on a sense cell may be immediate, i.e., directly coupled to the amplifier. For example, in certain fish some nerve endings are very responsive to small electric currents and are shielded from other influences, or the action may need mediators. For example, in the rods and cones of the eye there are photosensitive pigments that bleach on exposure to light. It is what happens to the pigments that is amplified. But the common feature to all sense organs is this amplifier —the nerve membrane—and we should understand its operation before delving into sensory physiology. The following, a peripheral account is centered about the contemporary view as derived from *Hodgkin* and *Huxley, Ussing, Teorell, Keynes,* and others. Quantitative discussion has been foregone in favor of imagery.

Electrical activity of nerve and muscle was originally measured as a flow of current. That it was a current seemed certain, although neither bubbles appeared nor metals plated out in the tissue as might be expected if it were due to a reduction-oxidation battery. The shock of an electric eel could put a spark across a gap or be used to plate out metals in a system coupled to the eel by electrodes. The high point in measurement of such activity was reached by *Bernstein* in 1861. He studied the current flowing during a single synchronous nervous discharge in a bundle of fibers. Plotted as a function of time it included frequency components up to at least *10 kc*. Additionally, he showed that during a nervous transient, excited from an external source at one point along the nerve trunk, current initially flows into the nerve fibers at that point for much less than a millisecond and then flows out afterward for about a millisecond or two. Furthermore, it was found that the maximum strength of the inward current was about ten times larger than the maximum of the outward current; this has subsequently proved to be a reasonable estimate. Until ten years ago, it remained a difficult problem to account for these currents, even qualitatively. In 1952 *Hodgkin* and *Huxley* published a study on which our current views rest.

Let us first imagine how electrical work can be performed by ionic solutions without involving oxidation or reduction. It will be recalled that in a solution of an ionized salt such as KCl, the different ions take on shells of hydration and move about independently of each other like a mixture of gases. There is a local electrical neutrality everywhere for there are as many K^+s as Cl^-s. Every K^+ has its field restricted by the cloud of Cl^- in the vicinity, and vice versa for every Cl^-. Like gases, these two ionic atmospheres exert an osmotic pressure whose formula is very much like the gas law: $\pi = RTC$, where C is concentration, i.e., n/V. Suppose we have such a solution inside a sack and immerse it in a bowl of water in which non-ionized material, such as sugar, has been dissolved so as to keep net osmotic pressure the same on both sides of the sack wall. If we make that wall such that K^+ will penetrate it, and also H_2O, but not Cl^- or sugar, what will happen? K^+ will push out through this wall under its own osmotic pressure. But as it leaves, an excess of Cl^- is set up on the inside of the sack, an excess of K^+ on the outside, and this distributed dipole over the sack wall sets up an electric field across the wall opposing the further flow of K^+ outward. When this potential becomes large enough that there is no net movement of K^+ across the wall, then this potential is that which is in equilibrium with that concentration of K^+ inside the sack. More concisely, it is the potential of that concentration. If u is the mobility of K^+ in the membrane, and F (the Faraday) is the number of coulombs/mole, the flux of K^+ outward under its osmotic pressure equals the flux inward under the electrical field, so that $uRTdC = -uFCdE$; $E = E_o - \frac{RT}{F} \log C$, where E_o is a constant of integration. If KCl is in the bathing solution, in a different concentration from that inside, and the osmotic balance has been made up with, say, sugar, then

$$E_{inside} - E_{outside} = \frac{RT}{F} \log \frac{C_{out}}{C_{in}},$$

the familiar *Nernst* equation. The reverse electrostatic potential would occur if the sack were permeable to Cl^- but not to K^+.

This statement of difference in energy level across the sack wall, which is due to unequal concentrations of dissolved ions, can be given potentiometrically for each species of ion. But how can this difference be dissipated to perform electrical work? If the sack wall were simultaneously and everywhere made permeable both to K^+ and Cl^-, the net ionic flow of each in the same direction results in equal and opposite currents everywhere along the path of diffusion. But it is immediately apparent, that if *one* patch of the sack were made permeable only to K^+ and *another* patch elsewhere made permeable only to Cl^-, then the concentration difference across the sack wall would run down via a current flow from the K^+ patch to the Cl^- patch on the side of lesser concentration of KCl and in the reverse direction on the side of greater concentration.

This notion can be extended widely. For example, it may be considered that the sack be filled with a certain concentration of KCl and bathed with a solution of equal concentration of NaCl. Now let the sack wall only pass K^+, but not Na^+ or Cl^-. If you now add a salt bridge between the inside and outside, K^+ will flow outward through the wall; there will also be a diffusion through the salt bridge inward of Na^+ in excess of the diffusion of K^+ outward through the bridge. Thus the system will run down in part by diffusion, but also in part by conduction of current outward through the sack wall and inward through the bridge. This drift of positively-charged ions through a relatively driftless cloud of oppositely charged Cl^- is reminiscent of the drift of electrons along a wire.

Thus a concentration cell can be made to do electrical work without oxidation-reduction occurring, provided only that the various types of charges can be separately channeled. Before we go on to the nerve, however, let us consider again the previous example of the sack of KCl solution in a bath of another KCl solution osmotically adjusted to the inside concentration with sugar. After the wall is charged up to equilibrium potential, no more net current flows. Yet, of course, there will be a continuous net exchange if the fluxes in balance are nonzero. For example, suppose that all the K^+ inside the sack has been radioactively tagged. Its access to the sack wall

* This work was supported in part by the U. S. Army, the Air Force Office of Scientific Research, and the Office of Naval Research; and in part by U. S. Air Force (ASD) Contract AF33(616)-7783.

is constant if the internal concentration is kept constant. Its rate of movement through the wall thereafter depends on the potential to which the wall is charged. But this potential depends on the concentration of K^+ on the outside. Thus, you get the impression that the rate at which the tagged K^+ moves into the surrounding bath increases as the concentration of K^+ in that bath increases. That is another way of saying that, at equilibrium, the total exchange in the system is rate-limited by the lower flux (arising from a lower concentration). However, it also implies that the conductance of K^+ through the membrane is a function of voltage, decreasing as the absolute magnitude of the membrane potential increases.

This is further complicated by the notion that if the ionic channel is specific for K^+ and has a smaller capacity to carry K^+ than the fluid media on both sides of the membrane, the flux from the lower concentration to the larger will be further reduced by preemption of the channel by the larger concentration. This ought be the case whether you suppose micropores through the membrane or specific ion carriers. Indeed this interaction has been observed in both nerve and muscle. Under conditions which favor the increase of a particular ionic flux one way across the membrane, the flux of that ion the other way is reduced.

These brief comments may serve as a background against which to view the complexity of nerve membrane. In view of our interest in providing a quick image, rather than a digression of formal relations, the liberty of developing a quite unjustifiable genetic sketch is being taken; one that should be regarded as a metaphor. Imagine a long balloon of a membrance both filled and bathed in the same solution in which Na^+ is twenty times richer than K^+ and there is the proper complement of Cl^-. Now let this membrane be semipermeable to all these monovalent ions; e.g., on an ultramicroscopic scale it is composed of tubules or channels, and each tubule passes only one of the three ions and water. (Alternatively the ions may be transported across only if carried by special compounds. In either case you have the channel defined.) Now let us add two more features. First, given a source of certain foods, the cell converts part of the energy stored in the food into establishing an electric field only in those channels that pass Na^+. Thus the only way in which any of the other ions could be affected by this field is by its effect on the Na^+ ions. This field is positive toward the inside of the wall and negative toward the outside. Na^+ then tends to move out more easily than it moves in, and it will continue to do so until the field set up by the concentration difference of Na^+ balances that due to metabolism. Here is a mechanism very much like that of a triode. Next, some food is converted, by metabolism, into a store of negatively-charged organic ions inside the cell. These never pass the membrane and accumulate in the amount needed to maintain osmotic balance.

At the start of this system, the outward flux of Na^+ is larger than the inward, and this constitutes a flow of current into the cell. In the two media, this current is carried by net movements of all ions. There is a voltage gradient across the membrane (except in the channel for Na^+), positive on the outside. Thus, the inward flux of K^+ will exceed the outward flux; the outward flux of Cl^- will exceed the inward. The nondiffusing anions within the cell maintain the osmotic pressure, and K^+ starts concentrating on the inside and Cl^- rarefying. Since the fixed field within the Na^+ channel produces a current generator, the system boot-straps itself up until the concentration potential of each of the passively diffusing ionic species becomes equal and opposed to the driving force of the Na^+ on it. In nerve tissue this state is reached when the C_{Na+} inside $= 0.05$ C_{Na+} outside, C_{K+} inside $= 20$ C_{K+} outside, and C_{Cl-} inside $= .05$ C_{Cl-} outside. There is an adjustment to be made because of the presence of the nondiffusable ions, the *Gibbs-Donnan* equilibrium, but it can be neglected here.

What will the membrane potential be? That is, what is the strength of the battery here? Suppose we were to measure the potential with a pair of electrodes, which only exchanged K^+ with the fluids (similar to a pH electrode which only exchanges H^+). Since K^+ is unconstrained, it can move to come into equilibrium with any of the forces applied to it across the membrane. Thus, despite the concentration difference between inside and out, a K^+ electrode will measure no potential; for how can more K^+ flow in either direction when K^+ is at equilibrium with applied forces? Thus the membrane potential should be equal to that given by computing it from the difference in K^+ concentration, providing only that K^+ has no pump in its channel and has the same activity on both sides of the membrane. Alternatively one can say that a K^+ electrode pair across the membrane sees the potential of the concentration difference minus the potential of the difference in free energy across the membrane. If the two are in a steady-state equilibrium, the electrode pair will measure no potential difference. The same argument applies to Cl^-. But what will a pair of Na^+ electrodes measure? Since there is a pump operating, the potential across the membrane will depend on the electrode impedance, an unsatisfactory measure. Yet suppose there were a steady state set up by the pump-driven flux outward and the passive flux inward. The potential of the difference in free energy across the membrane, common to all channels, is that which is in equilibrium with the field of pump peculiar to the Na^+ channel alone. Thus, that field balances out the free energy difference potential with respect to the Na^+ channel, and the electrodes will record only the potential due to the concentration difference of Na^+ across the membrane. If some of the Na^+ leaks through channels not provided with a pump there will be an appropriate error. But, we do not have at present the good K^+ or Na^+ or Cl^- electrodes for intracellular work, the last because the reduction-oxidation potential of the living cell is enough to reduce Ag^+ or Hg^+ to the metallic state.

In practice, one measures membrane potential with a pair of pipettes filled with saturated KCl solution and connected electronically through reversible Cl^- electrodes to wires attached to a *vtvm*. Since K^+ and Cl^- have about the same ionic velocities, no error occurs, because neither ion tends to diffuse out faster than the other. At the same time, a very high concentration of K^+ and Cl^- at the tip of the pipette uncouples the ions in the fluid immediately around the tip so that they behave as if in much lower concentration; each being somewhat less dragged by the cloud of the other. With all such simplifications accepted it is still difficult to tell exactly what such an electrode pair measures. Each ion involved tends to have a net movement into or out of the pipette according to its concentration gradient. If the tip is very small in opening, compared to the relatively large body of solution in the electrode and substrate around the tip, the system comes to a more or less steady state at a particular potential across the tip, since neither the electrode nor the substrate is changed substantially by small flow of ions one way or the other. This steady state is complex to describe and depends somewhat on the geometry of the tip. Since the membrane has the aspect of a leaky capacitance held by the pump to a particular difference in free energy, the potential of which can be expressed as an ordering of charge across the membrane, this potential is freely communicated by the conducting electrolytes to the reversible electrode system, which has a much smaller leak across it than the resting membrane. However, this membrane potential is in series with the tip potentials, and many doubt that they are symmetrical in this situation. Nevertheless with such probes, the nerve membrane potential (and associated error) is seen to be about *80 mv*, inside negative, which is about what one would calculate from the concentration differences of the equilibrium ions, K^+ and Cl^-. The non-diffusable anions inside the cell do not contribute directly to this measure for they have an open circuit across the membrane. Na^+ is constrained by the pump, and, in any case, at this membrane potential has a very low conductance across the membrane, about *1/10* that of K^+. (Thus the membrane is much more sensitive to external changes of K^+ concentration than Na^+ concentration.)

The *80 mv* potential across the membrane corresponds to a field strength of the order of *100,000 v/cm*.

Are these ionic conductances fixed? No, as indicated earlier, they vary with membrane voltage, or at least those of K^+ and Na^+. Each of these conductances shows a profound voltage and time dependence when a voltage step is applied sharply across the membrane and clamped by an operational amplifier. Considering simply peak conductances, both are maximal at a membrane potential at about zero and decline steeply as this potential goes more negative. The Na^+ conductance declines more steeply than the K^+ conductance as a function of increasingly negative membrane potential and becomes the lesser of the two at about *−50 mv*. Both decrease still further if the membrane potential is driven more negative. Thus the membrane rectifies as you would expect. At its peak, the maximum Na^+ conductance is 10 times that of K^+ at the same time; whereas at rest, the K^+ is *10* times that of Na^+ at *−80 mv*. But the Na^+ conductance is even further complicated by having a *turn-off*. When the Na^+ influx sharply exceeds a certain rate, the channel acts as if there were a blocking capacitor which

[Continued on page 121]

SESSION VII—INVITED: Solid-State Sensing

THPM 7.3: Sensing Techniques for Space Research

G. H. Ludwig

Goddard Space Flight Center

Greenbelt, Md.

THE VALUE of earth satellite and space probes for gathering scientific information about the physical universe is well established. Since these spacecraft are very expensive, considerable thought must be given to the design of equipment on the spacecraft so that the greatest possible amount of information can be obtained about the phenomena to be measured.

Any experiment, no matter where it is conducted, may be thought of as a generalized system, as shown in Figure 1. The end elements are the basic sensors and the final report of results. The intermediate elements are the signal-conditioning instruments which convert the signals from the basic sensors into usable electrical quantities, the processing of these electrical quantities into a form which can be used for study by the experimenter, and the analysis of the data. In addition, for many experiments it is necessary to add storage in one or in several places. Storage may actually be a part of all the blocks in Figure 1. For example, if the sensor is a self-integrating ion chamber of the *Neher* type, it provides a storage function of its own. If the pulses appearing at the output of this chamber are counted, then this counter represents a second form of storage. A tape recorder is often incorporated into the signal conditioning and data reduction systems; placement of the reduced data on an oscillographic record or in tabular form can also be considered to be storage.

The major difference between the general outline shown in Figure 1 and an actual spacecraft system is the addition of a block representing the telemetering of the data from the spacecraft to the earth. This block can, in principle, be placed anywhere along the line of data flow. In general, the information bit rate along this line decreases as one progresses from left to right from unprocessed to more and more highly processed data. It must be remembered that the experimenter will see his data for the first time at the output of the telemetry system. The factors which determine where the telemetry system should be placed along the line of data flow for any specific experiment include:

(1)—Ability of the experimenter to predict results. If the experimenter knows where in the possible range of values his results will occur, he may arrange for considerable processing in the satellite before he sees these data. If, for example, he is interested in the energy spectrum of protons in the cosmic ray flux, and if he already has a general knowledge of the energy spectra of all other constituents, he might concentrate on the protons and reject all other particles. He might include a computer in the spacecraft to determine an analytic function that would represent the spectrum. Then he would need to telemeter only a set of coefficients rather than an extensive set of data points. On the other extreme, if very little is known about the phenomenon it may be necessary to telemeter all data directly from the sensor and then, after a preliminary investigation of the raw data on the ground, to determine how they should be conditioned and processed.

(2)—Information bandwidth available for data transmission. Obviously, the first alternative discussed under *(1)* would require far less information bandwidth than the second.

(3)—System reliability. The larger the amount of data processing in the spacecraft, the greater the complexity and the smaller the reliability of the system. If the experimenter were to telemeter only the foregoing coefficients, he would need to have a high degree of confidence in his instrumentation.

(4)—Time available for the preparation of the experiments. Complex spacecraft data processing systems require a long time for development and calibration.

Obviously, the best location along the line of data flow for placement of the telemetry system can vary widely, even among experiments on the same spacecraft. Thus, any acceptable central spacecraft data handling system must be carefully designed to permit the necessary flexibility.

On spacecraft containing more than one experiment, the signal conditioning instrumentation is often split into two sections. The first consists of the detectors and the circuits which process their outputs up to the point where the central system combines the data from a number of experiments. The second section includes the instrumentation in the central system, which may further process and store the data before transmission. As attempts are made to measure the characteristics of the phenomena in greater and greater detail, more and more data processing in the spacecraft before transmission will become necessary. This trend is expected to continue to the point where programmable computers will be used aboard the spacecraft to perform complex analyses. Such applications will become important because on-board computers will require less payload weight than would be required to telemeter very large quantities of raw data, and conservation of ground receiving station capabilities and data reduction facilities will be necessary.

The role of the sensor and its immediately-associated electronics is to convert a physical parameter into an electrical quantity which can be accepted by a control spacecraft data system for eventual transmission over a telemetry link. It is necessary that:

(1)—Telemetry be accomplished within the smallest information bandwidth practicable.

(2)—Instrumentation meet the requirements of ruggedness, relatively low operating power, lightweight, and relatively small volume imposed by the launching vehicle capabilities and the launching environment.

(3)—Instrumentation be reliable while operating unattended for long period in the space environment.

(4)—Since very large quantities of data will be gathered, the data form should be such that direct entry into computers for machine processing on the ground is possible.

Investigation of many different physical phenomena in space have been or are being undertaken. These include studies of the atmospheres and ionospheres of

the earth and other planets, magnetic fields and energetic particles, solar physics, galactic and extragalactic astronomy, and the physical characteristics of the moon and planets. Many sensors and signal-conditioning systems have been developed for these investigations.

To give some impression of the diversity of instruments being prepared for present satellites and the detector techniques currently employed, the experiments to be carried on the first *Orbiting Geophysical Observatory* are listed in Table I. This satellite will be launched in late 1963 into a highly eccentric orbit (apogee at 17 earth radii) to conduct investigations of the earth's atmosphere and ionosphere, energetic particles, magnetic fields, solar physics, and astronomy. Of course, this single program involves only a fraction of our total effort in space research. But it is representative of the spacecraft being used at the present time.

Experiment Title	Principal Experimenter	Phenomena to be Measured
Solar Cosmic Rays	K. A. Anderson, University of California	Solar proton and x-ray flux, energy and variations
Plasma, Electrostatic Analyzer	M. Bader, Ames Research Center	Solar plasma flux, energy and direction
Plasma, Faraday Cup	H. J. Bridge, Massachusetts Institute of Technology	Solar plasma flux, energy and direction
Positron Search and Gamma Ray Spectrum	T. L. Cline and E.W.Hones, Goddard Space Flight Center and Institute for Defense Analysis	Search for positrons and solar gamma ray flux and spectrum
Trapped Radiation Scintillation Counter	L. R. Davis, Goddard Space Flight Center	Geomagnetically trapped electron & proton flux, energy and direction
Cosmic Ray Nuclear Abundance	F. B. McDonald, Goddard Space Flight Center	Primary and solar cosmic ray flux, charge and energy
Cosmic Ray Spectra and Fluxes	J. A. Simpson, University of Chicago	Primary and solar cosmic ray flux, charge and energy
Trapped Radiation, Omnidirectional Counters	J. A. Van Allen, State University of Iowa	Geomagnetically trapped electron and proton flux and energy
Trapped Radiation, Electron Spectrometer and Ion Chamber	J. R. Winckler and R. L. Arnoldy University of Minnesota	Geomagnetically trapped electron energy and flux, and total ionization
Rubidium-Vapor and Flux Gate	J. P. Heppner, Goddard Space Flight Center	Magnetic field strength and direction
Triaxial Search Coil Magnetometer	E. J. Smith, Jet Propulsion Laboratory	Magnetic field low frequency variations
Spherical Ion and Electron Trap	R. Sagalyn, A. F. Cambridge Research Laboratory	Thermal charged particle density, energy, and composition.
Planar Ion and Electron Trap	E. C. Whipple, Goddard Space Flight Center	Thermal charged particle density, energy, and composition
Radio Propagation	R. S. Lawrence, National Bureau of Standards	Electron density
Atmospheric Mass Spectrum	H. A. Taylor, Goddard Space Flight Center	Atmospheric composition
Interplanetary Dust Particles	W. M. Alexander, Goddard Space Flight Center	Micron dust particle velocity and mass
VLF Noise and Propagation	R. A. Helliwell, Stanford University	VLF terrestrial noise, solar particle emissions, and cosmic noise frequency distribution and strength
Radio Astronomy	F. T. Haddock, University of Michigan	Solar radio-noise burst frequency spectrum
Geocoronal Lyman-Alpha Scattering	P. Mange, Naval Research Laboratories	Lyman-Alpha intensity
Gegenschein Photometry	C. L. Wolff and K.L. Hallam, Goddard Space Flight Center	Gegenschein intensity and location

***TABLE 1*—Experiments to be conducted on the first Orbiting Geophysical Observatory.**

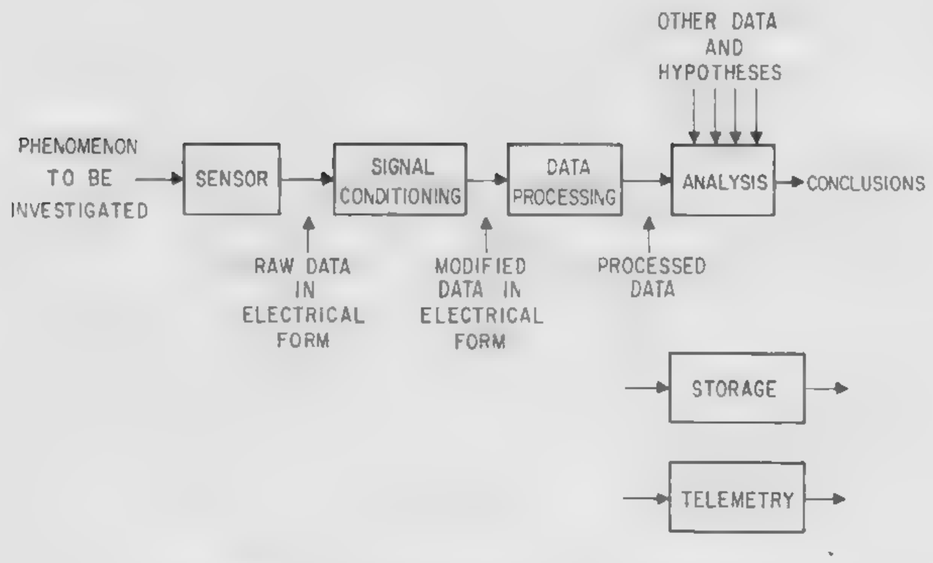


***FIGURE 1*—Elements of an experiment.**

SESSION VIII: Digital Design Techniques

Chairman: P. B. Myers

Martin Marietta Corporation

Baltimore, Md.

THPM 8.1: Specifying Transistor Characteristics for Worst-Case Switching Circuit Design

W. D. Roehr

Motorola Semiconductor Products, Inc.

Phoenix, Ariz.

Worst-case design of transistor switching circuits can be accomplished conveniently by using limit curves and equations. A germanium epitaxial mesa transistor-operated common emitter is an illustration.

To keep a transistor cutoff (i.e., $I_C \approx I_{CBO}$) the input circuit must maintain a minimum reverse bias V_T on the base to prevent emitter injection, while allowing for a base leakage current I_{BL} to flow; Figure 1.

A condition can exist where the collector voltage fails to return to the supply potential upon turnoff, but returns instead to some stable point in the transistor avalanche region. This phenomenon‡ depends upon the load loci and switching speed and may be avoided if empirical limits are given as shown in Figure 2.

The saturation region must be thoroughly defined for the designer to effect a suitable compromise between saturation voltage and current gain. Figures 3 and 4 and a curve of h_{FE} versus current at several temperatures (not shown) define the *on* condition. The position of the curves of Figure 3 shifts with temperature, although their general shape remains relatively constant. This fact permits curves to be drawn for any current and temperature by obtaining two points from the following equations:

Point 1	*Point 2*
$V_{CE} = V + R\,I_C$	V_{CE} - voltage specified for h_{FE}
$I_B = I_C/K$	$I_B = I_c/h_{FE}$

Point *1* is deep in the saturation region $\left(K \leq \frac{h_{FE}}{2.5}\right)$

so that changes in h_{FE} have negligible effect upon V_{CE}. Point *2* is at the edge of the saturation region where V_{CE} has negligible effect upon h_{FE}.

There are four transient condition characteristics to consider: delay time, rise time, fall time and storage time.

Delay time t_d is the time required to remove the charge Q_{OB} due to off bias V_{OB} from the input C_{ib} and output C_{ob} capacitances. Q_{OB} may be found by graphically determining the area under the curves of C_{ib} and C_{ob} versus voltage.

Rise time t_r is the time required for the input circuit to supply the following charges:

(1)—Q_I, due to I_C. $Q_I = I_C/\bar{\omega}_\tau$, where $\bar{\omega}_\tau$ is the large signal average gain bandwidth product.

(2)—Q_V, due to C_c, $Q_V = V_C\,\bar{C}_c$, where $\bar{C}_c$ is the large signal average collector capacitance.

(3)—Q_R, the charge lost by recombination during the rise time interval.

Since Q_R is dependent upon h_{FE}, its effects must be made negligible to find Q_I and Q_V. This is done by making the test circuit input current step

$$I_{B1} > 5\,\frac{I_C}{h_{FE}}$$

and we may write

$$Q_{IN} = I_{B1}t_r = Q_I + Q_V = I_c/\bar{\omega}_\tau + V_c\,\bar{C}_c$$

With a resistive load, $R_L = V_C/I_C$ we find

$$t_r \quad I_C\,\frac{\frac{1}{\bar{\omega}\tau} + R_L\,\bar{C}_c}{I_{B1}} \qquad (1)$$

For the normal *90%* rise time all transistor charge and hence t_r carries the factor *0.9*. It is convenient to regard $.9\ (1/\bar{\omega}_\tau + R_L\bar{C}_c)$ as a time constant τ_A, describing the active-region response. It will be noted that $Q_I + Q_V = \bar{\tau}_A I_C$. $\bar{\tau}_A$ is easily found from a measured *90%* rise time by solving $\tau_A = t_r\,I_{B1}/I_C$ and usually is fairly independent of operating point as Figure 5 shows.

Fall time t_f is simply the inverse process of rise time in which case recombination aids turn-off; τ_A therefore applies.

Storage time is the time required for the excess charge Q_X, due to overdrive current I_{BX}, to exit from the transistor. This charge can be found by measuring the amount of total turn-off charge Q_T stored on a *speed up* capacitor and using:

$$Q_T = Q_X + \tau_A\,I_C \qquad (2)$$

Knowing τ_A, equation *(2)* may be used with Figure 6 to find Q_T at any point.

It is well accepted that a storage time constant $\tau_S = Q_X/I_{BX}$ may be defined. For input conditions resulting in a step function of reverse base current, I_{B2}, two conditions exist depending upon whether storage is predominately in the base or the collector.

Base Storage	*Collector Storage*
$t_s = \tau_s\,\frac{I_{B1} + I_{B2}}{I_C/\beta_o + I_{B2}}$ *(3)*	$erf\ \sqrt{t_s/\tau_S} = \frac{I_{B1} + I_C/\beta_o}{I_{B1} + I_{B2}}$ *(4)*

where β_o is the value of h_{FE} at the edge of saturation.

No suitable equations for t_s have been developed, when significant charge is stored in both base and collector regions. This fact, however, does not impair the importance of Q_T for the optimizing of circuit capacitors or for use as a general figure of merit.

‡ Latch-up.

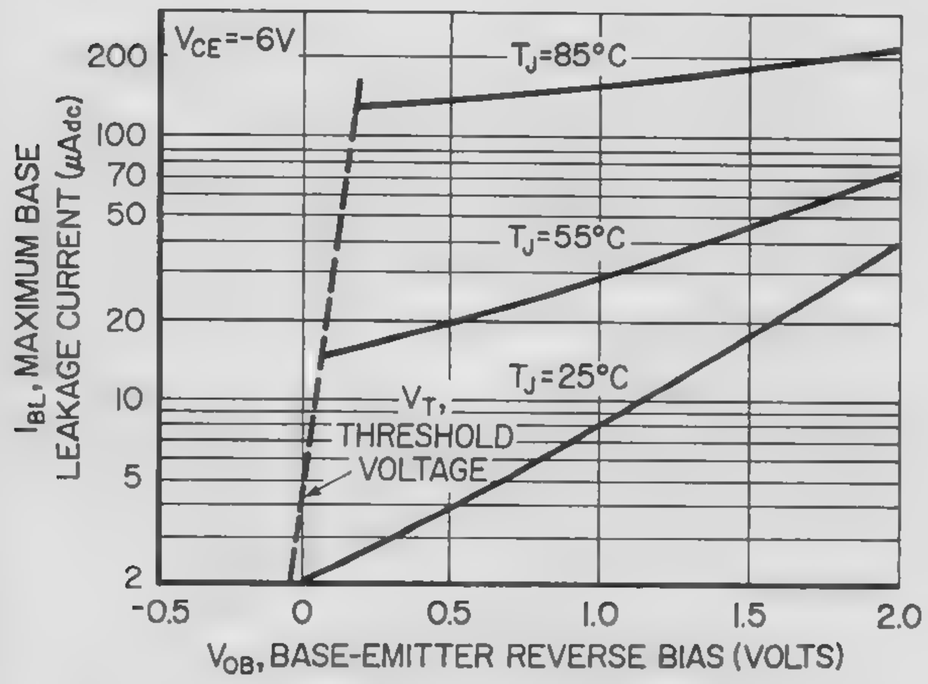


FIGURE 1—**Base leakage characteristics showing the large surface contribution (typical of diffused base alloyed emitter transistors) which must be accounted for in timing circuits.**

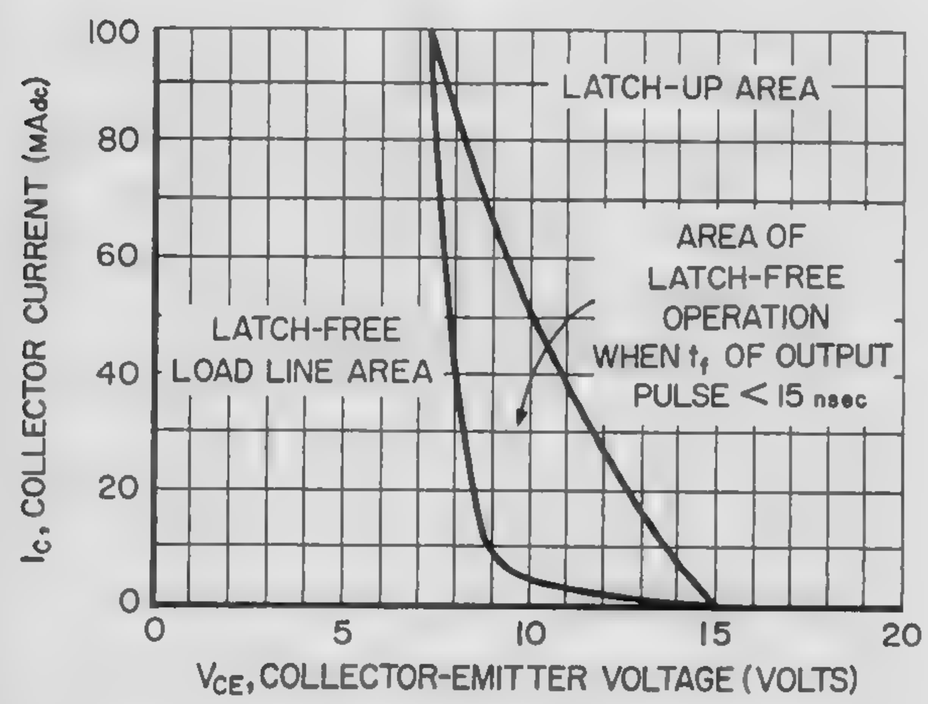


FIGURE 2—**Area of permissible load loci. Chart permits designer to avoid *latch-up* which can occur when V_{CE} exceeds BV_{CEO}.**

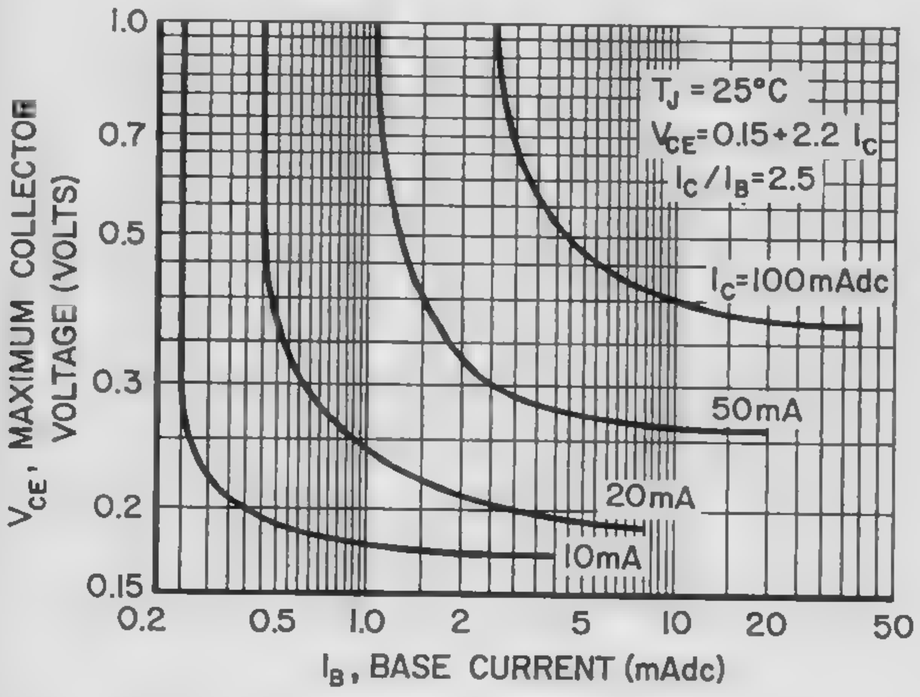


FIGURE 3—**Collector-emitter saturation region curves that serve to provide a guide for construction of curves at any current and temperature.**

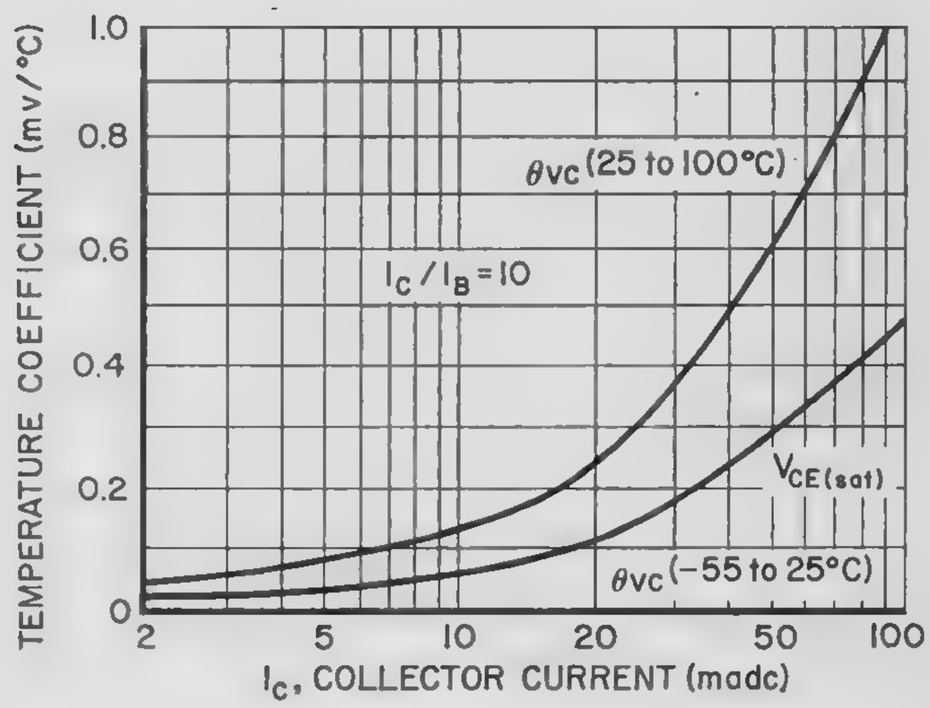


FIGURE 4—**Temperature coefficients apply to saturation region curves under all conditions: effects of current gain are superimposed.**

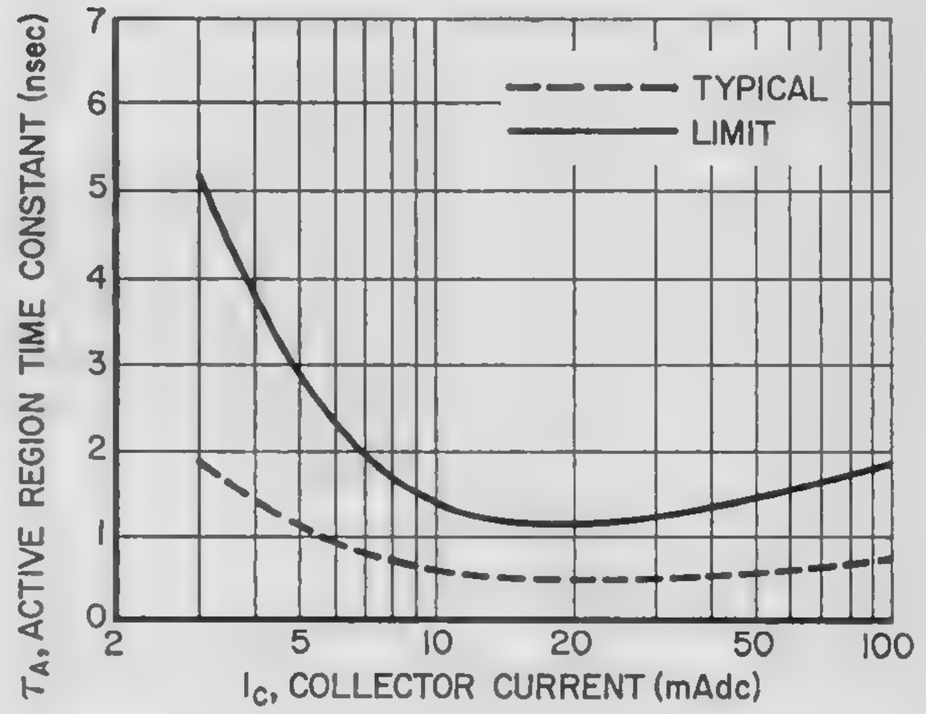


FIGURE 5—**Active region time constant that can be used to compute the charge required in the rise and fall time intervals.**

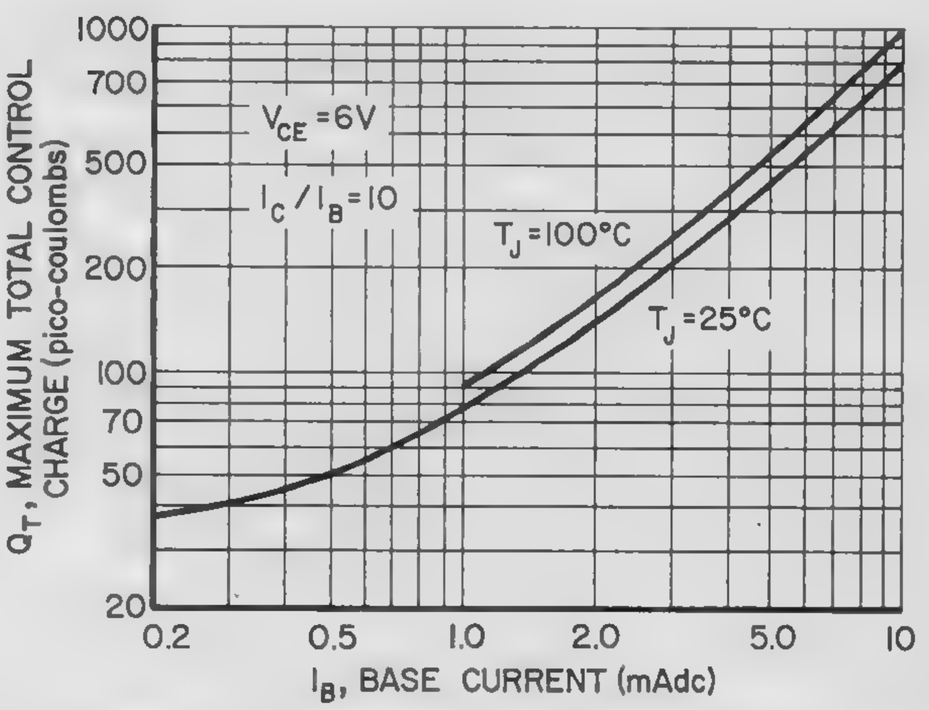


FIGURE 6—**Control-charge data which permits optimum choice of *speed up* capacitors and calculation of storage-time constant.**

SESSION VIII: Digital Design Techniques

THPM 8.2: Method of Using Parameter Confidence Limits in Circuit Design

L. J. Ragonese

Electronics Laboratory, General Electric Company

Syracuse, N. Y.

A RELATIVELY straightforward procedure for arriving at the circuit design which will have the maximum probability of drift-free (e.g., error-free) operation for any particular system has been evolved. Known as the *parameter confidence design method*, it presumes a digital circuit application which involves: *(1)*—a fixed number of building blocks of any particular topology; *(2)*—a maximum required frequency of operation; *(3)*—a specified fan-in fan-out requirement; *(4)*—a fixed thermal packaging scheme; *(5)*—the use of components whose relevant parameter distributions are known; and *(6)*—the existence of a minimum power dissipation *worst-case* design procedure for the particular topology*.

Since the pre-selection of individual components is either impossible or undesirable in microelectronics, individual parameter values are most likely described by non-truncated gaussian-like probability density distributions.

In microelectronics, substantial temperature differences can be expected within a system as circuits are packed ever more closely together. Due to non-zero temperature coefficients, the effective probability distributions of individual parameters within a system show increases in standard deviation as a result of temperature differences. As a result, digital circuits of a given topology, which are each designed to fulfill the same probability of drift-free operation under succeedingly more severe ranges in system temperature, are found to dissipate at an ever-increasing rate. The temperature range within any particular physical system varies at best linearly, but usually at an ever-increasing rate, with per-circuit power dissipation.

The design method consists of three independent steps: mapping the circuit realizability plane, establishing the physical system thermal characteristic, and combining the results of the first two steps to arrive at the optimum design having the least probability of drift failure.

The mapping of the realizability plane requires the carrying out of an arbitrary number of *worst-case* minimum-power-dissipation circuit designs, where the *worst-case* parameter limits are selected in an unconventional fashion described below.

In the terminology of statistics, the limits which contain a parameter with a probability of $x\%$ are called the $x\%$ *confidence limits* for the parameter. The continuum of parameter values between the confidence limits is called the *confidence interval*. While there are, in general, many possible $x\%$ confidence intervals associated with any distribution, consideration here is restricted to those of minimum length. The *degree of confidence* is represented by $\triangle$. Thus in Figure 1, the parameter values between *.83 R* and *1.17* R are called the 80% confidence interval values, and the degree of confidence for that interval is 80%.

The *parameter confidence design method* hinges on the hypothesis that the probability of drift-free system operation is an ever-increasing function of the degree of confidence that the individual parameters are within their design limits. This is powerful in that the optimum circuit design is established without having to establish the probability of drift-free circuit operation.

The actual mapping procedure is carried out as follows:

(1)—Given: a particular digital circuit topology with specified maximum switching speed, fan-in fan-out requirements; end of life component probability distribution data for all relevant design parameters at several discrete temperatures within the range of interest; e.g., *20°C*, *40°C*, etc.

(2)—Arbitrarily design a minimum dissipation *worst case* circuit using the *99.99%* upper confidence limit at *40°C* and the lower *99.99%* confidence limit at *20°C* as the two *worst-case* limits. (These would be about *1.38 R* and *.72 R*, respectively, in Figure 2.) Calculate the average circuit dissipation and plot at *40°C* on a circuit dissipation versus temperature graph.

(3)—Repeating the process for maximum temperatures of *20, 60, 80, 100* and *120°C* results in the establishing of the *99.99%* line in Figure 4.

(4)—Repeating the procedure of *(2)* and *(3)*, but using corresponding confidence limits establishes the lines labeled *99.95%; 99.9%, etc.*

Thus, a continuum of possible circuit designs, each optimally fulfilling different operating conditions, is mapped.

Consider a digital machine composed of a number of similar circuits imbedded in some mechanical packaging system. The maximum temperature within the system increases as the power dissipated by the individual circuits increases. A graph of the variation in maximum system temperature, as a function of per-circuit dissipation, shall be defined as the *system thermal characteristic*. The characteristic is purely a function of heat conductivities, system geometry, number of heat sources, and perfectness of heat sink. In Figure 4, the dashed lines represent the thermal characteristics of four different systems: *A*, *B*, *C*, and *D*. The intersection of each system thermal characteristic and the realizability plane represents the minimum dissipation circuits which have been specifically designed for the temperature range of the specific system. Points *a*, *b*, *c*, and *d* in Figure 4 represent the designs which will have a minimum probability of drift failure in their respective systems.

* Reference *(6)* refers to a procedure by which is determined the minimum value of power dissipation sufficient to maintain proper operation of the circuit, despite an excursion of the parameters to some given extreme set of values.

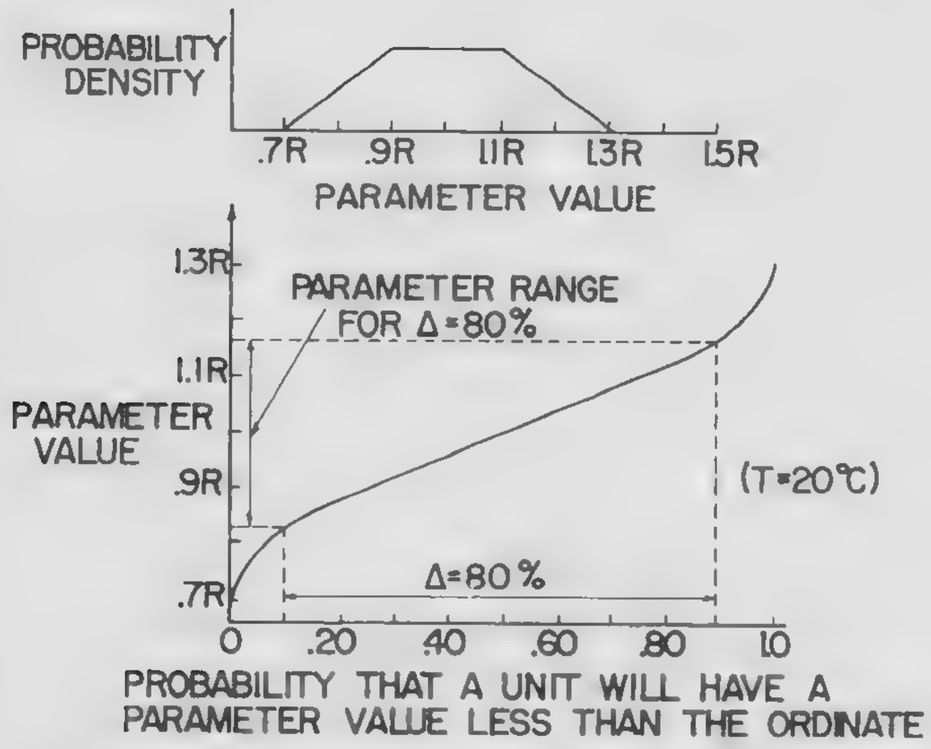


FIGURE 1—Probability density, probability distribution, and degree of confidence for a typical parameter. Skewed and non-truncated density functions can be similarly handled.

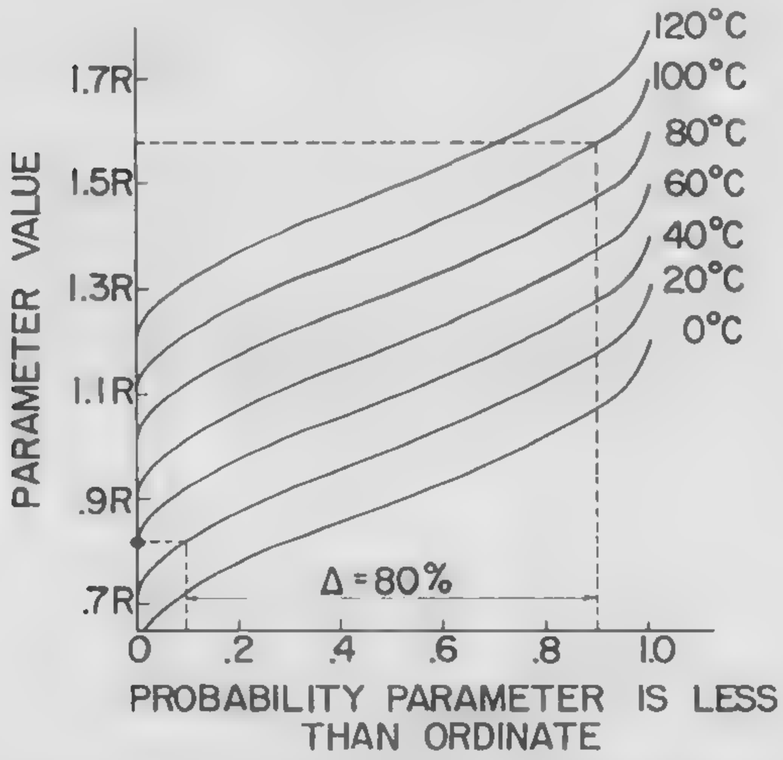


FIGURE 2—Idealized probability distribution functions for the same parameter at different temperatures.

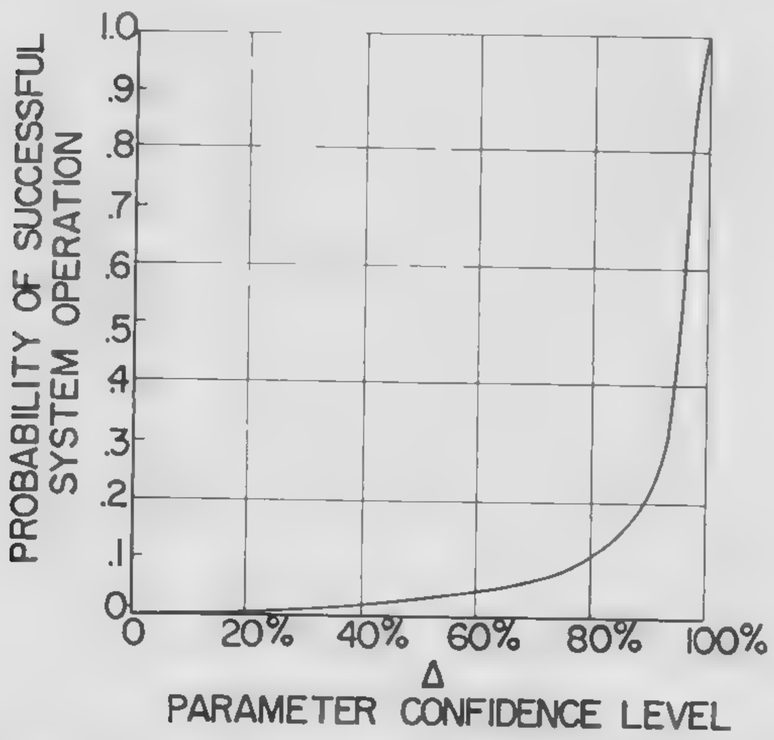


FIGURE 3—The probability of successful system operation is an ever-increasing function of parameter confidence level.

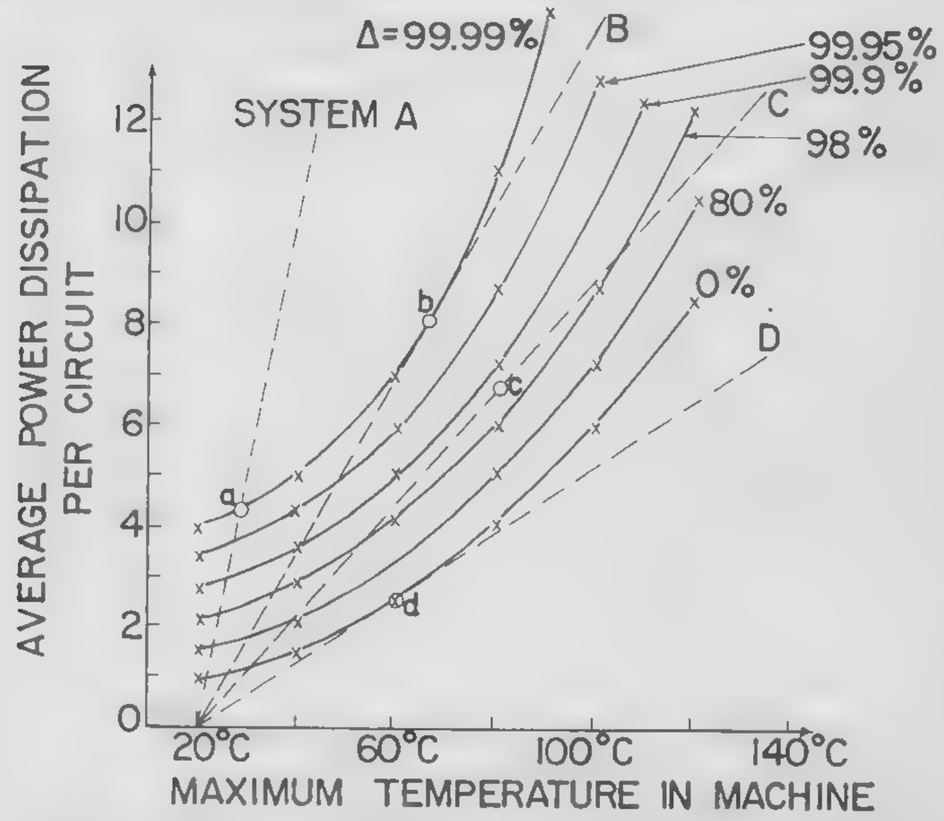


FIGURE 4—A representative realizability plane mapping with superimposed thermal characteristics for systems *A*, *B*, *C*, and *D*. Ambient or heat sink temperature is *20°C*.

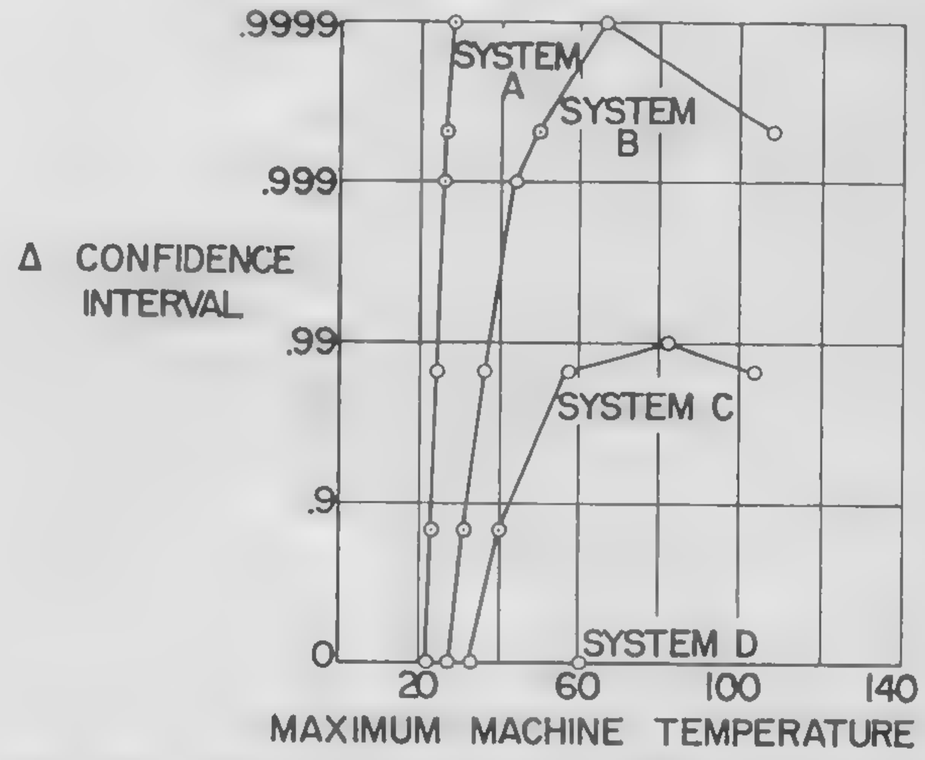


FIGURE 5—Degree of parameter confidence as a function of maximum system temperature. This information was obtained directly from Figure 4.

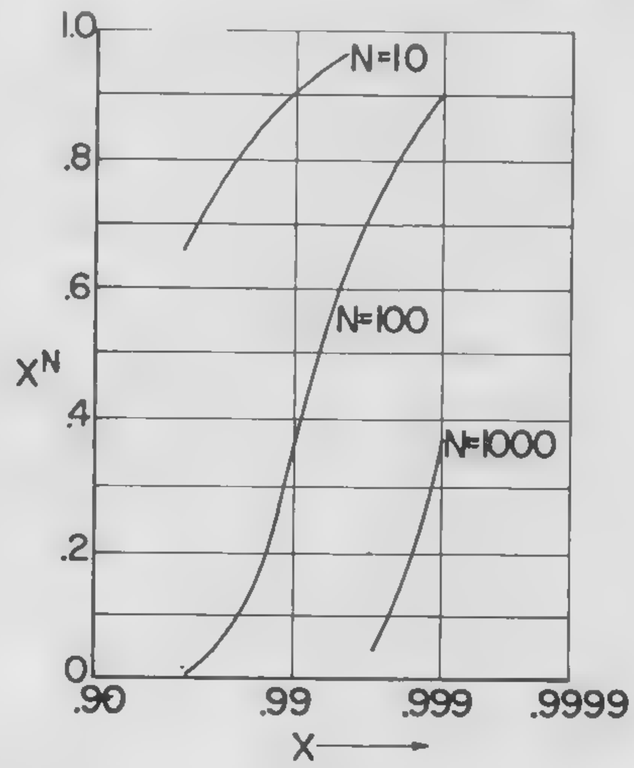


FIGURE 6—The effect of number of simultaneous events on the cumulative probability of success.

SESSION VIII: Digital Design Techniques

THPM 8.3: Synthesis of Electronic Bistable and Monostable Circuits*

L. O. Hill, D. A. Hodges, D. O. Pederson, R. S. Pepper**

Electronics Research Lab., University of Calif.

Berkeley, Calif.

For ACTIVE DEVICES, which in themselves are not potentially bistable, a synthesis procedure can be developed to generate the *dc* circuit configurations of bistable circuits. In this procedure, a device is modeled as a *2*-port or a *3*-terminal controlled resistance (conductance). As an example, the controlled-*G* model of an *npn* transistor is shown in Figure 1. The controlled-*G* model provides a close representation of the output I_c-V_c characteristics for the *off* and saturated states which are of greatest interest here. The controlled-*G* curve for this transistor is monotonically increasing and is labeled a class-*I* type. If a unipolar transistor is modeled in a similar manner, as shown in Figure 2, the controlled-*G* curve is monotonically decreasing and is labeled class *II*. As illustrated in Figures 1 and 2 the direction of actual current flows, and corresponding node pair voltages are defined as positive.

To generate a bistable circuit, general *3*-terminal controlled-*G* models are used for the active devices without initial assignments of class or polarity restrictions. If all possible connections of two *3*-terminal controlled-*G* models, and a resistance and a voltage source are made, *114* distinct configurations result. By the use of duality, interchange and by checking for independent control, these *114* configurations can be reduced to six possible configurations and their duals. At this point, it is convenient to establish polarity and controlled-*G* class restrictions for each basic configuration. If now actual devices are considered, many of these six configurations must be eliminated. For a restriction to bipolar and unipolar transistors (of both polarity types), modeled as in Figures 1 and 2, only one basic configuration and its dual are possible. These two configurations are shown in Figures 3*a* and *c*. The configuration of Figure 3*a* must use class-*II* devices, and a direct substitution of unipolar transistors leads to the complementary unipolar circuit of Figure 3*b*. The configuration of Figure 3*c* must use the dual of class *II*, i.e., class-*I* devices. Substitution of bipolar transistors leads to the usual bipolar equivalent of the *pnpn* device.

Other possible bistable circuits are generated from the two configurations of Figure 3 by converting devices from class *I* to class *II* or vice versa. This is done through the addition of voltage and current sources to the device as shown in Figure 4. As an example, a voltage source, V''_o, and a current source, I''_o are added to the output of a bipolar transistor in Figure 4*b*. New output variables, I'_2 and V'_2, are defined to maintain the positive labeling of actual current flow. The two sources provide the I'_2-V'_2 characteristic shown in Figure 4*c* and the controlled-*G* model shown in Figure 4*d*. It will be noted that both the class and current polarity restrictions of the model have been changed. To cite an example, a converted *npn* bipolar transistor can be used in place of an *n/p* unipolar transistor.

If both input converted and output converted bipolar transistors are used in the configuration of Figure 3*a*, the current switching (*Schmitt* type) circuit of Figure 5*a* is obtained. Similarly, if other sequences of converted devices are used, a total of 20 bistable circuits are generated from the configurations of Figures 3*a* and *c*. Polarity complements are not included. Three more circuits are shown in Figures 5*b*, *c* and *d*.

As an alternate procedure, the configuration can be converted as in Figure 6*a*. Here, R_L and V have been divided in two. The center point for identical devices is then at ground, and the configuration can be considered to have two separate parts. In one of these parts, we are now free to change the polarity of the supply. This, in turn, changes the class and polarity requirements of the controlled-*G* models to achieve bistability. For the case of Figure 6, *npn* transistors must be used, and the basic transistor *Eccles-Jordan* circuit results. Using converted devices in the converted configuration leads to unipolar or unipolar-bipolar versions of the circuit. (The *Eccles-Jordan* circuits can also be generated from Figures 5*a* and *c* by proper circuit grounding and manipulation.

A synthesis procedure to develop configurations of monostable circuits starts from the above bistable configurations. We first develop the *I-V* characteristic at all node pairs which may be created by soldering iron or pliers entry. The *I-V* characteristic at the port includes all *dc* sources and resistances and may be called a *4*-point characteristic, since in the large it can be char-

[Continued on page 122]

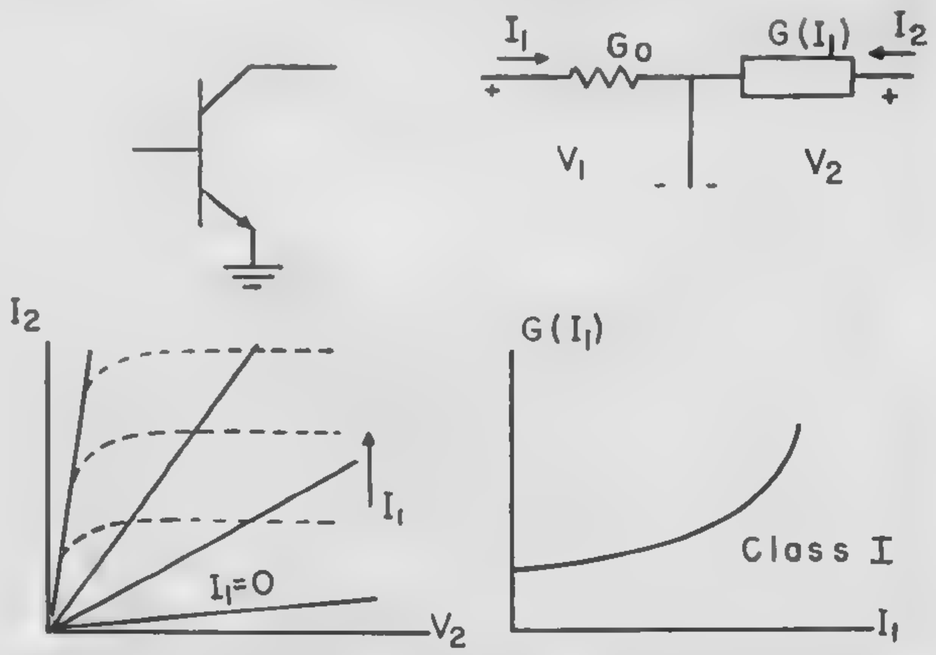


FIGURE 1—**Controlled-conductance model of the *npn* bipolar transistor, common-emitter connection.**

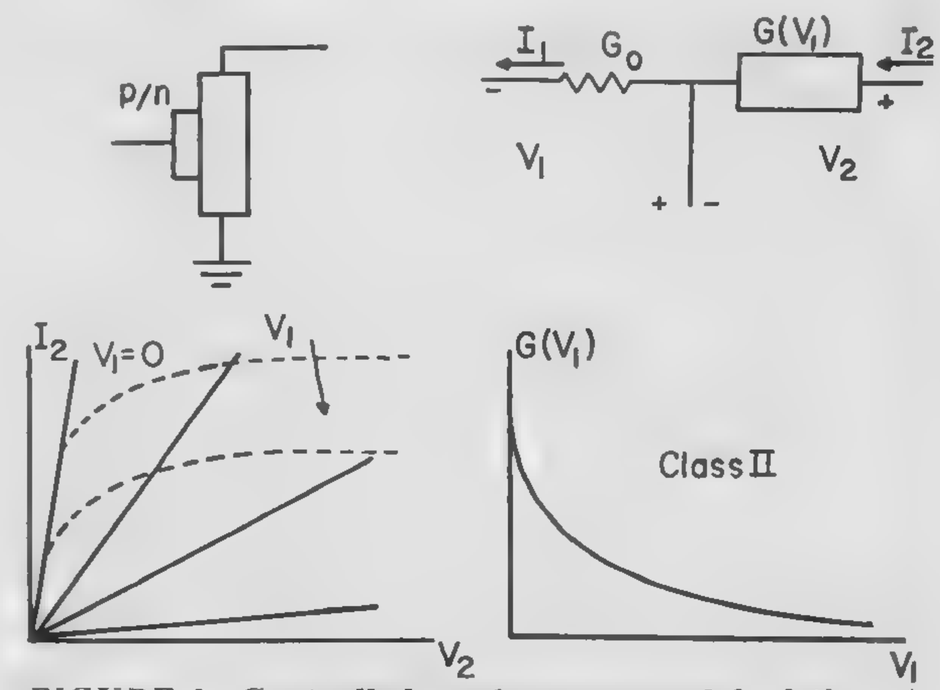


FIGURE 2—**Controlled-conductance model of the *p/n* unipolar transistor.**

* This work was supported in part by the Electronic Technology Laboratory, AF Systems Command.

** Now with Astroelectronics Laboratory, Westinghouse Electric Corp., Newbury Park, Calif.

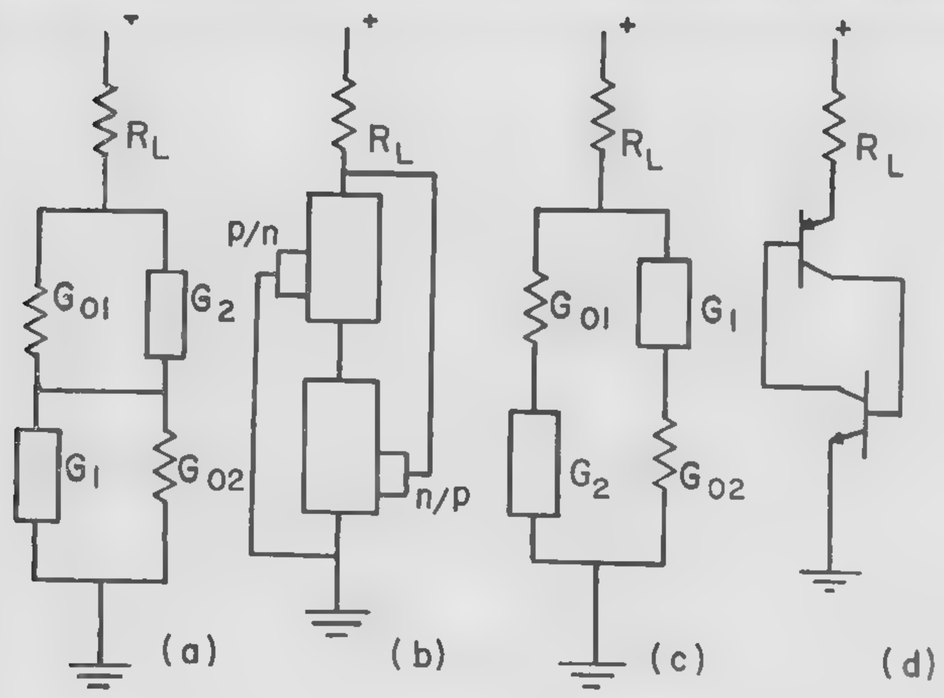


FIGURE 3—The basic configurations for bipolar and/or unipolar transistor bistable circuits.

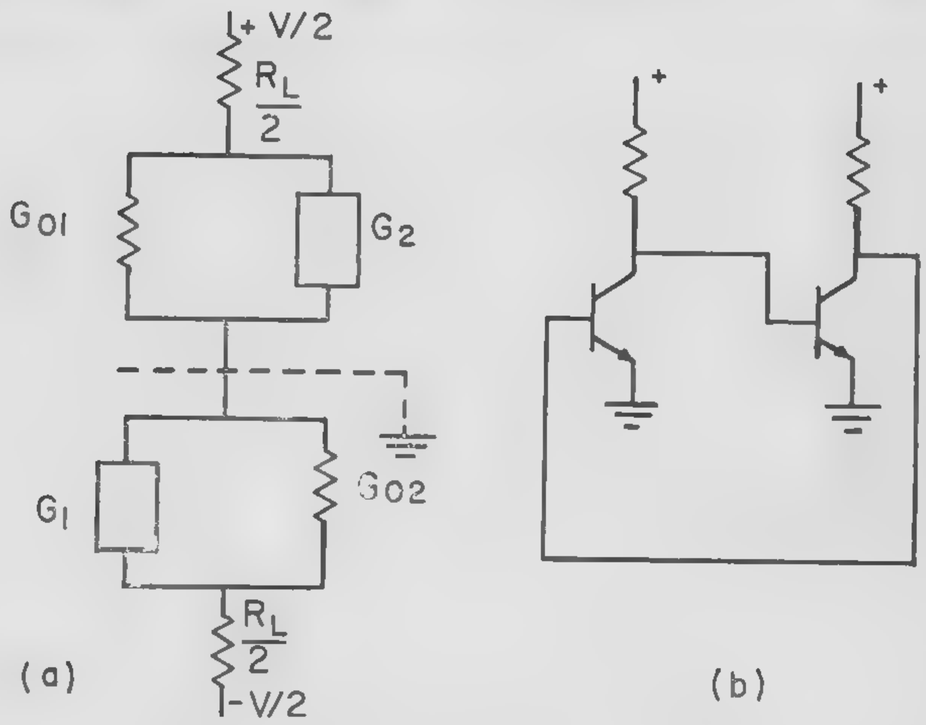


FIGURE 6—Development of the *Eccles-Jordan* circuit.

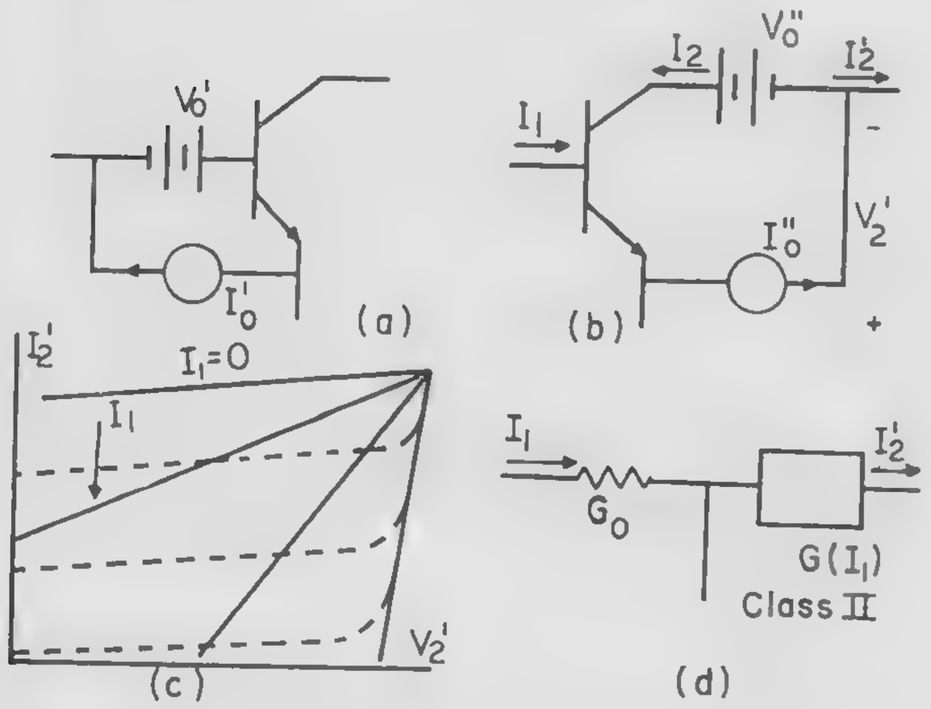


FIGURE 4—Class and polarity conversions of bipolar transistors.

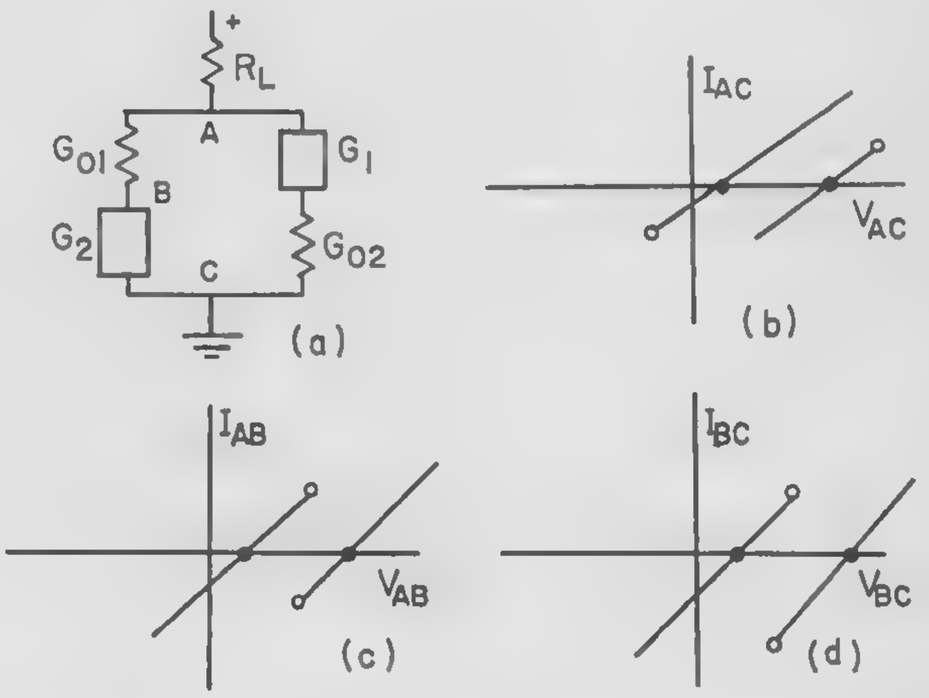


FIGURE 7—Four-point characteristics of a bistable configuration.

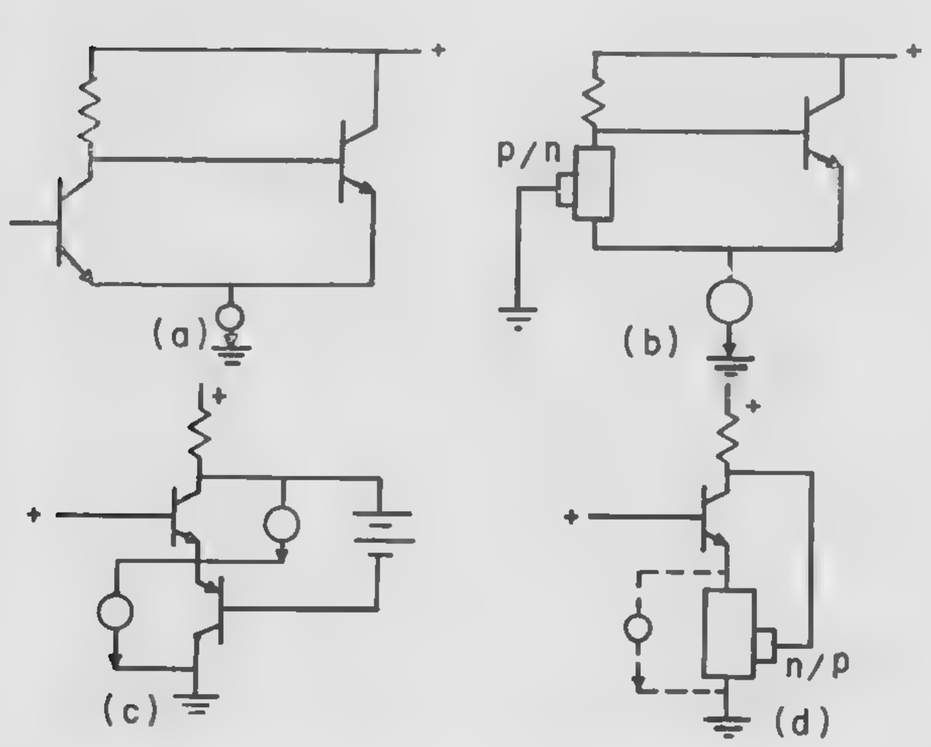


FIGURE 5—Representative bipolar and/or unipolar bistable circuits.

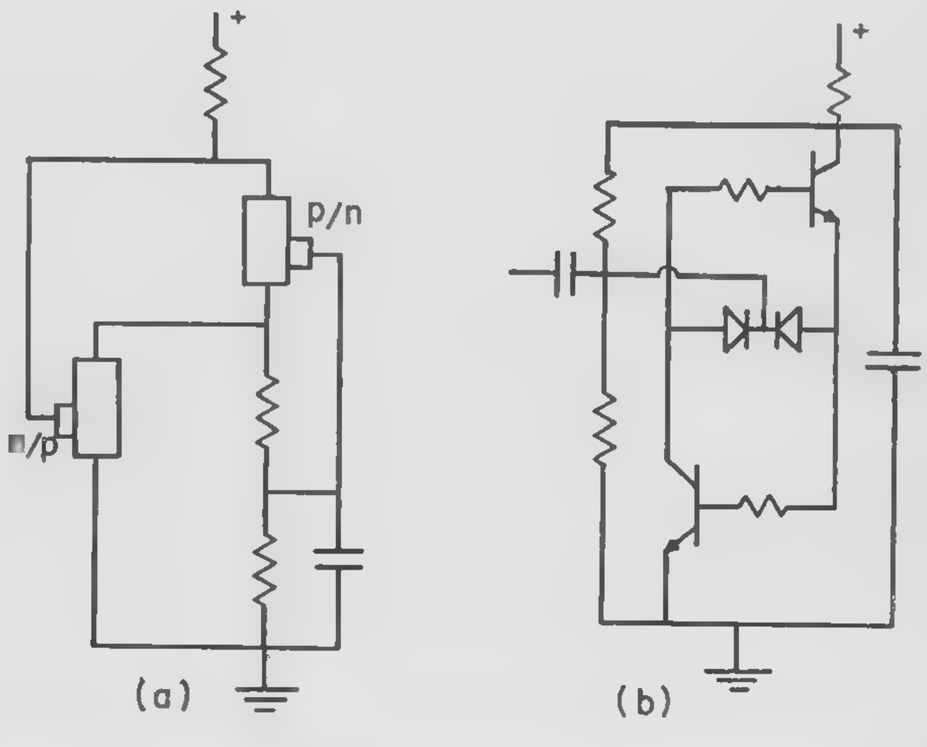


FIGURE 8—(a): Unipolar, monostable circuit. *(b):* A bipolar, bistable circuit with the counting property.

SESSION VIII: Digital Design Techniques

THPM 8.4: The Application and Realization of Threshold Logic‡

S. B. Akers, Jr. and B. H. Rutter

Electronics Laboratory, General Electric Company

Syracuse, N. Y.

During the past few years, there has been an increasing amount of interest in the area of threshold logic. Interest has spread into such diverse fields as logic design, pattern recognition, and bionics. This is due to the wide logical versatility of the threshold gate, the possibility of using the variable-weight feature in self-organizing systems, and the close correspondence between the operation of the threshold gate and that of the neurons in the brain.

The logical operation of the threshold gate is shown in Figure 1. Each of the N binary inputs has a numerical weight (positive or negative) associated with it, and the output of the gate is *1*, if and only if the weighted sum of these inputs is at least as great as the numerical threshold, T. Figure 2 shows how four threshold gates may be interconnected to realize the *15*-input parity function, i.e., the function which is *1* if and only if the number of *1's* on the inputs is odd[1].

If all four outputs of the gates in Figure 2 are considered, the circuit becomes a *unary to binary* converter, i.e. the *4*-bit output F_3-F_2-F_1-F_0 is the binary representation of the number of *1*'s on the inputs. An equivalent realization of this circuit with *and* gates and *or* gates would take literally hundreds of gates. By introducing appropriate time delays with feedback (Figure 3), it is also possible to convert this circuit into a twelve-input serial adder. (In general, any n-input serial adder can be realized with at most $(\log_2 n + 1)$ threshold gates.)

Until recently, the circuit designer has been limited to fan-in and fan-out values (usually less than *10*) which could not readily utilize the advantages of threshold logic. Presently available tunnel diodes appear to have sufficient precision (better than *1%*) and are low enough in cost to permit their use in threshold gates with fan-in and fan-out considerably in excess of *10*.

Since the gate must also have gain and isolation between input and output, a transistor may be used; Figure 4. As the input current increases from zero, the diode is in a low voltage state and the transistor is *off*. When the current exceeds the peak current i_p, the diode switches to a high-voltage low-current state, and the transistor turns *on*. Each input that is a binary *1* generates a current equal to the weight of that input times some unit current, $W_k i_u$, and when the sum of $W_k i_u$ is greater than the peak current i_p, the output switches. Figure 5 shows a simple majority logic gate which thresholds when the number of energized inputs is $(N + 1)/2$ or greater, where N is an odd number. This gate has inherent inversion because of the transistor.

Correct operation of the gate requires that the peak current lie between the input current levels corresponding to a majority and a minority excitation; Figure 6. This leads to the result that the total error due to all variations must not exceed $\pm(100/N)\%$. Two major sources of error are variations in the input current (due to changes in supply voltage and input resistors) and variations in the diode peak current, which contribute directly to the total error. Other factors, such as changes in the diode *dc* resistance at the threshold (due to the peak changing) or in the effective source resistance do not appear directly, but are reduced by the ratio of diode to source resistance. If a stage is not a perfect voltage source (R_L not zero), other stages fed by it will interact somewhat. This contributes to a constraint on the minimum supply voltage which can be used. Other restrictions on the supply voltage and resistance values are created by the *initial conditions* of tunnel-diode peak current i_p, minimum transistor β, maximum transistor current capability, and the fan-in and fan-out N. The exact choice of design parameters is determined by the consideration of power dissipation. For a given set of *initial conditions* there are proper values of voltage and resistance which result in minimum power.

The analytical results indicate that a majority gate with fan-in and fan-out of *51* is feasible. This figure appears to be near a practical limit, considering the limitations of presently available components. The power dissipation varies almost directly with the peak current of the tunnel diode; about *700 mw* for *10 ma* and less than *100 mw* for *1 ma*. A *51*-input gate has been operated. To test the operation of threshold logic gates in combination with each other, the unary-binary converter of Figure 2 was constructed. In general, any negative weight may be simulated by inverting the input and changing the threshold. The last stage, with *29* inputs, was found to be the most critical, and thus determined the basic error limitations.

One disadvantage of the tunnel diode is its hysteresis; once it has switched it has to be reset before new inputs are applied. In most cases, it will also be necessary to reset the stages in the same sequence as the flow of logic.

In circuits wherein the gates have a different number of total weights, the designer has a certain freedom to modify individual stages to take advantage of reduced fan-in or fan-out. He can thereby reduce the power dissipated by those stages or permit larger tolerances on the components.

‡ Replaces the *J. J. Tiemann* paper which has been withdrawn.

[1] This method of realization was first offered by *W. H. Kautz* in "The Realization of Symmetric Switching Functions with Linear-Input Logical Elements," IRETEC; September, 1961.

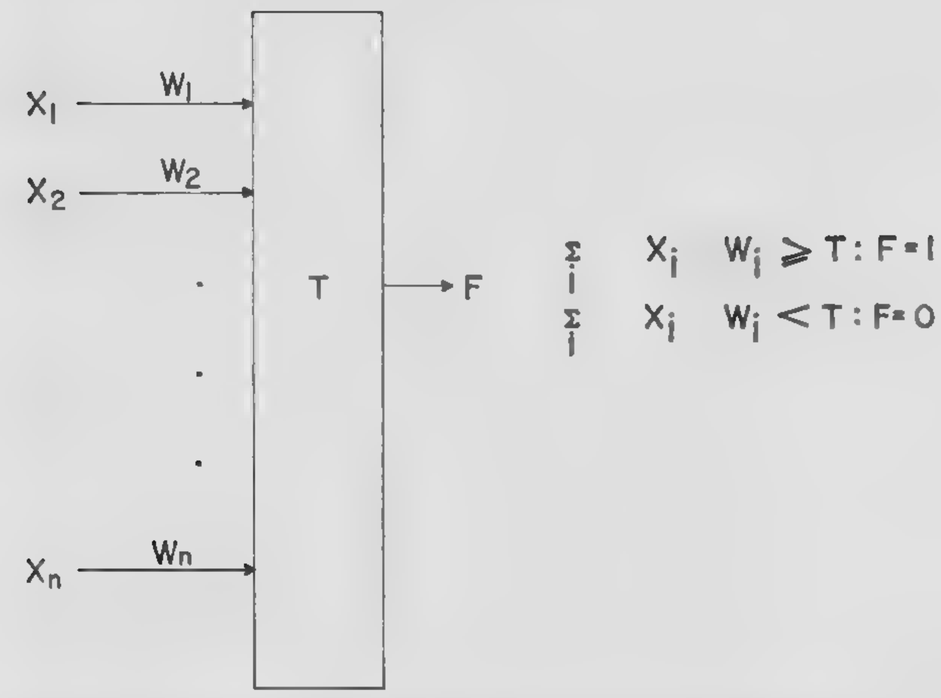


FIGURE 1—Logical operation of the threshold gate.

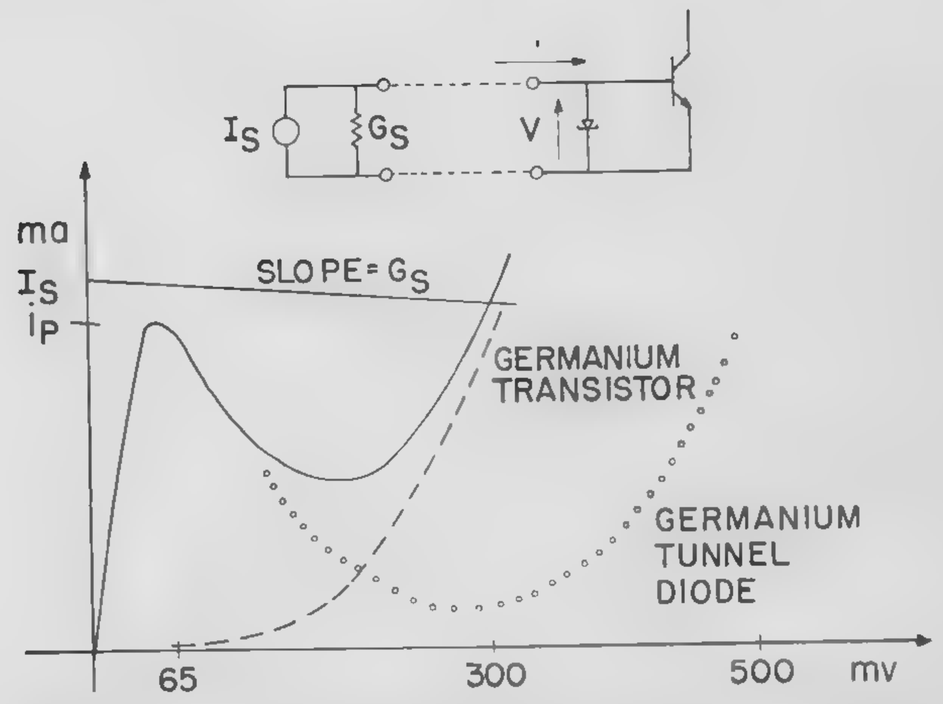


FIGURE 4—Typical input characteristics of tunnel-diode transistor combination. I_s and G_s represent the effective source current and conductance. The solid curve is the combination.

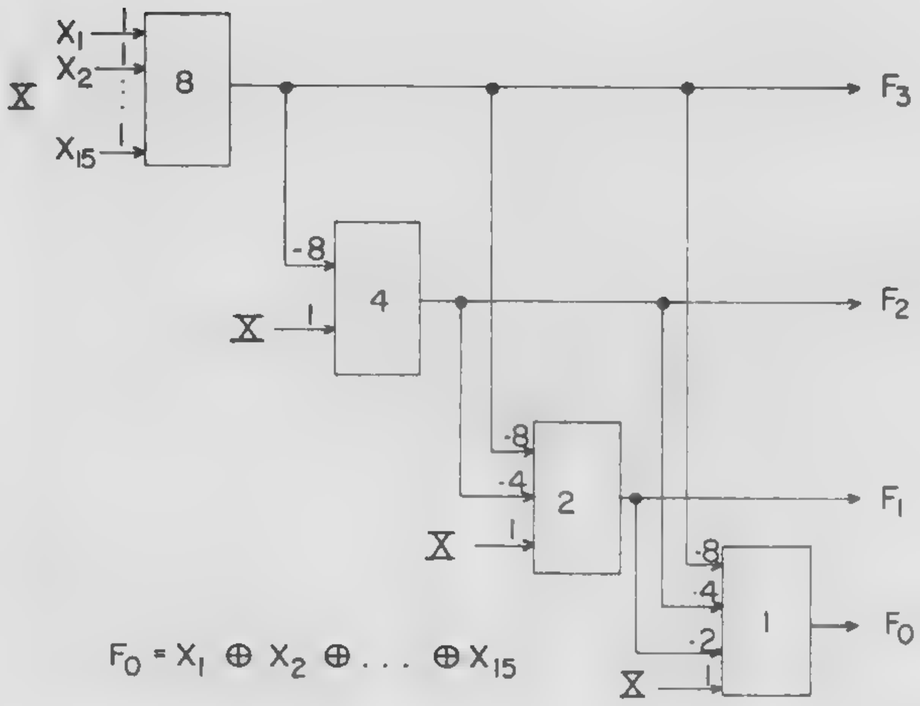


FIGURE 2—Realization of the *15*-variable parity function. If the outputs of all four gates are considered, the circuit is a *unary to binary* converter.

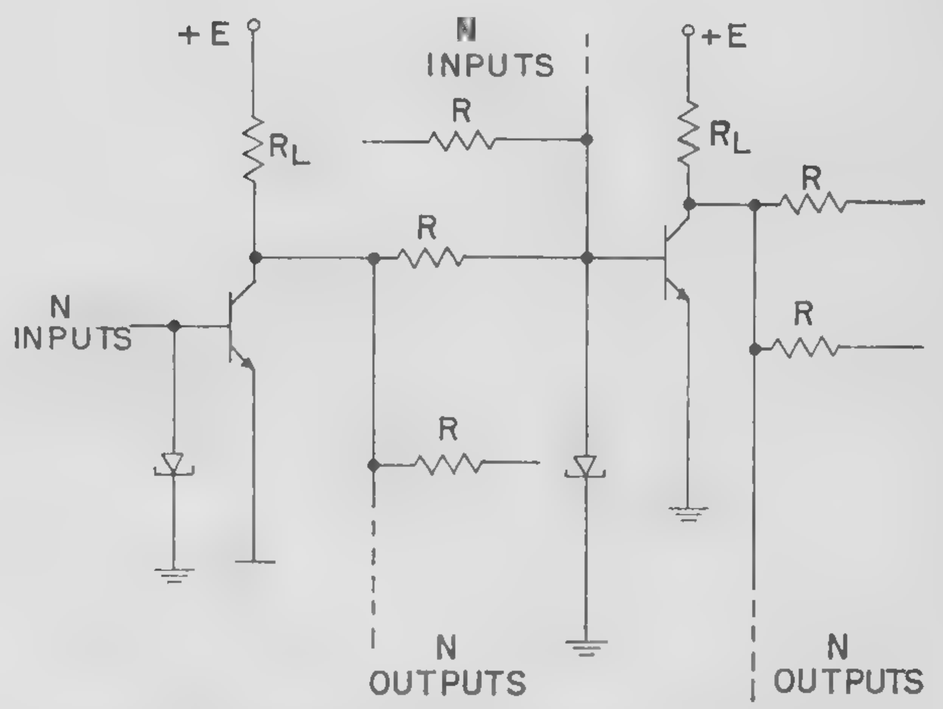


FIGURE 5—Threshold logic gates. Fan-in and fan-out of *50* or more appears to be feasible.

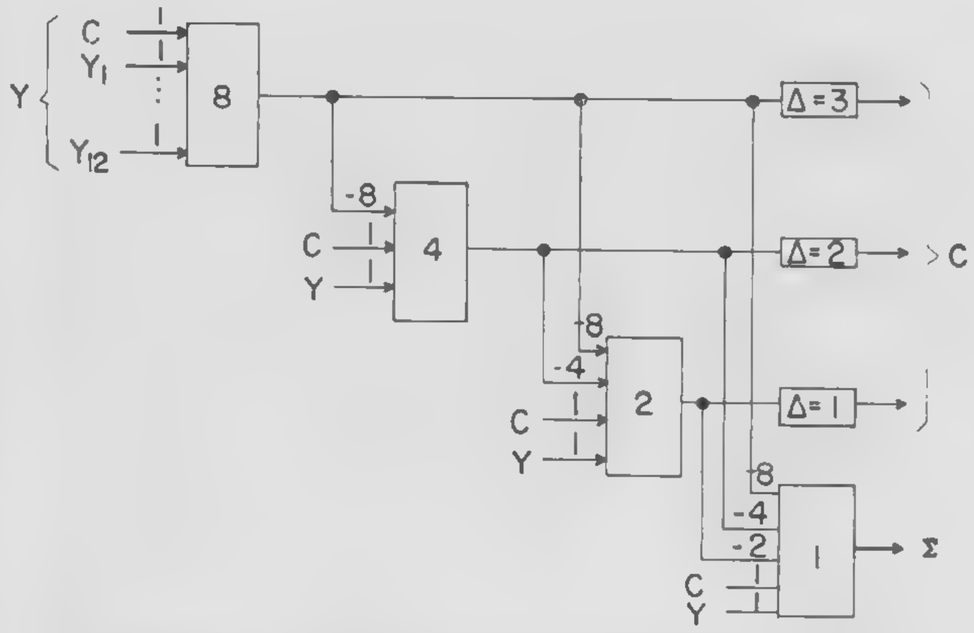


FIGURE 3—Realization of a *12*-input serial added with four threshold gates.

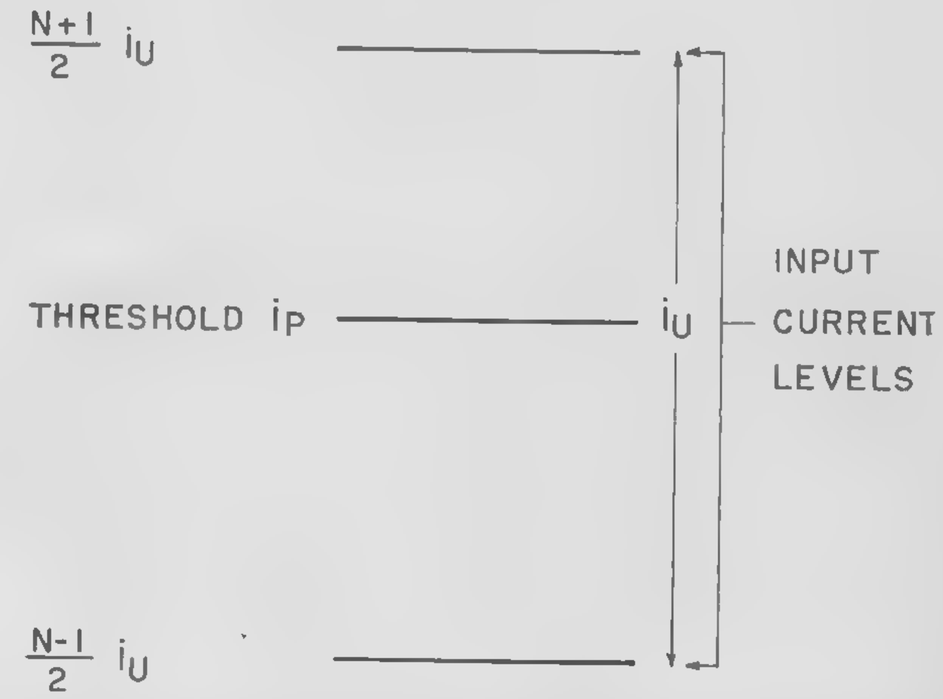


FIGURE 6—Threshold margins of majority gate. The peak current must be between the input levels shown. N is the number of inputs; i_u the unit current.

SESSION VIII: Digital Design Techniques

THPM 8.5: Energy Gain and Directivity Achieved Using Balanced Magnetic Circuits

E. E. Newhall and J. R. Perucca

Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

A MAGNETIC CIRCUIT ORGANIZATION which permits gain and directivity to be obtained easily, without biases, with good margins, and without requiring resistance in the coupling loop, has been established.

Figures 1*a* and *b* show two flux sources. It is clear that whenever the *send* winding is energized, the sources are saturated from right to left. Energization of the *receive* winding sends the flux sources to neutral. Suppose two equal length parallel paths are connected to the flux source of *a* in Figure 1 as shown in *c*. If the *input* and *receive* windings are energized in coincidence, in the senses shown, then the input signal will aid switching in the upper path and inhibit switching in the lower path. At the termination of switching, the outside periphery of the circuit will be perturbed from neutral in a counterclockwise sense. This represents a *1*. Under these circumstances signals in the order of *1-10 ma* turns can act to store information. On the other hand, if the element has information stored in the outside periphery, and the center leg is held neutral, the current in the signal path must build up to a large value, sufficient to switch the outside periphery, if this information is to be destroyed. Also, some reflection shows that whenever the *receive* winding is energized, the output voltage in Figure 1*c* will have the same wave shape as the input voltage, if we neglect resistance losses. Figure 1*d* shows a multiplicity of independent balanced circuits energized from flux sources at the ends. The constriction between balanced circuits prevents interaction.

Balanced circuits may be organized into a three-phase shift register interconnected and driven as shown in Figure 2. Consider phase *2*, for example. Element *1* transmits, and elements *3* and *4* receive. Elements *3* and *4* tip with very little current and once tipped generate a back voltage which keeps the coupling loop current to a minimum. The tipping current which flows can be significantly less than the threshold for switching of the undesired path around the outside periphery of element *2*. Note carefully that for zero tip no coupling loop current flows, and there is no tendency to switch around the outside periphery of element *2*. Since this periphery has a finite threshold, there will be a range of coupling loop currents for which this threshold will not be exceeded. This range of tips is very easy to amplify for this reason.

In Figure 2, it will be observed that elements *1* and *7* are driven from the same clock source and have the same time behavior. A further examination indicates that there are at most six distinct elements, or six distinct time behaviors. We take advantage of this in Figure 3*a* where the first row of elements will be associated with the first bit, and so forth. The interconnections between balanced circuits are the same as in Figure 2. Figure 3*b* shows an input-output curve for one bit. It is clear that the gain is greatest for small signals, as expected.

It should be noted in Figures 2 and 3 that the elements which are receiving should be *enabled* for at least as long as the elements which are transmitting, so that all available signals are absorbed easily by the receiver. This is accomplished easily in Figure 3*a* by using twice as many drive turns on the transmitting structures as the receiving structure.

A *14*-bit shift register has been constructed from the elements shown in Figure 4, wound as shown in Figure 3*a*. This register operates up to *200-kc* bit rates.

A method of internally regenerating flux patterns within ferrite sheets is shown in Figure 5*a*. The reset or *0* pattern is shown in the structure. The first flux pattern below the structure shows how a partially degenerated *1* would appear in memory location No. *1*. The buildup of this degenerate *1* into a full *1* by the action of the four drive phases is shown in the remaining sequence of four flux patterns.

In the top portion of Figure 5*b* is shown a balanced circuit with magnetic inputs at *X* and *X'*. Energization of either *receive* winding causes switching in the balanced circuit. Some reflection shows that this makes it very easy for flux to switch in *X* and out *X'* or vice versa. By contrast, if the *receive* winding is not energized, considerable *mmf* is required to switch flux from *X* to *X'*.

Suppose we substitute a balanced circuit for legs *A*, *B*, *C*, *D*, and the interconnecting legs in Figure 5*a*. The result, and its operating sequence are shown in line diagram form in Figure 5*b*. This is obviously more complicated than Figure 5*a;* however, no biases are required, and, as before, the undesired back path may be ignored for the range of signals to be amplified. Thus, Figure 5*b* represents a potential method of transmitting and regenerating flux patterns in sheets, with good margins, without biases.

Acknowledgment

The authors are indebted to many members of the Communications Systems Research Department of Bell Telephone Laboratories for encouragement and assistance. They are also indebted to the Metallurgical Research Department for their close cooperation and to *J. H. Brown* and *J. C. Stuart* for their enthusiastic development of the series-connected array shown in Figure 4.

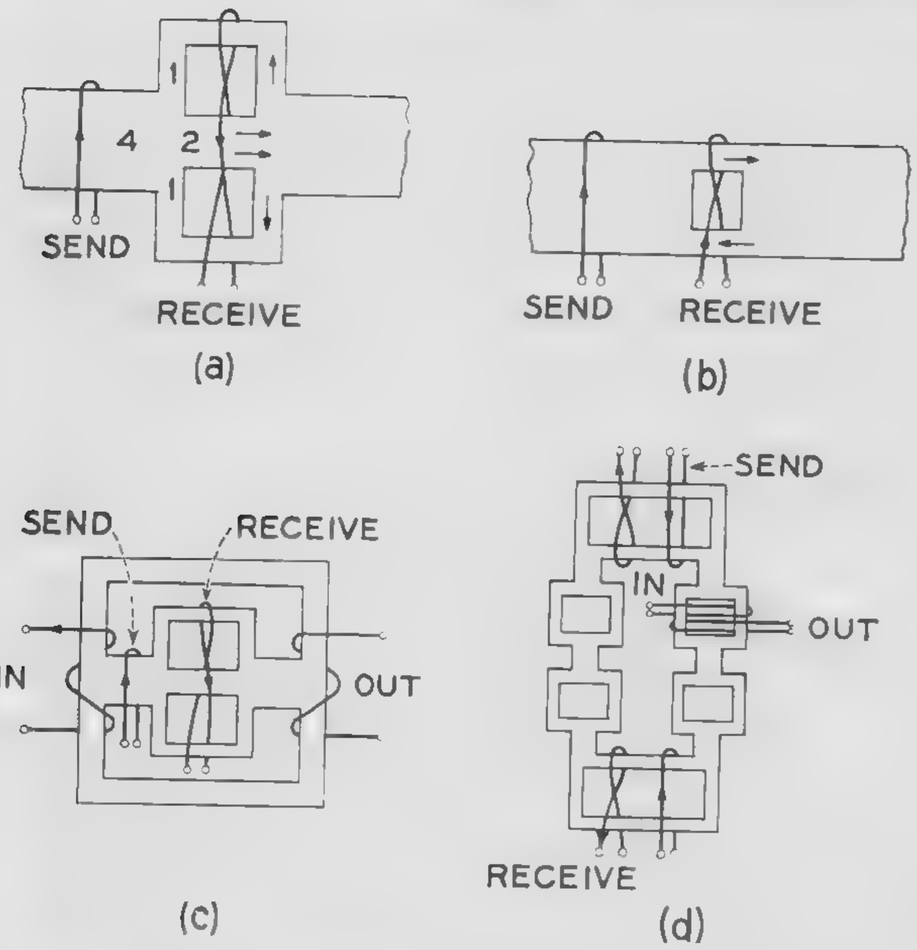
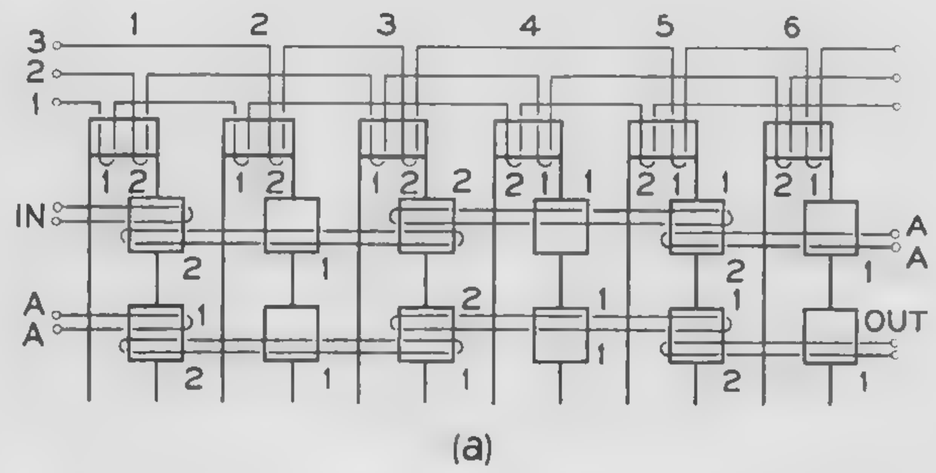


FIGURE 1—**Two different flux sources are shown in *(a)* and *(b)*. A simple balanced circuit is illustrated in *(c)*, and in *(d)* is a series-connected array of simple balanced circuits.**



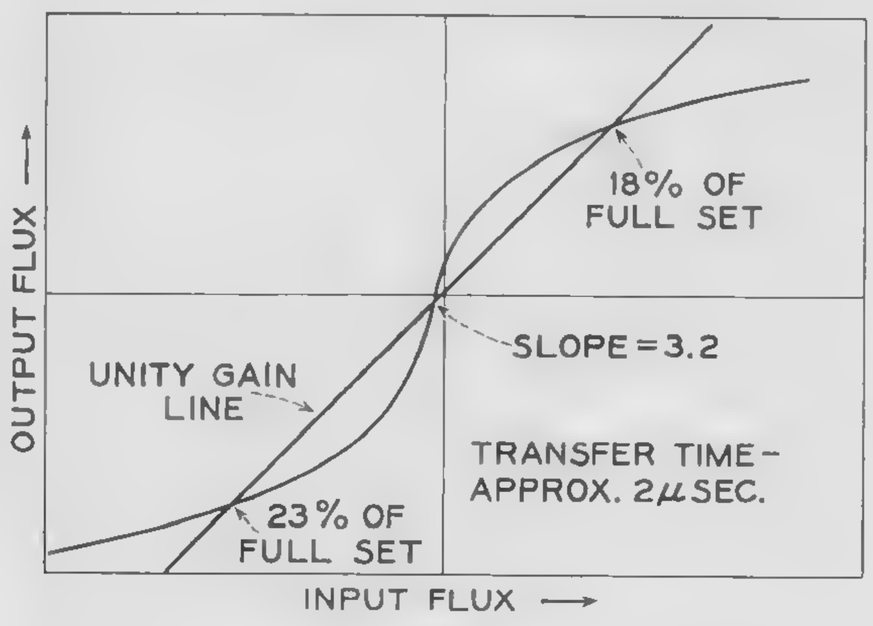
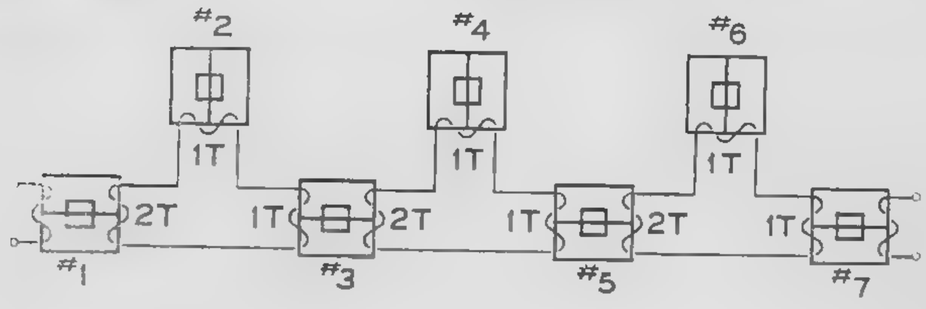


FIGURE 3—**A three-phase shift register, constructed from series-connected simple balanced circuits is shown in *(a)*. An input-output measurement on one bit of an operating register appears in *(b)*.**



PHASE 1 – #3 ISOLATES. #1, #2, #7 RECEIVE. #5 TRANSMITS. #4 TRANSMITS CANCELLING #5 IN COMMON LOOP. #6 HELD.

PHASE 2 – #5 ISOLATES. #3, 4, RECEIVE. #1, #7 TRANSMIT. #6 TRANSMITS CANCELLING #7 IN COMMON LOOP. #2 HELD.

PHASE 3 – #1,7 ISOLATE. #5, #6 RECEIVE. #3 TRANSMITS. #2 TRANSMITS CANCELLING #3 IN COMMON LOOP. #4 HELD.

FIGURE 2—**Three-phase shift register constructed from simple balanced circuits.**

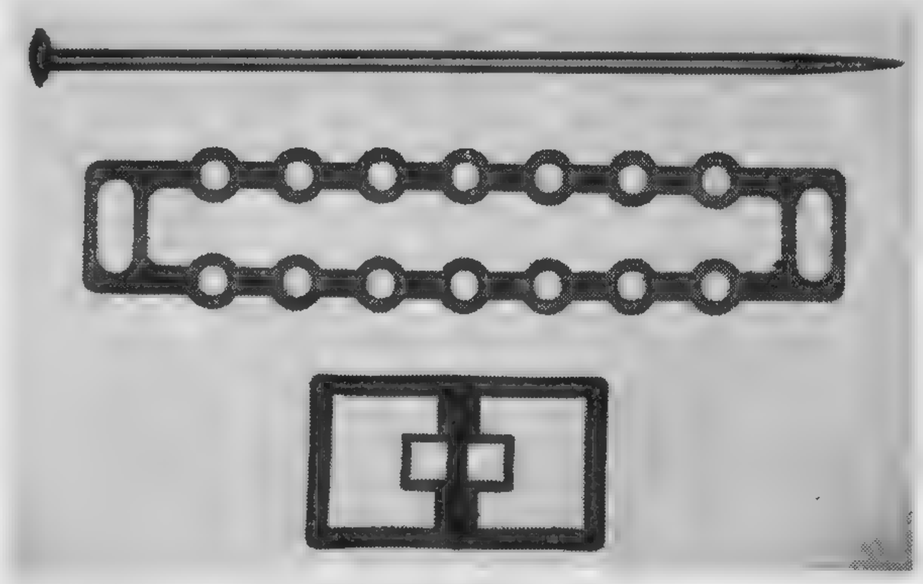


FIGURE 4—**Simple-balanced circuit and series-connected balanced circuits. Holes are *0.040" i.d.* and *0.080" o.d.***

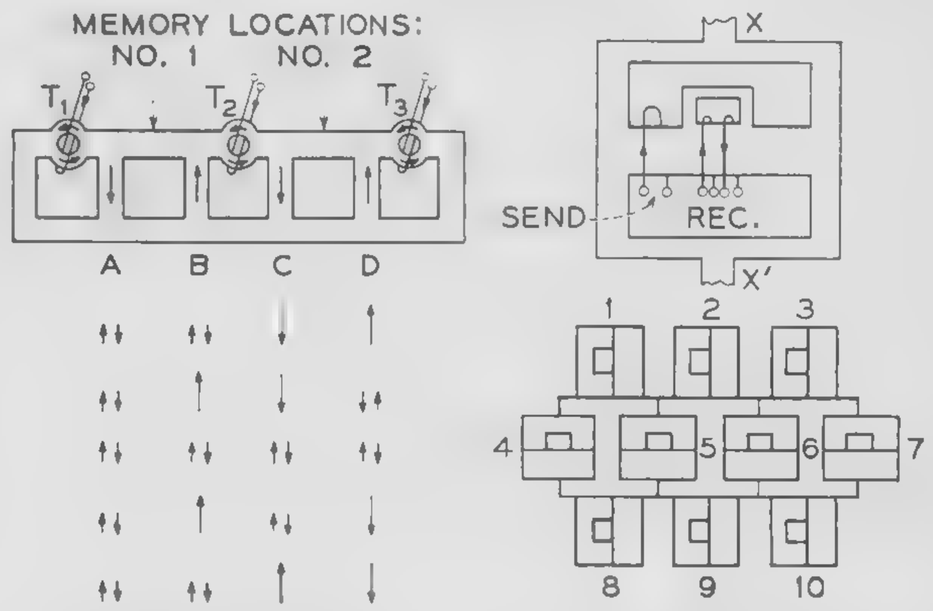


FIGURE 5—**Single and double-rail elements supposedly capable of internal flux pattern regeneration by pumping.**

Informal Discussion Sessions

THE 7: Coherent Optical Techniques and Applications

[West Ballroom]

Moderator: G. Wade, Raytheon Company, Burlington, Mass.

Panel Members: W. W. Rigrod, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
J. A. Armstrong, Harvard University, Cambridge, Mass.
R. H. Rediker, MIT Lincoln Laboratory, Lexington, Mass.
E. I. Gordon, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
C. J. Peters, Sylvania Electric Products Inc., Waltham, Mass.

THE 8: Integrated Digital Logic

[East Ballroom and Assembly]

Moderator: D. Farina, Fairchild Semiconductor, Div. Fairchild Camera-Instrument Corp., Palo Alto, Calif.

Panel Members: C. Cook, Jr., Texas Instruments, Inc., Dallas, Tex.
E. Hall, MIT Instrumentation Laboratory, Bedford, Mass.
U. S. Davidsohn, General Electric Co., Syracuse, N. Y.
I. Weiman, Electro-Optical Systems, Inc., Pasadena, Calif.
R. Kudlich, AC Spark Plug Div. General Motors Corp., El Segundo, Calfi.
R. Platzek, Autonetics Div. No. American Aviation, Inc., Downey, Calif.

THE 9: Broadband Amplifiers

[Pennsylvania West]

Moderator: D. O. Pederson, University of California, Berkeley, Calif.

Panel Members: L. Roeshot, HRB-Singer, Inc., State College, Pa.
R. Burgess, MIT Lincoln Laboratory, Lexington, Mass.
V. R. Saari, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
E. G. Nielson, Electronics Lab., General Electric Co., Syracuse, N. Y.
N. Winningstad, Tektronix, Inc., Beaverton, Ore.
S. Schwartz, Fairchild Semiconductor Div., Fairchild Camera-Instrument Corp., Palo Alto, Calif.

Informal Discussion Sessions

THE 10: Combined Analog-Digital Circuit Techniques

[Pennsylvania East]

Moderator: E. P. Stabler, Electronics Laboratory, General Electric Co., Syracuse, N. Y.

Panel Members: G. A. Korn, University of Arizona, Tucson, Ariz.
R. H. Baker, MIT Lincoln Laboratory, Lexington, Mass.
M. McWhorter, Stanford University, Palo Alto, Calif.
F. J. Witt, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
H. W. Abbott, General Electric Co., Syracuse, N. Y.
F. D. Waldhauer, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

THE 11: Partial Switching of Ferrites

[Independence-Constitution]

Moderator: R. E. McMahon, MIT Lincoln Laboratory, Lexington, Mass.

Panel Members: W. Overn, Remington Rand Univac, St. Paul, Minn.
H. P. Lemaire, RCA, Needham, Mass.
V. J. Sferrino, MIT Lincoln Laboratory, Lexington, Mass.
R. Shahbender, RCA Laboratories, Princeton, N. J.
I. Italia, ITT Federal Laboratories, Nutley, N. J.
O. Gutwin, IBM Corp., Yorktown Heights, N. Y.
A. Elovic, Electronic Div. Indiana General Co., Keasbey, N. J.

SESSION IX: Logic II

Chairman: J. S. Mayo

Bell Telephone Laboratories, Inc., Murray Hill, N. J.

FAM 9.1: Switches With Complementary Transistors

A. E. Bachmann

P.T.T. Research Laboratory

Berne, Switzerland

If one of the two complementary transistors in the circuit of Figure 1 starts drawing current, a regenerative feedback action takes place because the collector of each transistor is directly connected to the base of the other one. With the aid of a reference source, one of the transistors can be held to cutoff so that no regenerative action takes place until this blocking source is overcome. Depending upon which two of the three leads are under consideration, this circuit develops either an open- or a short-circuit stable characteristic and therefore is similar to a four-layer element or a tunnel diode, respectively[1].

As long as the voltage V at the emitter input of transistor T_1 (Figure 1) is less than the battery voltage E_1 this transistor is cut off. On the other hand, transistor T_2 is fed with the collector cutoff current I_{CBOp} of transistor T_1. This first leakage current, together with the collector cutoff current I_{CBOn} of transistor T_2, causes a small current I_{10} to flow out of battery E_1. Its magnitude appears in equation *(2)*, when the operating point reaches the switching point V_S of the characteristic. The value of the switching voltage V_S is given in equation *(1)*. Most of the variation V_S with temperature comes from the last term; i.e., from the current drain I_{10} out of battery E_1. Notice that I_{CBOp} and V_{Cp} have a negative sign, whereas I_{CBOn} and V_{CEn} are positive in this notation. This last term can be made small by choosing transistors with small cutoff currents and large collector resistances and making the source resistance R_1 small. If E_1 is made large enough, the last three terms in equation *(1)* have little influence.

Once transistor T_1 starts conducting, it rapidly brings T_2 into conduction and vice versa. The current I_1 increases, which causes V to drop. The switch now operates its negative resistance region; points S to W. The slope is given by equation *(3)* and therefore can be adjusted with the aid of R_1. When the temperature is changed, the magnitude of the negative resistance changes in direct proportion to that of the common emitter current amplification factor α_{En} of transistor T_2. A typical set of measured curves is shown in Figure 3. If the temperature increases from $0°C$ to $+41°C$ the switching voltage V_S drops approximately 0.5 v. Equations *(1)* and *(2)* yield a drop of 0.48 v. This change is rather large because of the type of transistors used, having collector cutoff currents I_{CBOp} of up to $10\mu a$. The magnitude of the negative resistance shows a slight increase caused by the increase of α_{En} with temperature. Both the *off*- and the *on*-resistance change only slightly. Their magnitudes are the order of several megohms and *10-ohms*, respectively.

The shape of the characteristic of this first switch is mainly determined by R_1 and the current amplification factor α_{En} of the *npn*-transistor T_2.

If this transistor T_2 is also back-biased with the aid of an additional source E_2 (Figure 4), the leakage current I_{10} can be reduced and the stability of the switching voltage, with respect to the temperature changes, can be improved appreciably. Equation *(5)* shows that the magnitude of I'_{10} is smaller by a factor $(\alpha_{En} + 1)$ than that of I_{10} in the non-back-biased version.

Once the potential at the emitter of T_1 has reached the level of E_1 (equation *(4)* for point G of characteristic) T_1 starts to conduct. Its collector current flows almost entirely into R_2. This continues, and the voltage V stays practically constant until the voltage drop across R_2 gets larger than the blocking source E_2. Now transistor T_2 also opens, and the regenerative action can take place. The switching current I_S (equation *(6)*) is mainly determined by R_2 and E_2, which vary little with temperature. The magnitude of the negative resistance is smaller than in the previous case, especially when R_2 is small; equation *(7)*. The main difference between the two characteristics, as plotted in Figures 1 and 4, lies in the flat portion G to S of the latter and in the improvement of the stability of V_G over that of V_S with changing temperature. The switching current I_S (Figure 5) shows a small decrease in magnitude of approximately 35 μa; whereas the rest of the switching characteristic stays remarkably constant over a temperature range of from $0°C$ to $+40°C$ for regular germanium alloy-type transistors.

For practical applications the back-biasing voltage E_2 can be obtained from E_1 with a voltage divider or reference diode.

With this second circuit, switching characteristics of almost any shape can be designed as long as the limiting values of the transistors are observed.

The application of these switches in timers, counters, clock pulse and sawtooth generators is straightforward. But in the logic part of telephone-switching networks one often needs circuits where n paths lie in *parallel lock-out*. As soon as one, and only one, of these n paths is established, the rest of them must be blocked; Figure 6*a*. If none of the n switches is in the *on* state, all of them have a characteristic of type B shown in Figure 6*b* when looking into the emitter of each of the *pnp* transistors. A positive pulse at terminal E_0 turns one of the switches on. As soon as this switch draws current, the characteristic of the others changes into Type C; Figure 6*c*. This is so because the current flowing through the common resistor R_s builds up the back-biasing voltage E_2, which together with R_2 is responsible for the flat portion G to S of the second characteristic. If now another trigger pulse appears at terminal E_0 it cannot turn on any one of the switches.

Both of these switches, but especially the back-biased one, are useful if an open-circuit stable switching characteristic of a definite shape is needed, or if it is necessary that this shape be altered by applying or changing an external voltage or resistor.

[1] Karp, M. A., "A Transistor DC Negative Immittance Converter," *Proc. Natl. Electronics Conf.*, vol. 12; 1956.

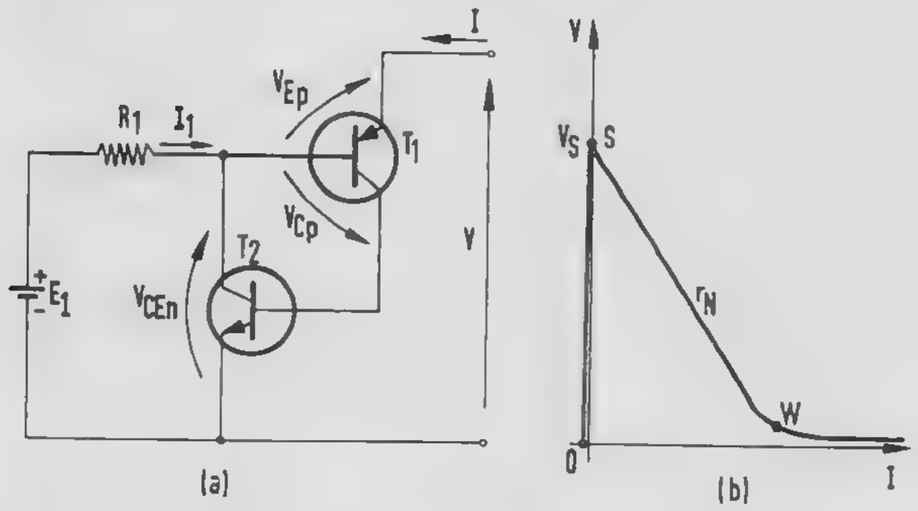


FIGURE 1—**Complementary switch circuit and its *V-I* characteristic.**

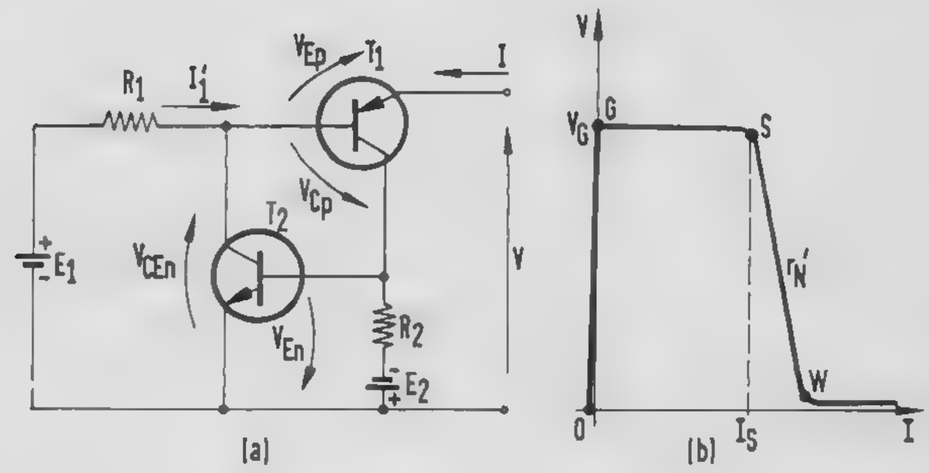


FIGURE 4—**Circuit *(a)* and *V-I* characteristic *(b)* of back-biased complementary switch.**

(a) COMPLEMENTARY SWITCH OF FIG. 1:

$$V_S = E_1 + V_{EpS} - kT/e - R_1 I_{10} \quad (1)$$

$$I_{10} = (\alpha_{En}+1)\left[I_{CBOn} - I_{CBOp} + (V_{CEn}/r_{Cn}) - (V_{Cp}/r_{Cp})\right] \quad (2)$$

$$r_N = -\alpha_{En} R_1 \quad (3)$$

(b) BACKBIASED COMPLEMENTARY SWITCH OF FIG. 4:

$$V_G = E_1 + V_{EpG} - R_1 I'_{10} \quad (4)$$

$$I'_{10} = I_{10} / (\alpha_{En} + 1) \quad (5)$$

$$I_S = (E_2 - V_{EnS}) / R_2 \quad (6)$$

$$r_{N'} = -\alpha_{En} R_1 \left[1 + (1/R_2)(\partial V_{En}/\partial I)\right] \quad (7)$$

FIGURE 2—**Principal equations: α = common emitter, short-circuit current-amplification factor of transistor T_2 (often denoted as h_{ie} or β).**

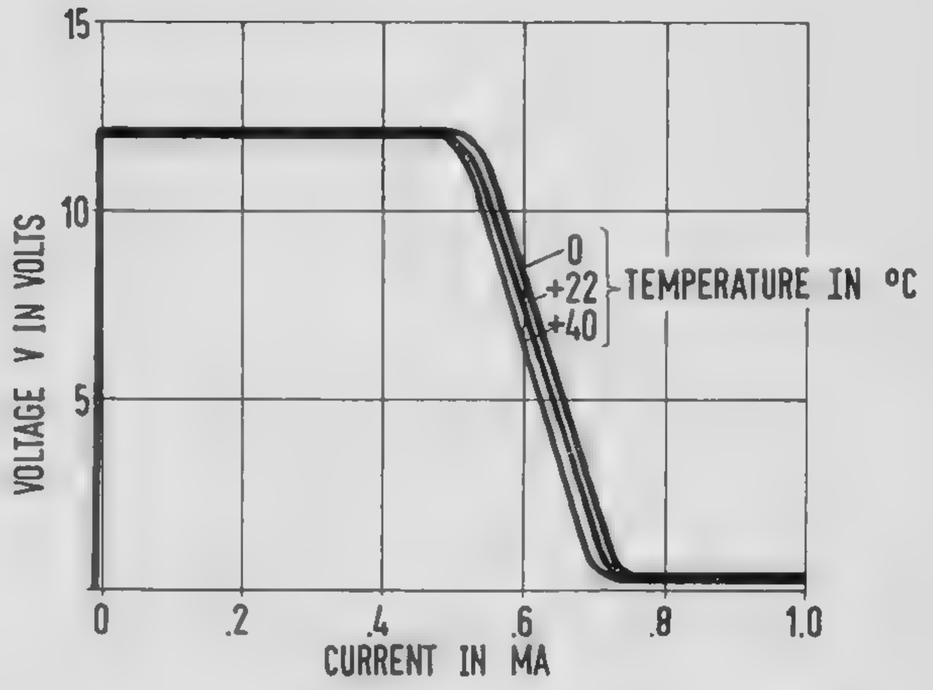


FIGURE 5—**Temperature measurements on Figure 4 circuit: $E_1 = 12$ v; $R_1 = 1$ kilohm; $E_2 = 1.55$ v; $R_2 = 3.2$ kilohm; T_1: OC 77; T_2: OC 140, with $\alpha_{En} = 69$.**

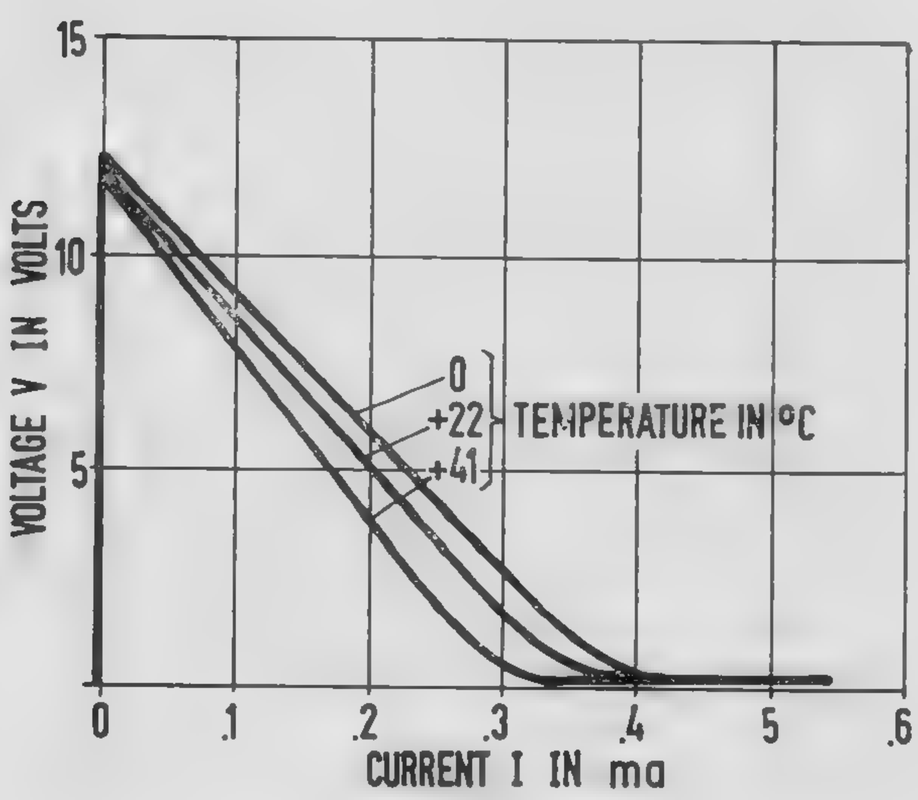


FIGURE 3—**Temperature measurements on Figure 1 circuit: $E_1 = 12$ v; $R_1 = 390$ ohms; T_1: OC 71; T_2: OC 140, with $\alpha_{En} = 86$.**

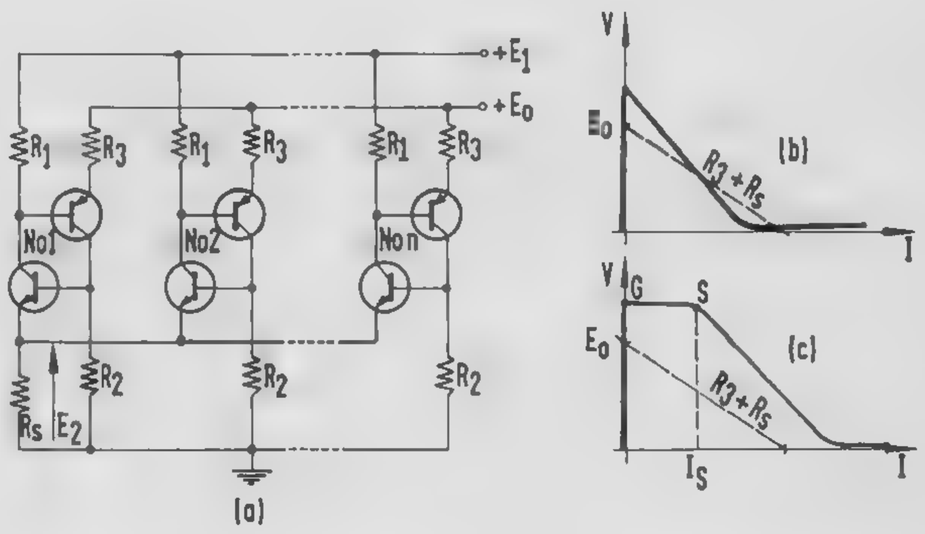


FIGURE 6—**A possible application of the general lock-out circuit using complementary switches is illustrated in *(a)*. The *OFF* characteristic *B* plot is in *(b)*; *ON* characteristic *C* in *(c)*.**

SESSION IX: Logic II

FAM 9.2: The Diamond Cricuit

R. H. Baker

MIT Lincoln Laboratory*

Lexington, Mass.

ANALOG COMPUTING is generally considered to be the antithesis of digital computing, and vice versa. Either method is capable of performing virtually all essential computing operations, but certain operations can be performed far more effectively by analog methods and others by digital methods. In real-time signal processing, the signals to be processed are usually analog in character. They vary continuously with time and can be fed directly into analog systems simply and economically, without introducing artificial coding (sampling) processes. Digital processing, on the other hand, has advantages of greater stability and accuracy. Many computing and telemetry systems are, therefore made up of a combination of digital and analog circuits, with provisions for analog-digital conversion at interfaces.

A new circuit currently under investigation offers unusual promise of bridging the gap between digital and analog methods and circuitry. Known as the *diamond circuit*, it is essentially a bridge modulator in which two-terminal elements (diodes) have been replaced by three-terminal elements (transistors) with power gain.

The basic configuration of the circuit and its relation to a simple diode bridge is shown in Figures 1 and 2. The remaining illustrations show how the same basic circuit, with minor variations, can be used as a building block to perform a wide variety of computing and signal processing operations.

In operation, the diamond circuit is a digital-analog hybrid, with some characteristics of each of these other species and some that are peculiar to itself. These characteristics can best be described in reference to certain fundamentals of digital and analog computing circuits.

In any signal-processing system, it is desirable to direct or route the data signal in a continuous fashion without unintentional distortion during detection or during processing. In practice, a system has losses, and the detection process lowers the signal energy (introduces errors). Signal energy lost during detection must be restored by regeneration (the error removed), before further routing, information processing, or computation can proceed.

In a digital system, signal regeneration is effected by using the data signal to switch an associated voltage supply to ground through a controlled resistance (or to not-switch the supply to ground, depending on whether the input signal is greater or less than a fixed digital threshold). Signal standardization is also accomplished by this supply-switching technique. Considerable power is used by this form of signal standardization, but the effects of device parameter drifts are minimized. The power required is directly related to speed and stability. Effective signal standardization and sharp controllable threshold are important advantages of digital design, but the power requirement can be disadvantageous.

Analog systems, on the other hand, generally employ signal detection independent of threshold. Losses (error) in primary signal are continuous. Hence regeneration or amplification must be continuous and must be very accurately controlled to insure stability and accuracy.

The basic operation performed by the diamond circuit may be described as signal change by offset control. This feature, plus the large power gain of the circuit, can be used to perform most of the functions usually required of a digital system, but with the circuit economy and mutiple reference inherent in an analog system. Specifically, the diamond circuit samples the data signal with very low losses and transfers this signal to the output at a high power level, with a readily adjustable threshold and/or offset. Continuity is not lost, as it is in the digital signal-detection process, and power required at transfer is very small.

The threshold feature is a basic property of digital systems, but the diamond circuit threshold follows the variations in the data signal: this is a property of an analog system. The diamond circuit is unique, however, in that it avoids signal losses by referencing automatically to the input signal. This is accomplished by floating the circuit. The data signal is used as the threshold control, and thus the threshold is continuously variable as the data signal changes; this provides a degree of flexibility not possible in ordinary digital systems. In principle, signal standardization is perfect, since the data signal may in theory be transferred to the output without distortion. The diamond circuit differs from conventional analog circuits in the sense that its gain need not be continuously controlled.

Gated sampling is a second important property of the diamond circuit. It provides positive control of signal routing, formerly characteristic only of digital equipment, without requiring the use of a fixed threshold. The variable threshold of the diamond circuit allows the use of processing and signal-detection techniques characteristic of analog equipment, without requiring continuous regeneration and *single-thread* processing. In addition, since gated sampling detection is possible, the effects of drift in device parameters are minimized.

Summarizing, the circuit offers:

(1)—A hybrid approach—
- (a)—Clocked, referenced discrete levels
- *(b)*—Single-thread multileveled

(2)—Defined accuracy
(3)—Floating system
(4)—Economy
(5)—Building block approach.

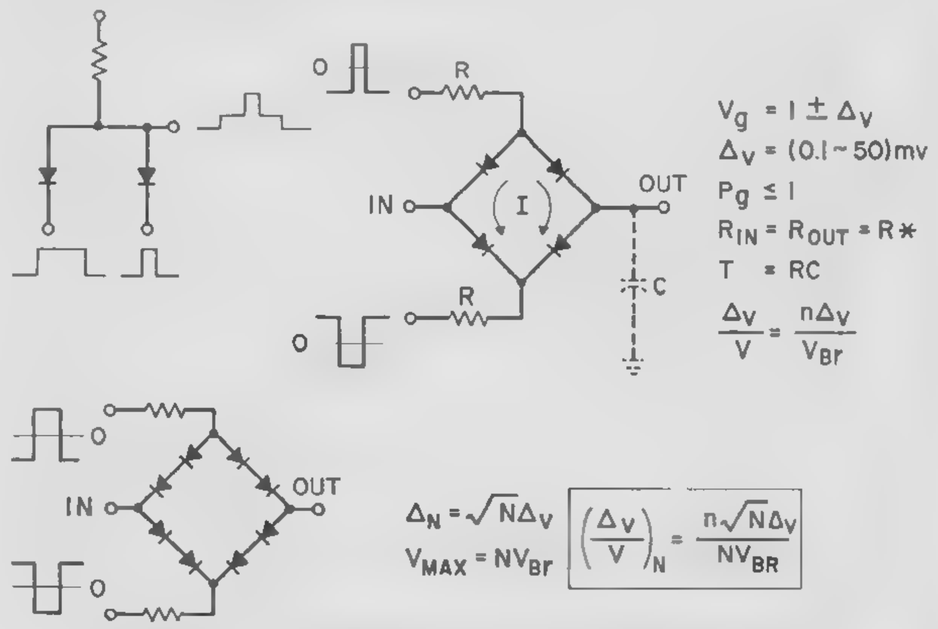


FIGURE 1—**Signal-to-noise considerations.**

* Operated with support from the U. S. Army, Navy and Air Force.

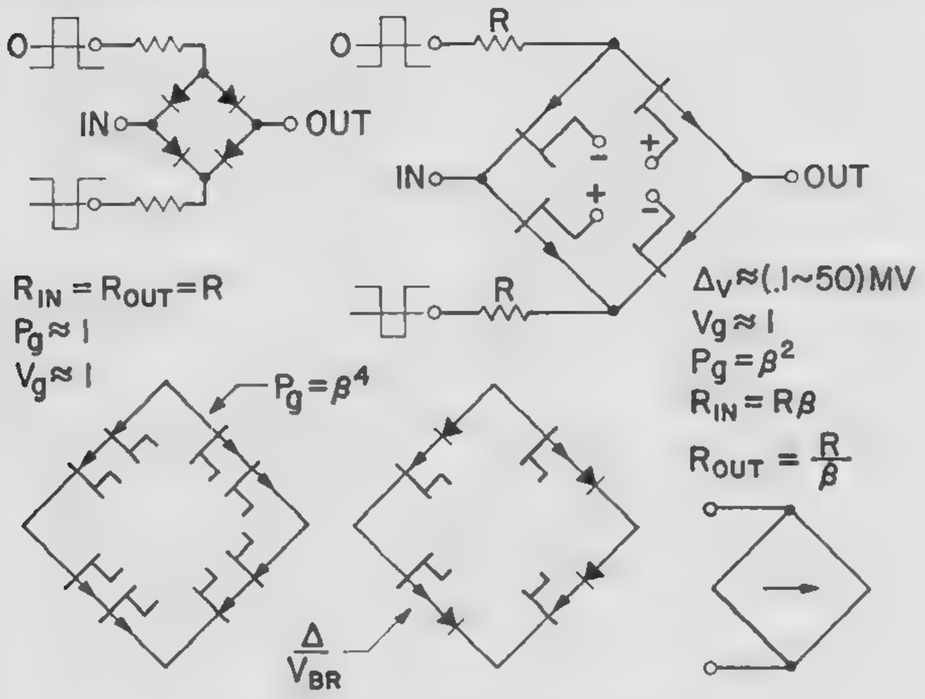


FIGURE 2—Basic diamond circuit.

FIGURE 3—Offset and threshold.

FIGURE 4—Analog add and subtract.

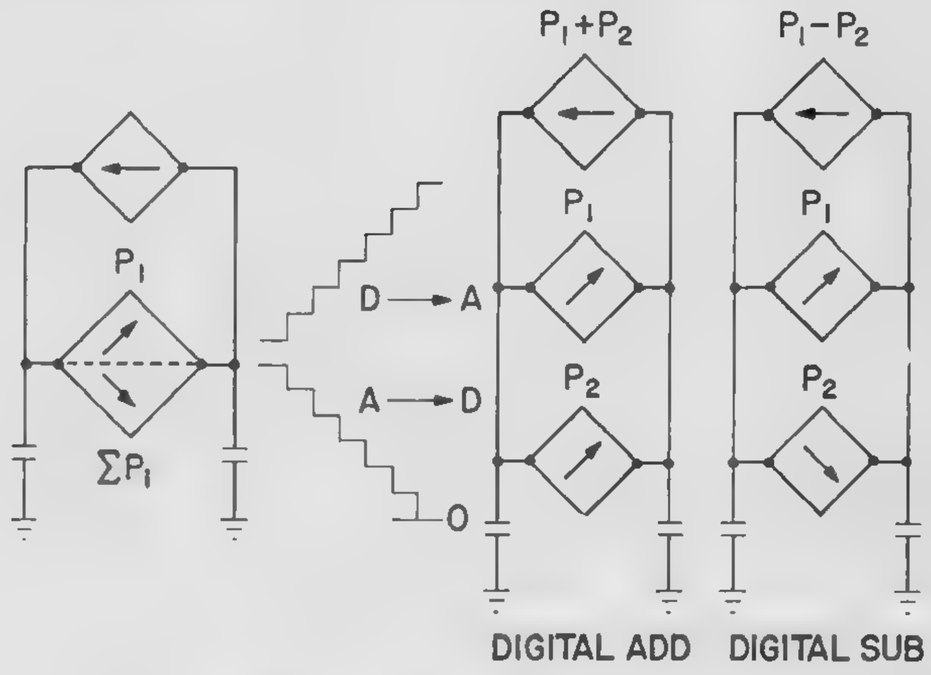


FIGURE 5—Digital add and subtract.

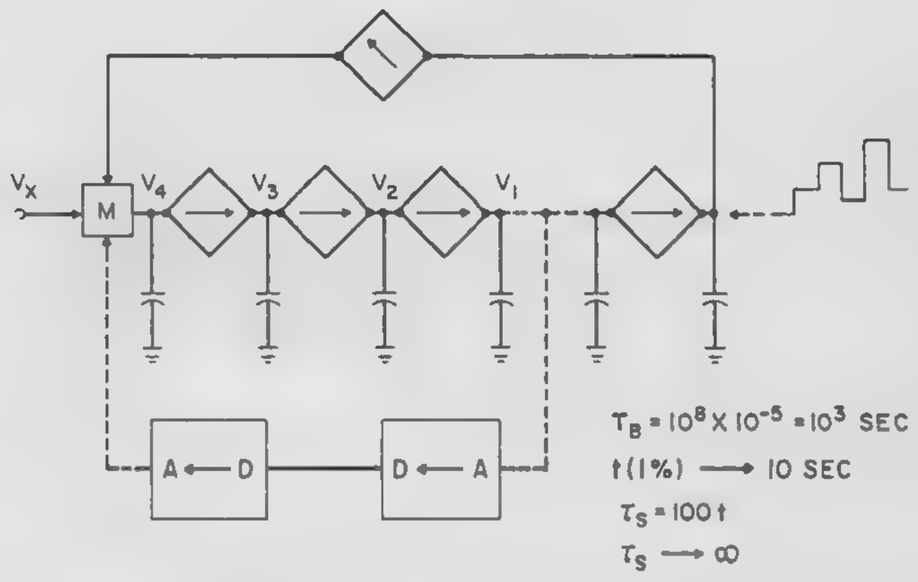


FIGURE 6—Digit *A* to *D* and *D* to *A* conversion.

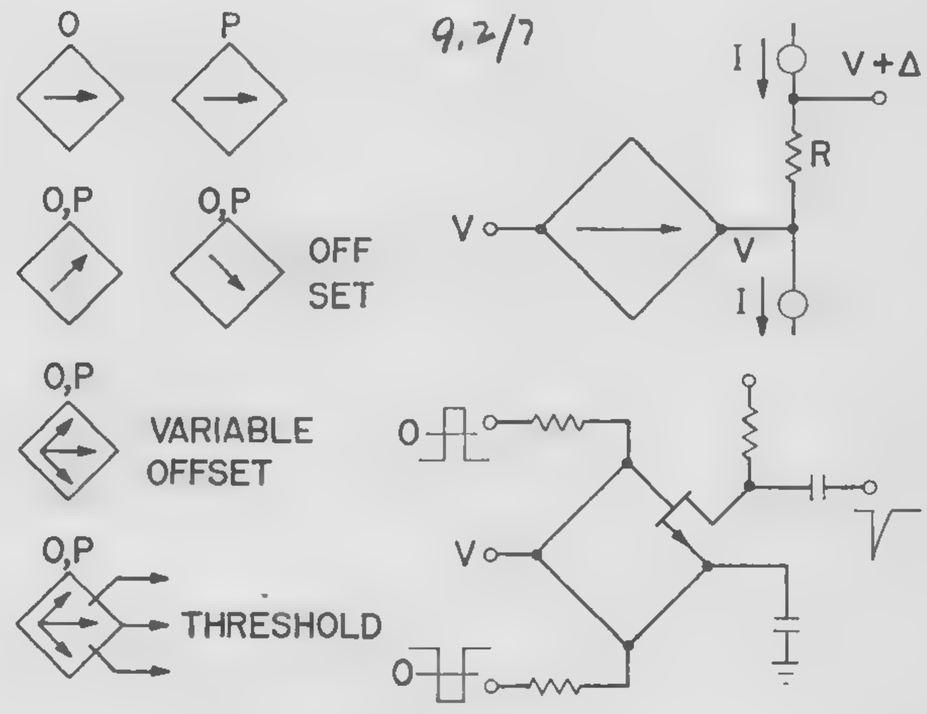


FIGURE 7—Analog storage.

SESSION IX: Logic II

FAM 9.3: UHF Analog-Digital Converter

H. R. Schindler

Electronics Laboratory, General Electric Company

Syracuse, N. Y.

Conversion of wide-band analog signals into digital form with small quantization error becomes possible by using new high-speed semiconductor devices such as tunnel diodes, charge-storage diodes[1], computer diodes and *uhf* transistors. Specifically, a converter having a sampling rate of *50 Mc* and a bit rate of *300 Mc* will be described. Such a converter samples the analog signal at intervals of *20 nsec* and generates, according to the signal level, a series of six bits within this time.

Hybrid Parallel-Series Solution

The block diagram of the system is shown in Figure 1. A hybrid parallel-series solution has been chosen, as it offers the highest circuit simplicity. Basically, the signal is split into three main channels, each of them being split again into three sub-channels. In the first three sub-channels, three level decisions are made simultaneously to determine if the signal level lies in the first, second, third or fourth quarter of the maximum signal range. As a result of these decisions a weighted current is introduced into the second and third main channels. A few nanoseconds later three level decisions are made in the second main channel. The outcome of the second series of three decisions introduces a weighted current into main channel three; point *Q*. Finally, the last three level decisions are made.

Care has been taken to terminate all transmission lines properly to avoid reflections in the system. Also, the problem of isolation has been treated carefully, such that only a tolerably small portion of the sampling signal can flow back to the signal source.

Basic Sampling—Threshold Circuit

Figure 2 shows the basic sampling and threshold circuit which consists of a transistor and two tunnel diodes. The transistor acts as an isolator and transmission line termination. The first tunnel diode (threshold *TD*), is fed by both the signal current and one-nanosecond wide current pulses repeating at *50 Mc*. These pulses are generated in a circuit using charge-storage diodes. The relative current levels are shown in Figure 3. In the absence of the current pulse, the tunnel diode can never switch into the high voltage state. At the instant of the current pulse, the diode fires if the signal current is below the threshold level. The second tunnel diode (memory *TD*) is biased slightly below the peak current, such that it switches into the high voltage state if the first diode fires. It remains in this state until it gets reset. The voltage waveforms across the two diodes are shown in Figure 4.

Current Level Differences Minimized

The threshold tunnel diodes are able to resolve current-level differences of less than *50 μa* within *.3 nsec*. This corresponds to a charge of less than *.015 picocoulomb* or *100,000* electrons. The theoretical limit determined by the tunnel diode shot noise was calculated to be in the order of *.004 picocoulomb*. Thus, for a signal with *25-Mc* bandwidth and maximum amplitude of *10 ma* this resolution is more than sufficient for conversion into six bits; 64 levels.

Figure 5 shows the basic layout of the weighting circuit, which, according to the decision of the threshold tunnel diode introduces within a few nanoseconds, a precise amount of current into the points *P* or *Q* of the block diagram.

Transmission Line Transformer In Circuit

The circuit uses a transmission line transformer, consisting of a twisted pair of wires, for phase inversion. The lower cutoff frequency of the transformer has been chosen such that the signal gets differentiated. In this manner problems concerning *dc* restoration can be avoided. The delay in the transformer is about *.3 nsec* and the signal risetime at its output is less than *.2 nsec*. The transformer is connected to a third tunnel diode for current amplification. Its output feeds a common-base transistor stage which drives the switching network consisting of ultra-fast computer diodes and another common-base stage. The precision of the current is achieved by choosing a high value for the emitter resistor of the second transistor.

The blocks which perform the logic and parallel-series conversion are based on the technique used in a pumped tunnel-diode transistor logic system operating at *500-Mc* clock rate[2].

---

[1] Moll, J. L., Krakauer, S., Shen, R., "P-N Junction Charge-Storage Diodes," *Proc. IRE*, p. 43-53; January, 1962.

[2] Peil, W., and Marlof, R., "Computer Circuitry for 500 Mc," *1962 Intl. Solid States Circuits Conference* Digest of Technical Papers, p. 52-53; Feb., 1962.

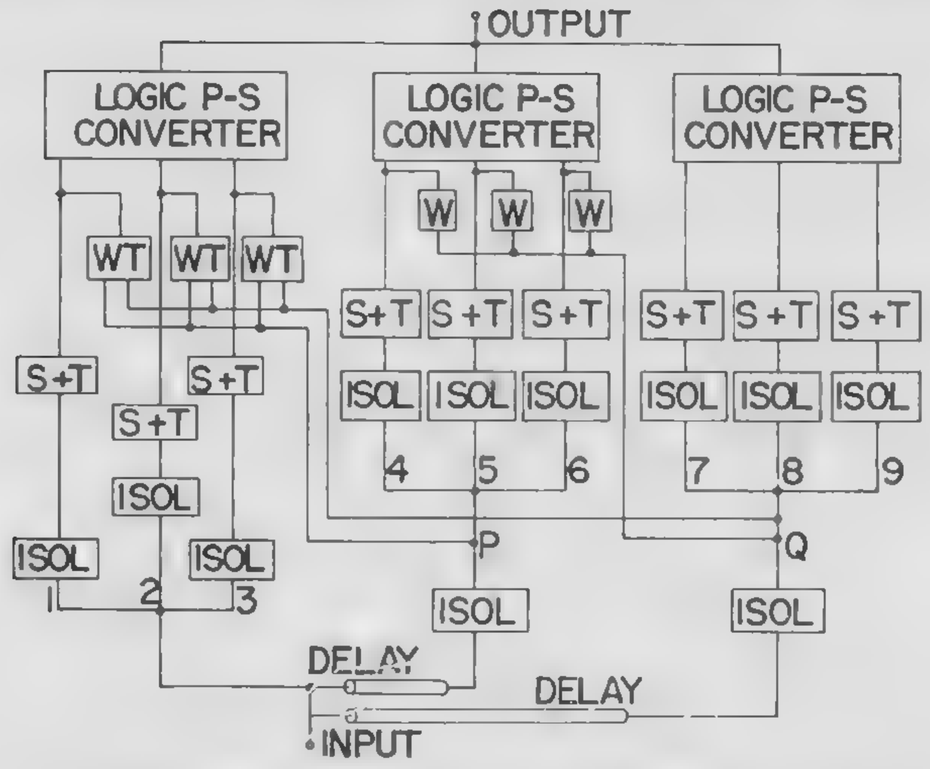


FIGURE 1—Block diagram of analog-digital converter. *Isol.* . . . isolation stage; *S & T* . . . sampling and threshold circuit; *W* . . . weighting circuit.

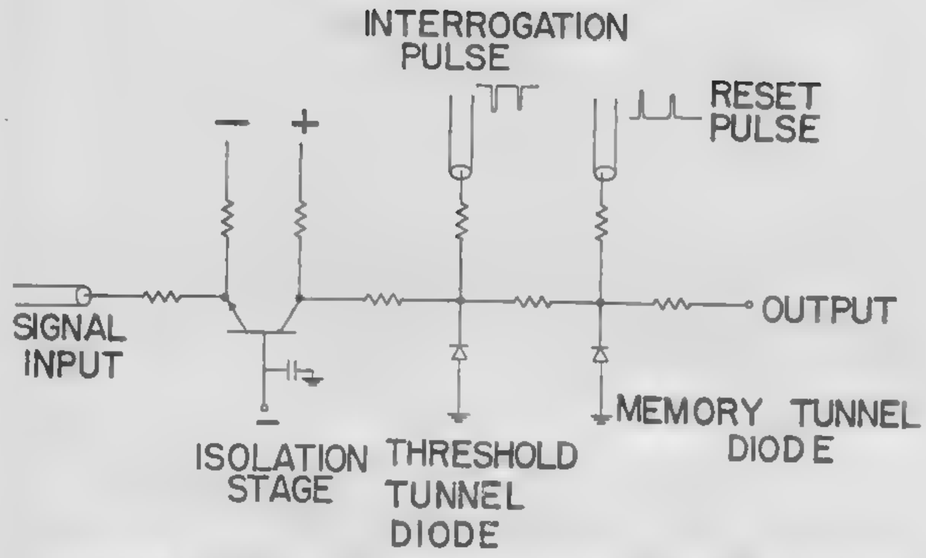


FIGURE 2—Sampling and threshold circuit. Sampling frequency is *50 Mc.*

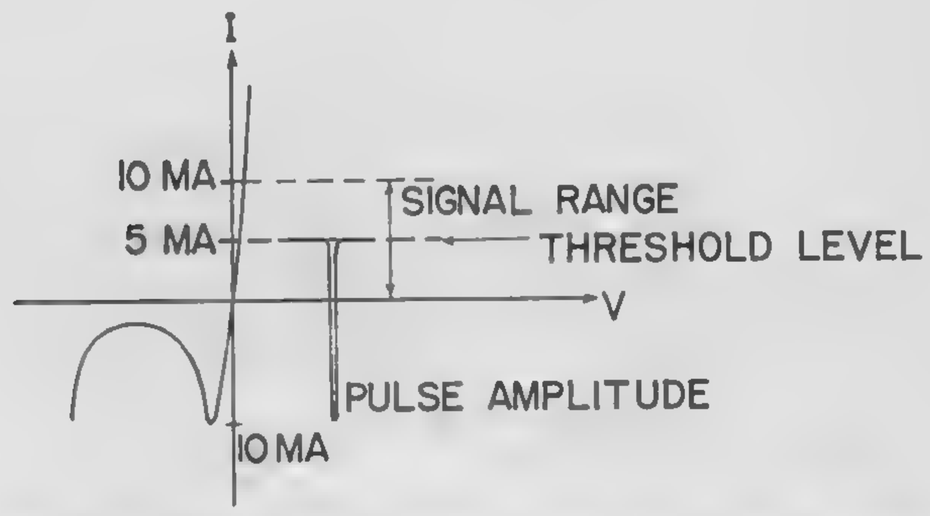


FIGURE 3—Current levels in threshold tunnel diode.

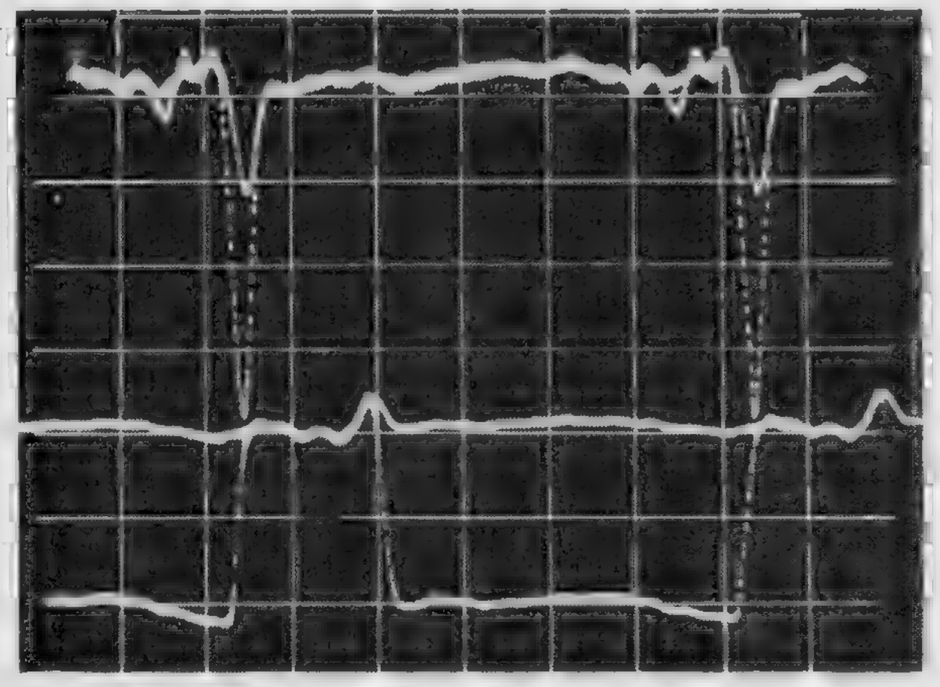


FIGURE 4—Upper Trace: waveforms across the threshold tunnel diode for signal currents below and above the threshold level. Lower trace: waveforms across the memory tunnel diode. Time from right to left, *3.3 nsec/div.*

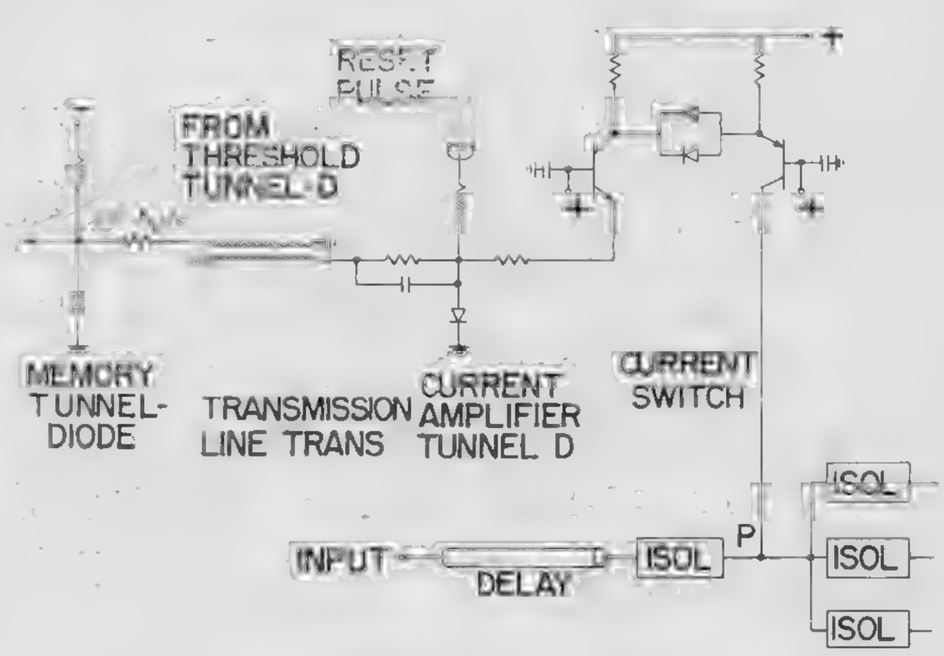


FIGURE 5—Weighting circuit generating a precise amount of current (*1%* accuracy) within less than *4 nsec.*

SESSION IX: Logic II

FAM 9.4: A Magnetic Film Analog-to-Binary Encoder

W. A. Barrett, T. R. Long and J. E. Schwenker

Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

A MAGNETIC FILM ENCODER, capable of encoding at video rates to five digit accuracy, has been built. Basically, the encoder consists of a magnetic wire enclosed in input and output windings. A single domain wall region, whose position is a function of the analog input, is established on the wire. The position of this wall region is detected and encoded by the output windings.

A working encoder, using a *0.005"* diameter copper wire electroplated with a *1μ*-thick axially oriented permalloy film, has been made[1]. A transverse (or *clock*) field is generated by a current in the wire; Figure 1*a*. The analog input current (to be encoded) is applied to a uniform solenoid (*62* turns/inch), and generates a uniform axial H field; Figure 1*b*. A constant bias current is applied to a solenoid (Figure 1*c*) wound so that a linearly-graded axial field is generated, with zero at the center, positive at one end, and negative at the other. The effect of these three fields on the film magnetization is shown in Figure 2. The initial state *(a)* is destroyed by the clock current *(b)*. When the clock current is removed in the presence of the analog and bias fields, the magnetization relaxes to state *(c)*, which contains a domain wall region[2]. This region forms where the analog and bias fields just cancel, and its position along the wire is determined by the magnitude of the analog current. The transitions from states *(a)* to *(b)* and *(b)* to *(c)* occur by rotation and can occur quite rapidly [3,4]. Hence, although a domain wall region appears, simple domain wall motion is not involved, so the speed of operation can be quite high. It should be noted that the direction of the clock current is unimportant, so that a sine wave or other convenient *ac* waveform may be used, resulting in two samples per cycle of the clock current.

To translate the domain wall position into a *Gray*-coded binary output, a set of output windings, each consisting of several 2-turn coils is placed along the magnetic wire; Figure 3. The polarity of the *emf* induced in each coil, when the domain wall region is formed, is determined by whether the domain wall region forms to the right or to the left of the coil. Adjacent coils for a particular digit are connected series-opposing to yield an output at clock time which varies up and down in voltage as the domain wall segment is moved along the wire. This is shown in Figure 4, in which the digit outputs at clock time for a typical five-digit encoder are displayed versus analog current. Since the domain wall region has some width, the transitions in output are not sharp. A regenerative threshold detector is therefore needed on each output digit winding.

A photograph of a prototype encoder is shown in Figure 5. The operating window for the fifth digit threshold detector (the worst case) is shown in Figure 6. Here the output is given for each of the *32* analog current values which lie exactly midway between the nominal transition values. If the regenerative detector threshold remains within this window, the encoder will be linear and accurate to ± ½ level. The sampling rate used here is 10_7 samples/sec, obtained by using a $5 \times 10_6$-*cps* sine-wave clock current.

The response to a step change in analog current occurs in one cycle, as indicated in Figure 7. It will be noted that the change is registered in the very next cycle and that only small further changes in output are seen in subsequent cycles.

Several residual noise effects must be eliminated for optimum performance. The analog winding back *emf*, *4-v* peak in the device described, should consist principally of a *10-Mc* component (for a *5-Mc* clock) due to the quadrature film switching process. This *emf* is proportional in size to the analog current. For this reason, an analog driver impedance of a few-hundred ohms is sufficient to maintain a low contamination of the analog current with current induced by the clock. A *5-Mc* component in the back *emf*, due to air coupling to the clock current, must be removed by balancing the clock driver to ground. Air coupling of the sense leads to the clock or analog current (signaled by a 5-Mc output component) must also be suppressed by rejecting the common-mode output and dressing the sense leads appropriately.

Acknowledgment

The authors wish to thank *A. C. Malacarne** and *D. W. Doughty* for the construction and initial testing of feasibility models.

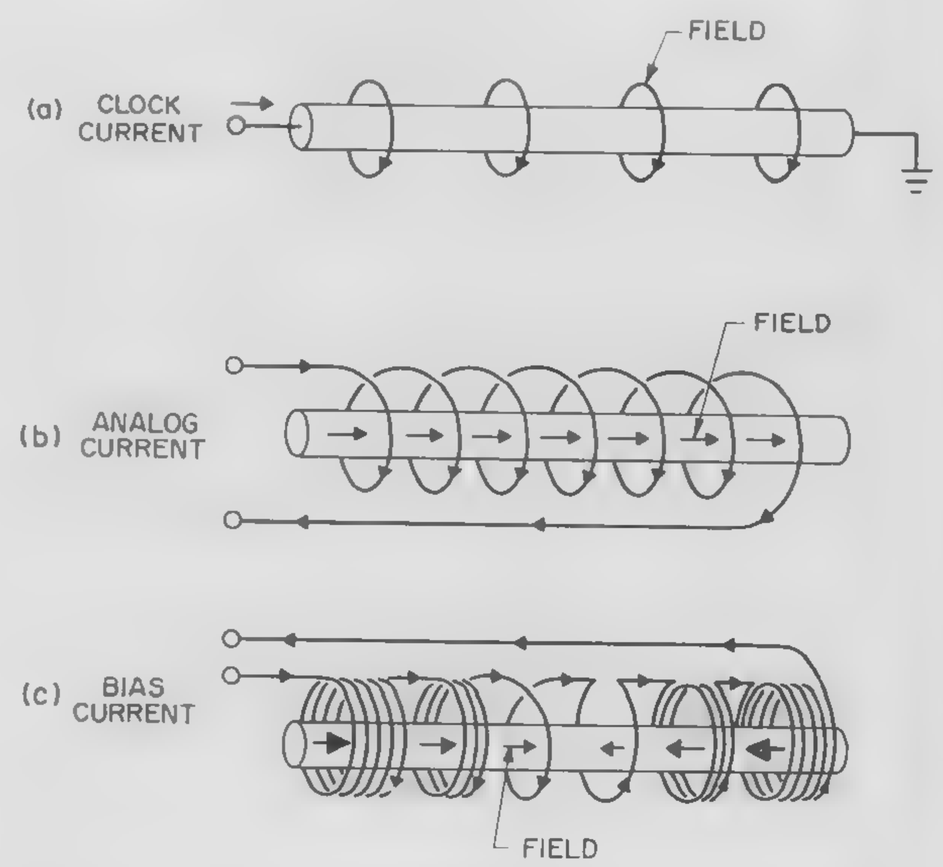


***FIGURE 1*—Input currents and their H fields for a magnetic film encoder: *(a)* clock, *(b)* analog (signal), and *(c)* bias.**

* Bell Telephone Company of Pennsylvania.

[1] Long, T. R., "Electrodeposited Memory Elements for a Nondestructive Memory," *J. Appl. Phys.* p. 1235; May, 1960.

[2] Crowther, T., *MIT Lincoln Lab. Group Report 51-2; ASTIA No. 255-697;* February, 1959.

[3] Dietrich, W., Proebster, W. E. and Wolf, P., "Nanosecond Switching in Thin Magnetic Films," *IBM J. Research and Development*, p. 189; April, 1960.

[4] Barrett, W. A., "Measurement of Film Relaxation Time," *Journ. Applied Physics;* to be published.

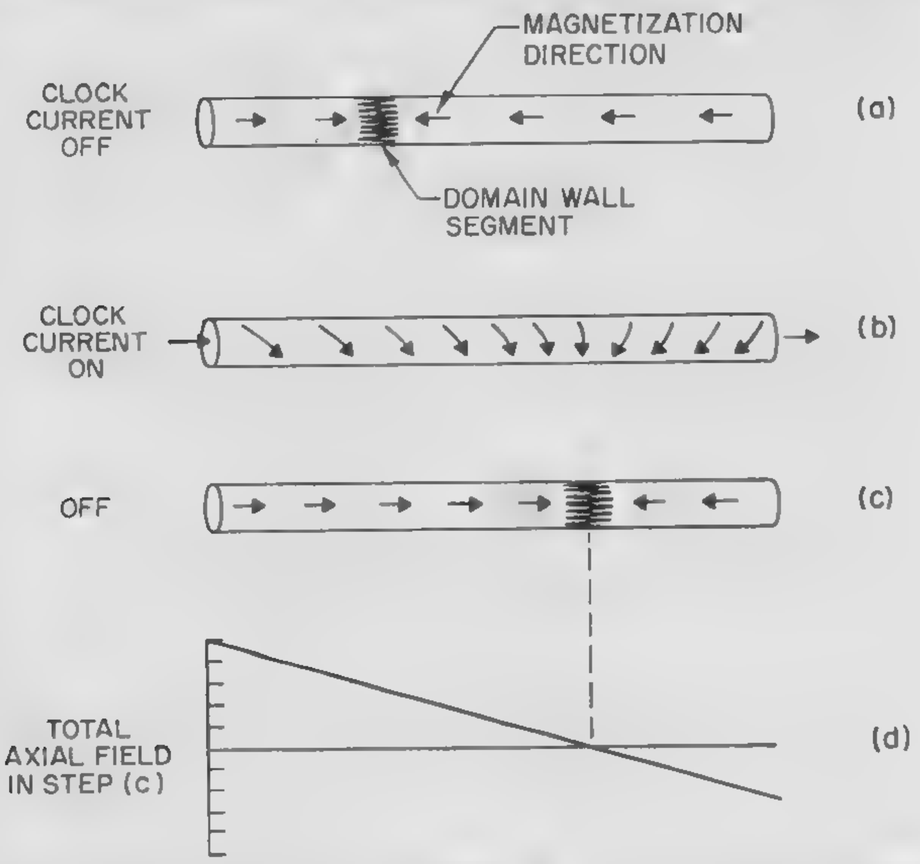


FIGURE 2—Spin directions in tensor film during encoding cycle: *(a)* initial state, *(b)* clock current on, *(c)* clock current off, and *(d)* axial-H field present in *(c)*.

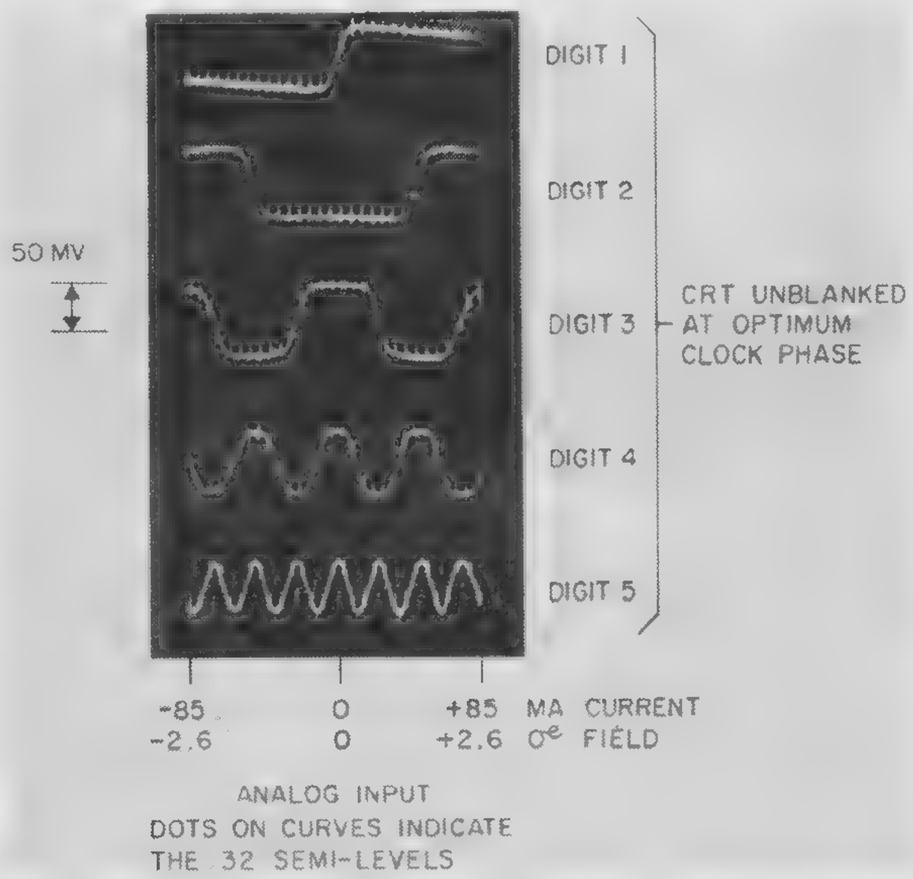


FIGURE 4—The five digit outputs (experimental). Analog current (slowly varying) horizontal, output vertical; clock field *5-Mc* sinusoid, *9-oe* peak.

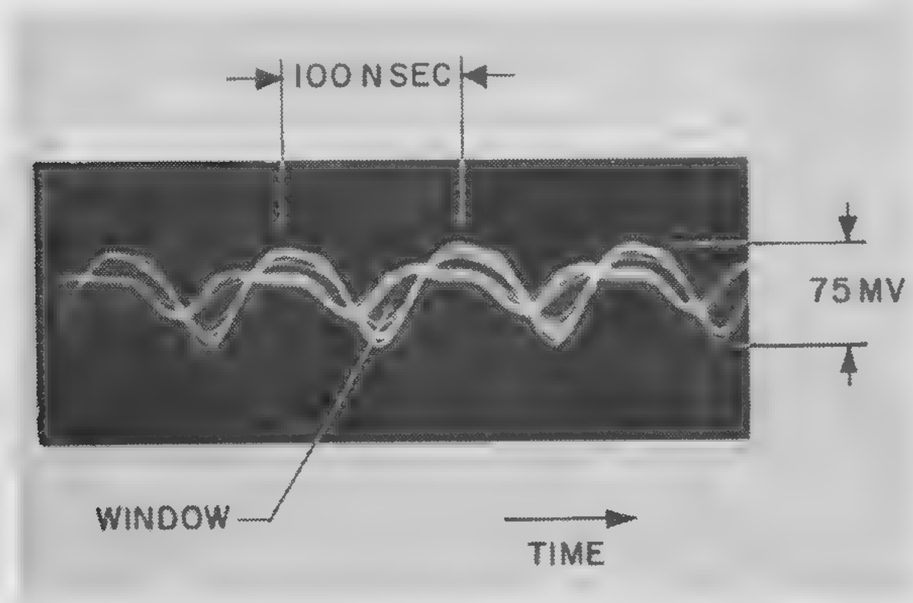


FIGURE 6—Detection window for fifth digit output. Output versus time for one cycle and all *32* analog current semi-levels.

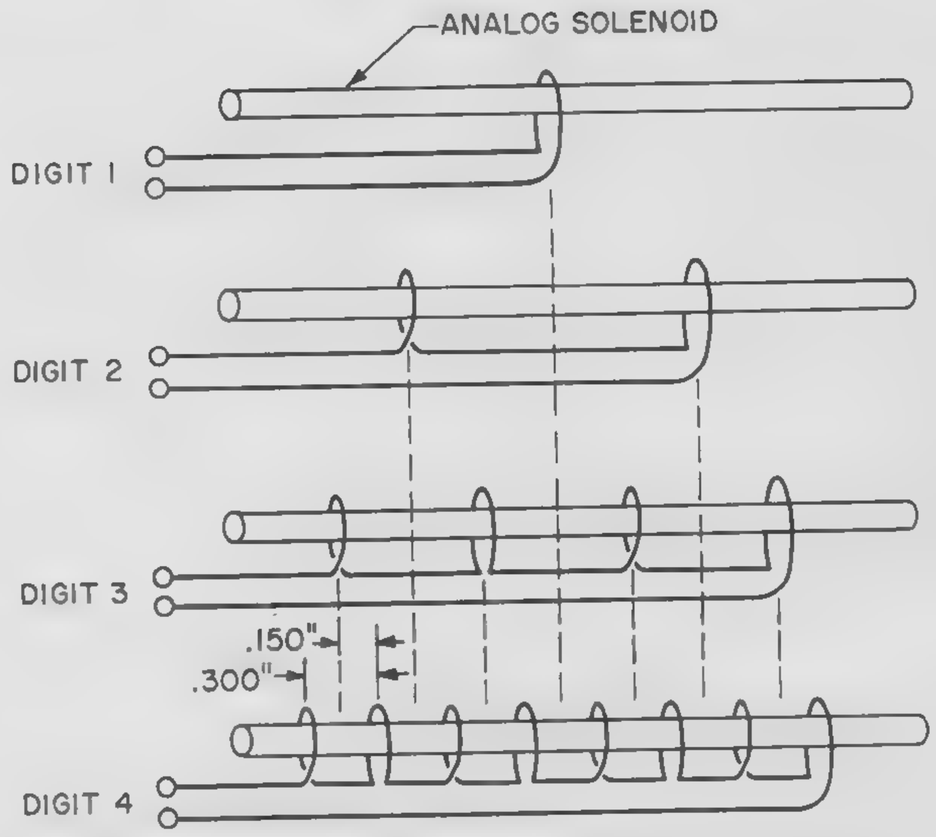


FIGURE 3—Encoder digit output windings to produce *Gray*-coded binary output.

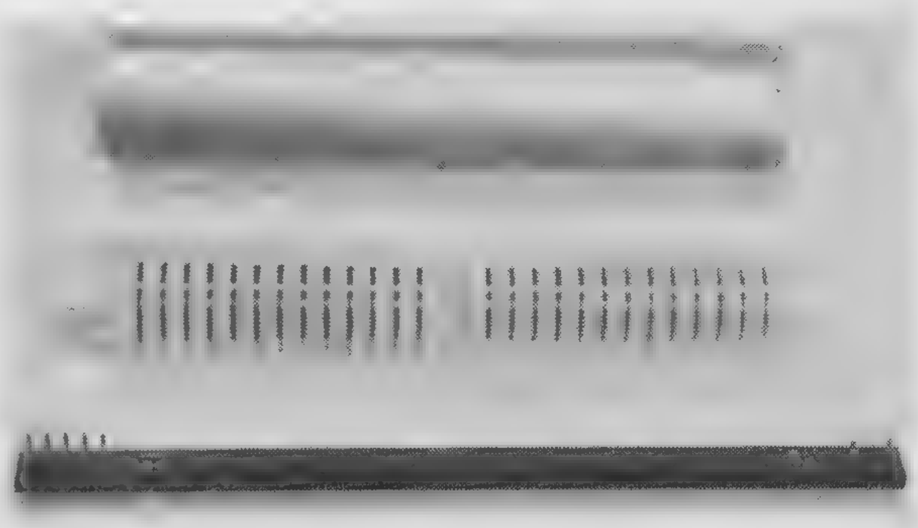


FIGURE 5—Photograph of encoder.

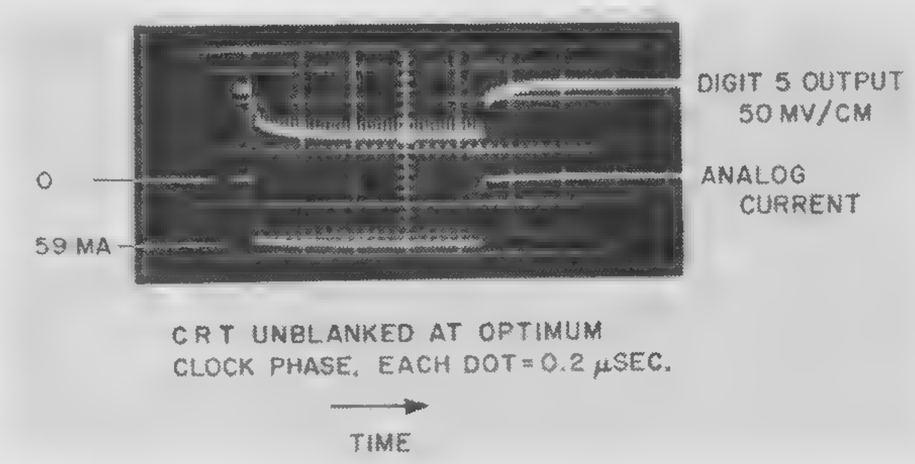


FIGURE 7—Response of encoder digit *3* output to step change in analog current: *(a)* analog current step, *(b)* output without step change, and *(c)* output with analog current step.

SESSION IX: Logic II

FAM 9.5: A Full Binary Adder Using Cylindrical, Thin-Film Logic Elements

G. W. Dick and D. W. Doughty

Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

THE CAPACITY of electrodeposited, cylindrical thin-film elements for performing the basic logical operations required in digital machines has been demonstrated[1]. Specifically, the two-lattice configuration shown in Figure 1, represents a one-bit memory and delay stage which can be connected in tandem to other similar sections to form a shift register driven by a four-phase clock.

A bit of information is stored in each cylindrical film element of a single lattice as a uniform clockwise, or counterclockwise magnetization condition (for *ones* or *zeros*, respectively) along a circumferential, easy, magnetic axis[2]. Alternate lattice sections, not storing information during a particular period, are magnetized in the film hard directions by solenoidal drive fields. On transferring information from one lattice section to the next, two phases are required. On the first (Figure 1) wires A_1 and C_1 are reset by applying solenoidal field current I_{A1} and I_{C1}. At this time solenoidal fields are relaxed on wires A_2 and B_2. During the second phase a similar transfer is performed from wires B_1 and D_1 to wires C_2 and D_2. Note that several sections can be interconnected as a shift register. Directivity of information flow and isolation between adjacent bit signals are obtained inherently through symmetries in the lattice and the phasing of the drives. Typical drive currents are shown in Figure 2.

As a result of the rotational, single-domain behavior of the film elements, complete flux transfers are achieved typically in a *50-nsec* interval; with drive pulse rise/fall times $\approx$ *30 nsec*.

Due to connecting wire impedance, transmitting and receiving element voltages are not equal at all times during transfers; thus, common or longitudinal mode voltages $V_{a1} + V_{a2}$ and $V_{d1} + V_{d2}$ are produced in transfers from section *1* to *2*; Figure 3. Since these components can accumulate over a number of tandemly-connected sections, transformers or other decoupling means are required to break any closed loop information paths in a system. Common mode currents which would unbalance the system are thereby suppressed.

Fan-outs of at least four are found to be reliably attainable. Combinatorial operations generally required in a sequential machine are realizable with majority logic gates and inversion means [3,4] as shown in Figure 5. Sufficient gain to permit fan-in and fan-out is obtained through signal regenerating action obtained in the wire elements themselves. Current waveforms in Figure 4 indicate the detrimental effects of fan-out and majority fan-in on the net signal current to one receiving lattice. Despite reductions in input current, relative to that of a simple *1:1* transfer, the output voltages obtained on subsequent phases are identical.

Signal path wiring and film elements used in the binary adder are shown in Figure 6. The organization is based on the use of a three-input majority gate M_3 to produce the carry signal, and a five-input gate M_5 to produce the sum[3,4]. Lattice sections D_1, D_2 and D_3 are used to obtain signal delays. Carry and sum majority operations can be represented symbolically as:

$$C(i) = A(i) \# B(i) \# C(i\text{-}1)$$

$$S(i) = A(i) \# B(i) \# C(i\text{-}1) \# 2\,\overline{C}(i)$$

where the operational signs refer to an arithmetic rather than *Boolean* summation, and each function is limited, in magnitude, to one unit by saturation. The signal $2\,\overline{C}(i)$ is obtained by reversing the sense of $C(i)$ and performing a fan-out into two gate inputs.

Bit patterns measured, as shown in Figure 7, with the adder operating at *1 Mc*, indicate the capacity of the system to handle the specified conditions of fan-in *(5)* and fan-out *(4)*. It appears that the drivers and the physical layout of the present circuitry are not commensurate with the high-speed switching ability of the films themselves, and it is expected that future improvements will produce higher bit rates.

Acknowledgments

The authors are indebted to *J. E. Schwenker, T. R. Long, R. M. Wolfe, K. V. Mina,* and *W. D. Farmer* for their assistance in this project.

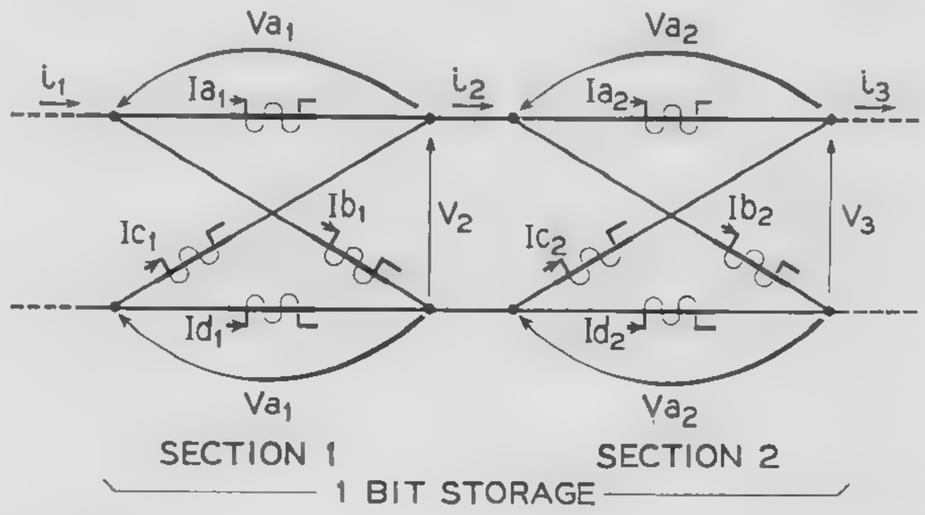


***FIGURE 1*—One-bit lattice shift register connections. Film—*81%* Ni *19%* Fe, *1*-micron thick. Diam.—*.005"*, active length—*0.2"*.**

[1] Wolfe, R. M., "A Cylindrical Thin Film Shift Register and Compatible Logic Circuitry," *Conference on Ultrafast Computing Techniques,* Lake Arrowhead, Calif.; August 7-10, 1962.

[2] Long, T. R., "Electrodeposited Memory Elements for a Nondestructive Memory," *J. Appl. Phys.* 31, p. 1235; 1960.

[3] Lindaman, R., "A New Concept in Computing," *Proc. IRE,* p. 257; Feb., 1960.

[4] Akers, Jr., S. B., "Synthesis of Combinatorial Logic Using Three-Input Majority Gates," *AIEE Third Annual Symposium on Switching Circuit Theory and Logical Design,* p. 150-157.

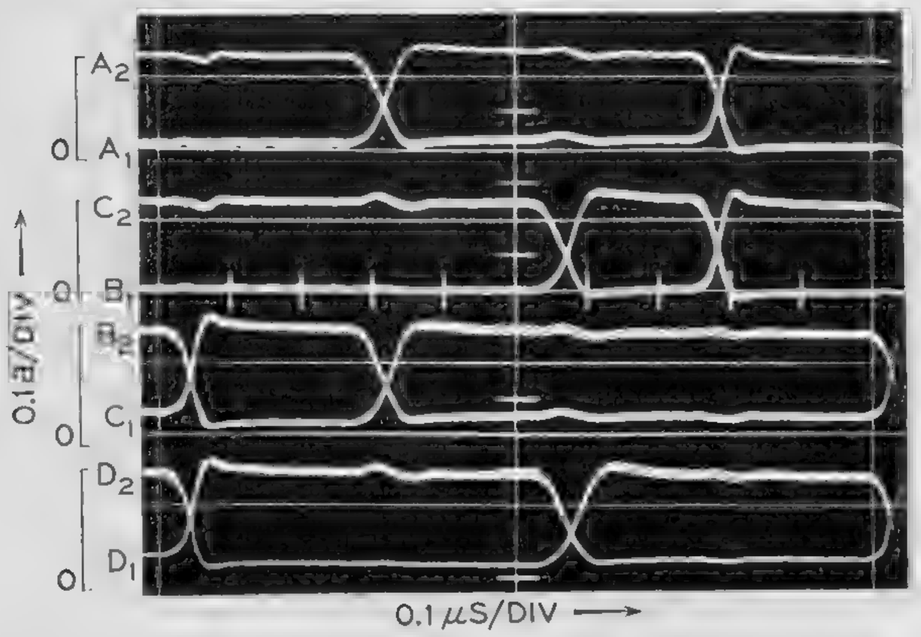


FIGURE 2—**Solenoid drive-current waveforms, for a one-bit shift interval. Solenoid data: *n—50* turns, length—*0.2"*, inside diameter—*.015"*; H_k = *2.0 oersteds.***

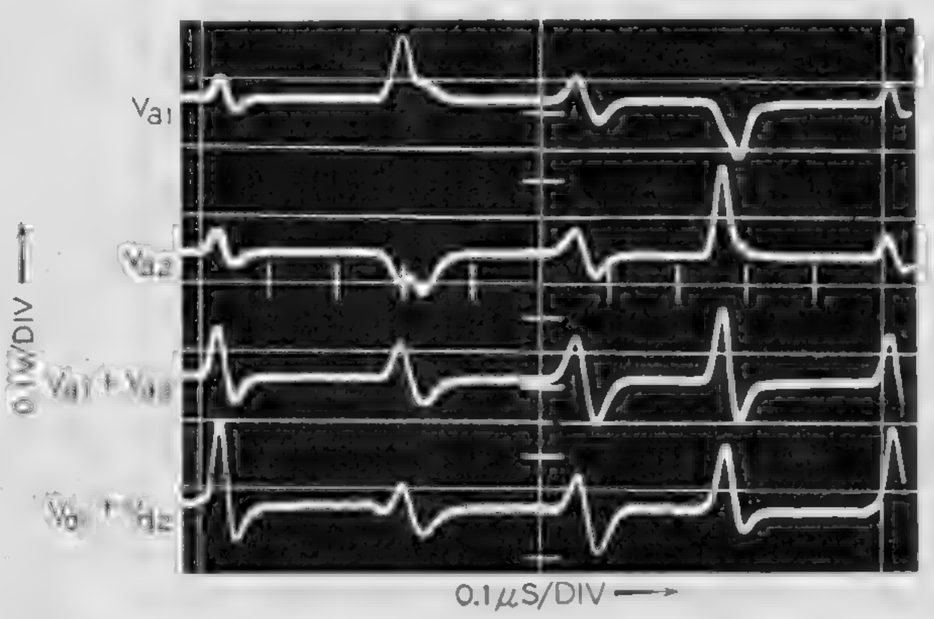


FIGURE 3—**Transmitting and receiving element voltages, showing the generation of common mode potentials through a single bit, reentrant register; Figure 5*a*.**

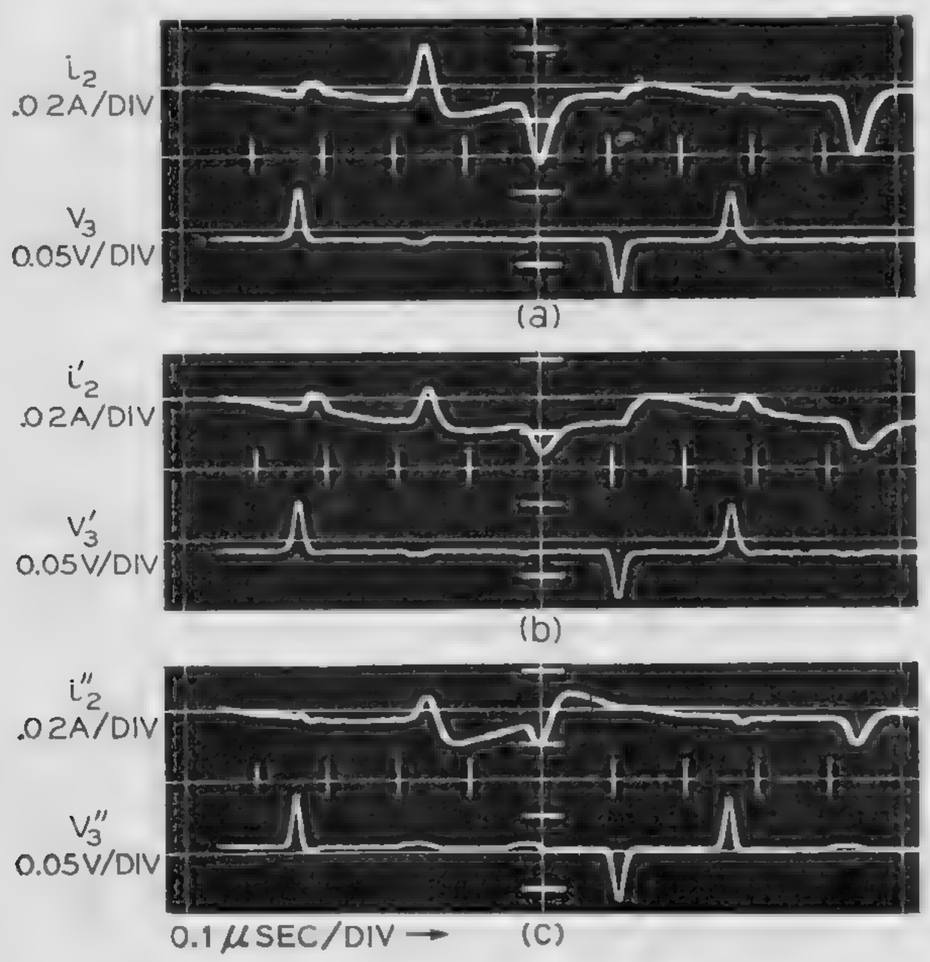


FIGURE 4—**Input (tipping) currents and output voltages of a lattice section after: *(a)*—normal transfer, *(b)*—fan-out of three, and *(c)*—fan-in or majority operation of three inputs.**

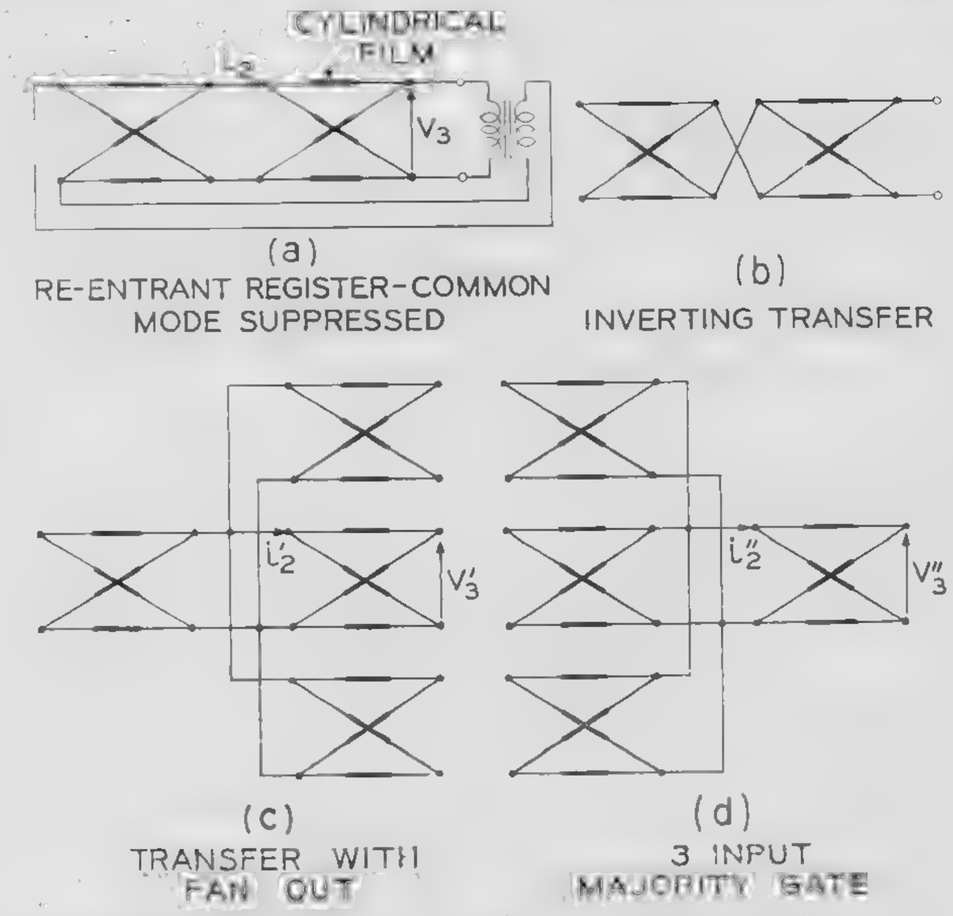


FIGURE 5—**Transfer and logical connections for lattice elements; solenoidal drive windings not shown.**

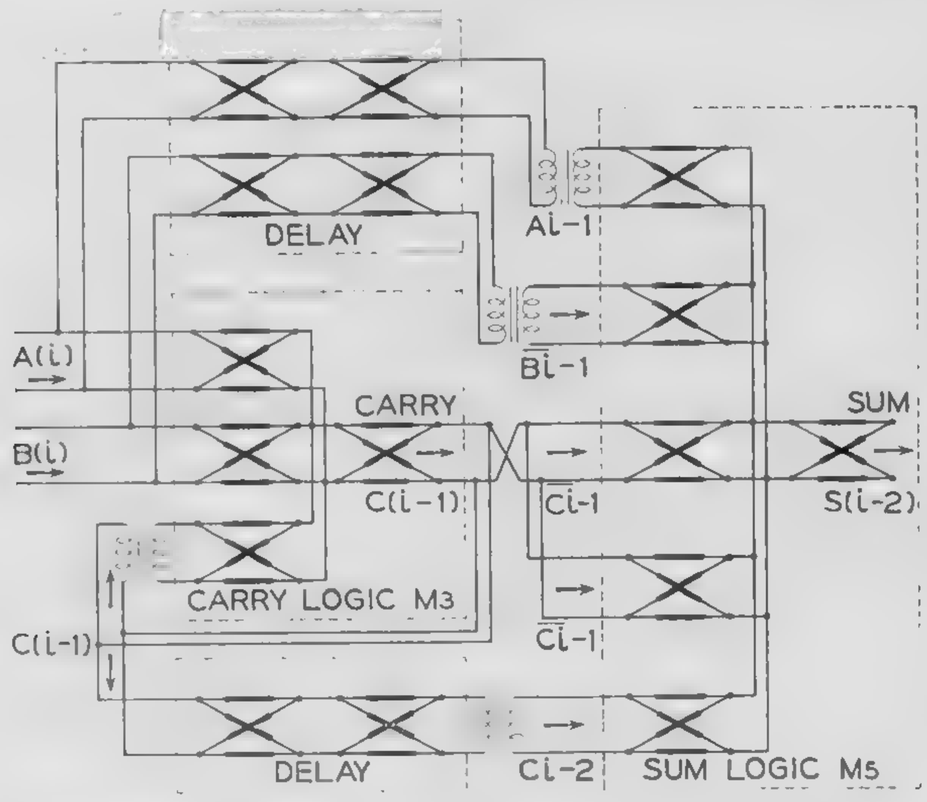


FIGURE 6—**Thin, cylindrical-film, serial binary adder using three- and five-input majority gates.**

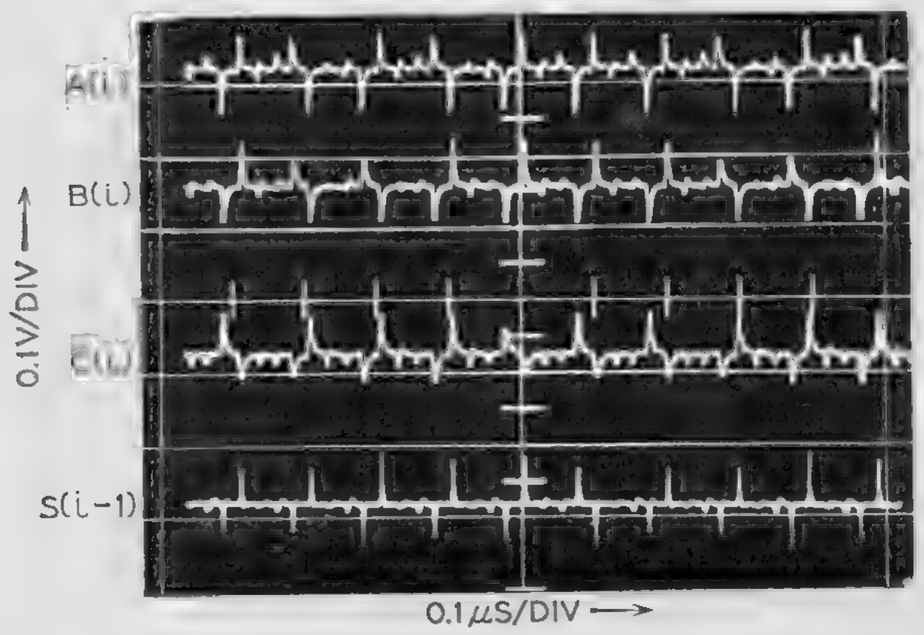


FIGURE 7 — **Input and output signal waveforms for the binary adder operating at *1-Mc* bit rate. *A(i)* = *010100*, *B(i)* = *011000*, and *S(i-1)* = *000001*. Absicca scale is *1.0 μs/div*.**

SESSION X: Linear Circuits

Chairman: R. L. Pritchard

Texas Instruments, Inc., Dallas, Tex.

FAM 10.1: Signal Processing with Parametric Delay Lines

A. R. Owens and K. A. Hughes

University College of North Wales

Bangor, United Kingdom

A PARAMETRIC delay line using fixed inductors and silicon diodes as variable capacitors has been described[1]; Figure 1*a*. Here the delay of the line is varied by the instantaneous signal voltage to produce a desired form of signal distortion.

Where the delay is required to be independent of the signal voltages, a bridge arrangement can be used; Figure 1*b*. Capacitance variation of a pair of diodes in the bridge arrangement is shown in Figure 2. Signal levels of *1-2 v* can now be handled without affecting the characteristics of the line, and the delay of the line can now be varied by varying the applied bias levels. This arrangement is used in some tape recording applications to obtain small changes in delay times.

In the present application large and rapid changes of bias (the pump) take place while a small signal is being transmitted along the line. The effect is to change almost instantaneously the value of capacitances in a linear transmission line, which can be represented by the equivalent circuit of Figure 3a.

Once a signal pulse has entered the transmission line it exists as a charge wave distributed in space, its velocity u_1 being determined by the line constants C_1 and L. If now the bias is suddenly changed so that the capacitance is changed to C_2, the velocity characteristic of the line is changed to a new value u_2. As the capacitance changes occur simultaneously at all points along the line, the spatial distribution and charge remains unchanged. But due to the change in velocity the time dimension of the output waveform is altered; Figure 3*b*. Thus, if the line capacitance is increased while the signal is traveling in the line, the velocity decreases, and the output signal is of greater duration than the input signal. Conversely, a signal pulse can be shortened by reducing the capacitance.

The rise time of the pump pulse is not critical, the only requirement being that the change of bias should be completed before the signal begins to emerge from the line. This type of line has been coded *simpump* as the pump is being applied to all points simultaneously.

A second type of line can now be considered, where, instead of changing the bias levels simultaneously at all points of the line, a progressive change of bias is obtained by means of a second, fixed parameter transmission line; Figure 4*a*. This is called a *distripump* line. In this case, when the signal exists in the signal line as a space wave, a pump pulse can be applied to the pump-line to chase and overhaul the signal. When this happens, the change will occur at the tail of the signal wave before its head is affected, Figure 4*b*, so that the time change can now be made greater for the same change in amplitude obtained previously.

Thus, in the *simpump* line, if the ratio of capacitance change is C_2/C_1 then the pulse duration is changed by a factor $u_1/u_2 = \sqrt{C_2/C_1}$, where u_2 and u_1 are final and initial line velocities. In the *distripump* line, the pulse duration changes by a factor

$$\frac{u_3/u_2 - 1}{u_3/u_1 - 1}.$$

where u_3 is the velocity of the pump line. The minus signs change to plus signs if the direction of travel of the pump is changed to meet the signal instead of chasing it; *reversed distripump*. These lines are being used to achieve pulse expansion and compression in the nanosecond region. The *distripump* line gives a greater time change than the *simpump*, if the available capacitance change is limited, as is the case at present.

Figure 5 shows the effect upon a signal pulse of a *3:1* change in capacitance. It will be noted that there is a change in amplitude in the processed pulse.

Detailed calculation shows that for the *simpump* line a signal segment of amplitude v_1 becomes two components

$$\vec{V_2} = \tfrac{1}{2} C_1/C_2 \left(1 + \sqrt{C_2/C_1}\right) V_1 \text{ and}$$

$$\overleftarrow{V_2} = \tfrac{1}{2} C_1/C_2 \left(1 - \sqrt{C_2/C_1}\right) V_1$$

after a bias change. Only V_2 is of interest here. Typical C_1/C_2 ratios of *4:1* and *1:4* give values of $\vec{V_2}$ of $3V_1$ and $3V_1/8$, respectively. Note that if the two operations were performed successively in the same line, the resulting pulse width would be restored to its original value, but the final signal amplitude would be increased by a factor of *9/8*. It is therefore proposed to use such a system for pulse amplification.

For a distripump line, calculation gives the same expressions for $\vec{V_2}$ and $\overleftarrow{V_2}$ as before. The stretching of the forward pulse, however, is now given by

$$\frac{u_3/u_2 - 1}{u_3/u_1 - 1}$$

The pulse going in with duration T_1 had a charge content proportional to $V_1T_1C_1u_1$. The emergent charge is proportional to $\vec{V_2}T_2C_2u_2$ which is

$$\tfrac{1}{2} V_1 C_1 T_1 \left(1 + \sqrt{C_2/C_1}\right) u_2/u_1 \left(u_3/u_2 - 1\right) \Big/ \left(u_3/u_1 - 1\right).$$

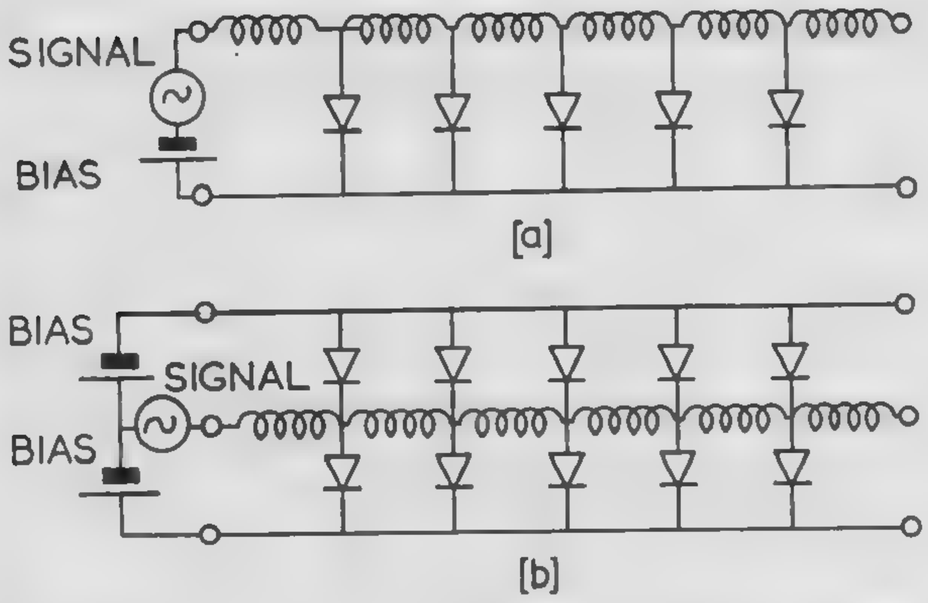
There is therefore a charge gain.

Typically, with $C_2 = 4\ C_1$, and $u_3 = 4\ u_2$, the output charge is $2.25\ V_1C_1T_1$, a gain of *2.25*. There is now the possibility of restoring the time dimension to its initial value using either *simpump* lines or *reverse distripump* lines, and there should be a considerable increase in the final signal amplitude.

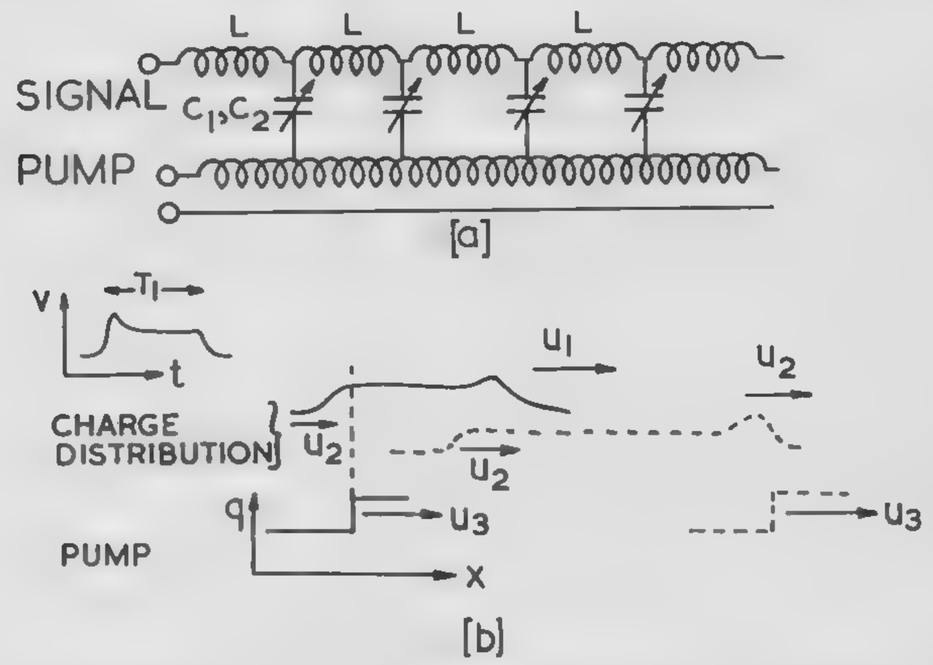
Thus in the example quoted the output pulse is of amplitude $\frac{3}{8}\ V_1$ and duration $3\ T_1$. Restoring the original time dimension requires: *(a)*—one *simpump* line with $C_1 = 9\ C_2$, or *(b)*—two *simpump* lines with $C_1 = 3\ C_2$. Taking the second case, as being more practicable, the output voltage in each is *2.4* times the input voltage. The whole chain should therefore have a gain of $\frac{3}{8} \times 2.4 \times 2.4 = 2.15$. Alternatively, reverse *distripump* lines could be used to restore the pulse to its original time duration. Using the foregoing typical figures such a line should give a pulse compression of *0.6*, with a voltage gain of *3*. Two stages of *reverse distripump* line following the first *distripump* line should therefore give a time relationship of $3 \times 0.6 \times 0.6 = 1.08$, with a gain of

[Continued on page 123]

[1] Riley, R. B., "Analysis of a Nonlinear Transmission Line," *Int'l. Solid-State Circuits Conf. DIGEST of TECHNICAL PAPERS*, p. 10-11; Feb., 1961.



FIGURES 1a and b—Nonlinear transmission lines using silicon diodes as variable capacitors sensitive to both signal and bias are illustrated in *(a)*. Bridge type of line with transmission characteristics controlled only by bias is shown in *(b)*.



FIGURES 4a and b—A parametric line with distributed pump is in *(a)*. Conditions in line as *(i)* pump step passes tail of signal pulse (full line) and *(ii)* pump step catches up with head of signal pulse (dotted line) appear in *(b)*.

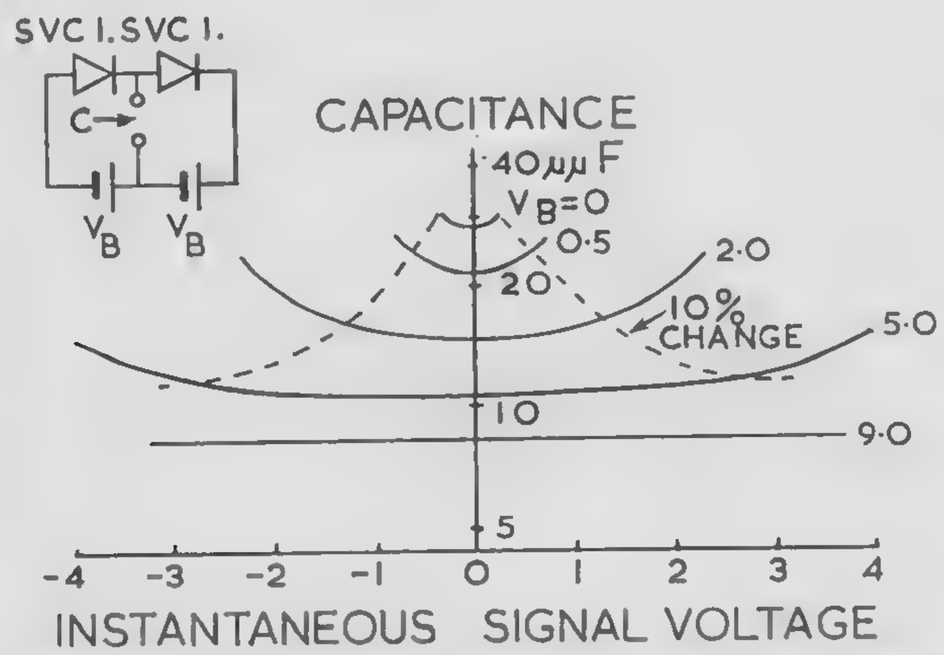


FIGURE 2—Variation of capacitance with signal voltage for a pair of back-to-back diodes. The dotted line indicates a change of capacitance of *10%*.

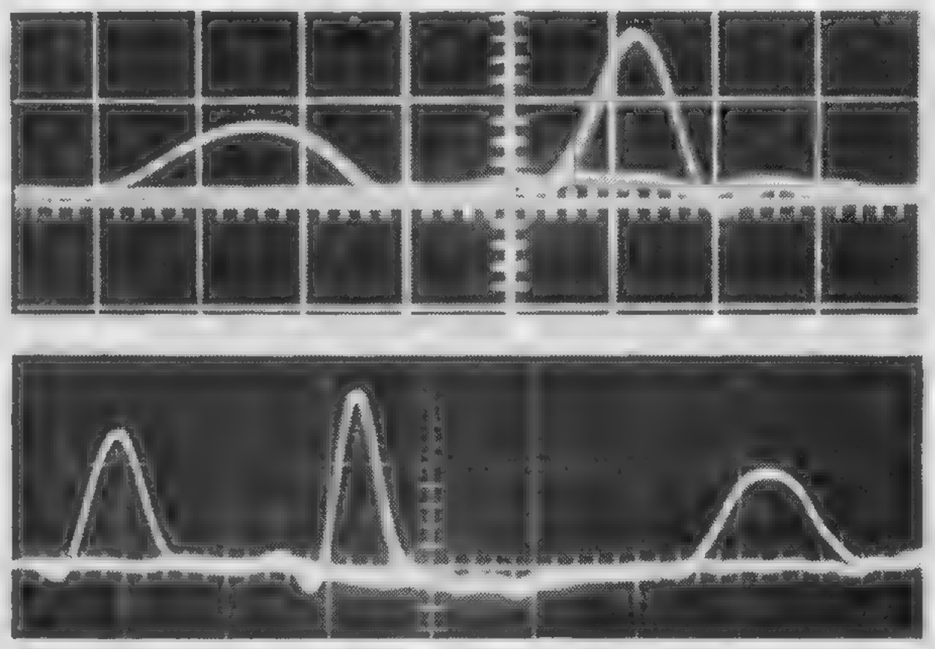
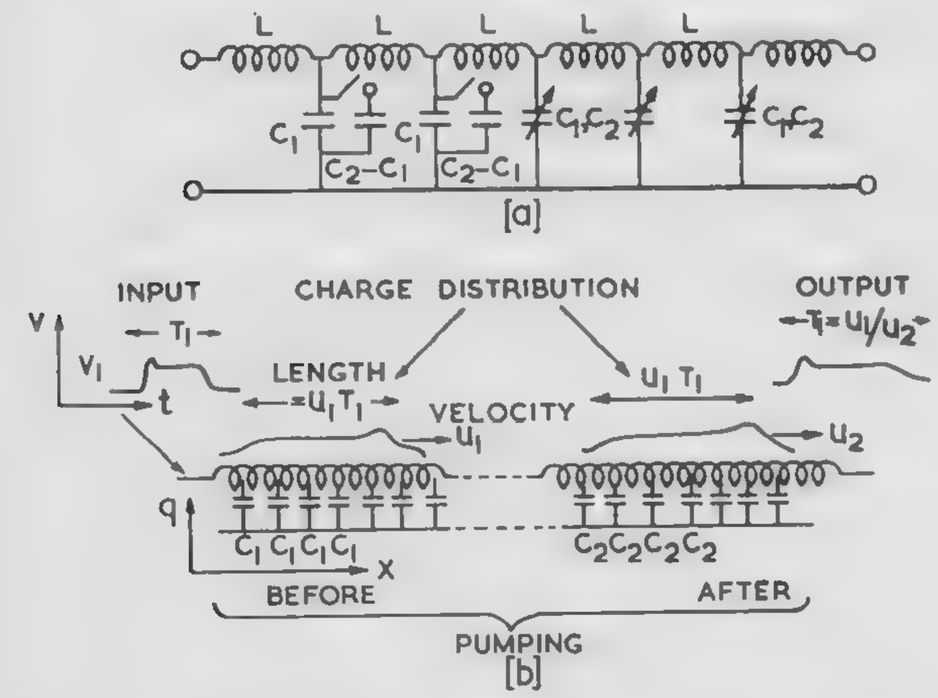


FIGURE 5a and b—Typical waveforms showing, at top, pulse compression in distripump line, and, below, compression and expansion in a reverse distripump line.



FIGURES 3a and b—Equivalent circuit, corresponding to low and high bias conditions is illustrated in *(a)*. Conditions in the line before and after a rapid bias change are shown in *(b)*. Charge distribution remains unchanged, but velocity changes from u_1 to u_2.

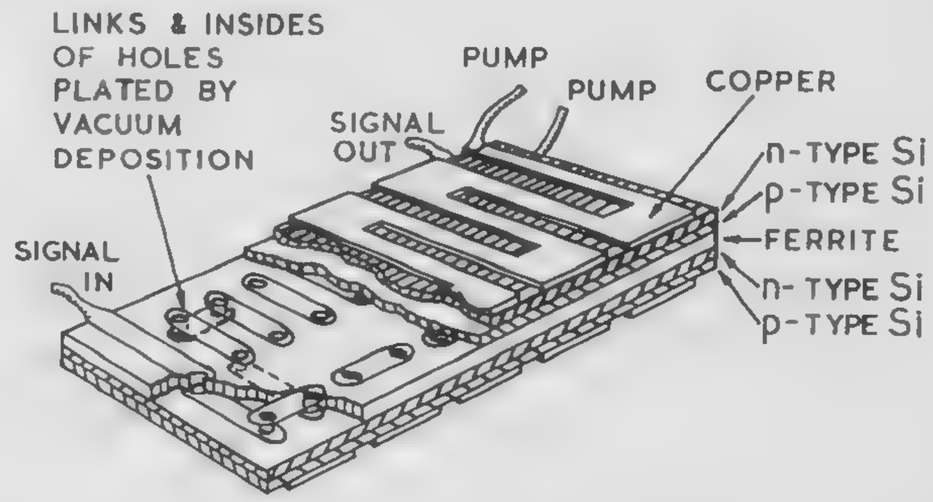


FIGURE 6—Proposed solid circuit structure using vacuum deposition techniques. The silicon layers can be multicrystalline and of high resistivity to prevent coupling between adjacent diode sections, as only variable capacitance is required.

SESSION X: Linear Circuits

FAM 10.2: Gain Characterization of High-Frequency Linear-Amplifier Devices

M. M. Hower

Bell Telephone Laboratories, Inc.

Laureldale, Pa.

SMALL-SIGNAL power gain measurements of active devices at high frequencies involve ambiguities due to the effects of internal feedback, making it difficult to measure accurately and isolate critical device parameters.

An extensive search for a definitive gain measurement has led to the definition of a new device parameter called *Gain Figure*. Specifically: *GF = (Forward Gain) × (Reverse Loss)*.

A rigorous analysis of a two-port shows that the product of forward gain and reverse loss is equal to:

$$\left| y_{21} \Big/ y_{12} \right|^2$$

and is independent of the source and load admittances. Moreover, a slight extension of the analysis shows that *GF* is independent of *y*, *h*, and *z*, i.e., *h* and *z* parameters may be substituted directly and

$$GF = \left|\frac{y_{21}}{y_{12}}\right|^2 = \left|\frac{h_{21}}{h_{12}}\right|^2 = \left|\frac{z_{21}}{z_{12}}\right|^2$$

This immitance invariance is quite important, for it means we can measure the *Gain Figure* of a device including input and output coupling networks and get the same result with any other reciprocal coupling networks*. In particular, in Figure 2*a* the measured *Gain Figure* is the same with and without N_1 and/or N_2 included.

A simple example is the common emitter transistor amplifier gain variation with collector load resistance. When R_L is large, we expect a better match to the transistor and consequently more forward gain than for small R_L. But, when there is a better match to the load, more power can be transferred into the transistor from a source in series with R_L so that the reverse loss decreases. The analysis shows both effects to be exactly equal. Consequently any increase in *Forward Gain* must be accompanied by an equal decrease in *Reverse Attenuation*.

*Mason*** has defined *Unilateral Gain, U*, as the *Maximum Available Gain* of an active device when y_{12} has been made zero. Moreover, he has shown that it is independent of the lossless network containing the device and that it can be achieved entirely by lossless coupling. Thus, the internal feedback of a device may be represented entirely by a passive network (Figure 2*b*) and the device can be thought of in the usual feedback terms. For conjugately matched y_S and y_L,

$$\text{Power delivered to } y_L = \left|e_o\right|^2 G_L$$

$$\text{Power available from source at } y_S = \left|e_i\right|^2 G_S$$

and

$$\textit{Forward Gain} = \left|\frac{e_o}{e_i}\right|^2 \frac{G_L}{G_S} = \left|\frac{\mu}{1-\mu\beta}\right|^2 \frac{G_L}{G_S}$$

In addition, from general feedback theory it can be shown that

$$\frac{G_L}{G_S} = \frac{G_{22}}{G_{11}}$$

where G_{11} and G_{22} are the real parts of the input and output admittances, respectively, of the unilateral amplifier represented above by μ. Substituting this in the expression for *Forward Gain* and making use of the fact that

$$U = \left|\mu\right|^2 \frac{G_{22}}{G_{11}}$$

it follows that

$$\textit{Forward Gain} = \frac{U}{\left|1-\mu\beta\right|^2}$$

Similar reasoning leads to

$$\textit{Reverse Gain} = \frac{B}{\left|1-\mu\beta\right|^2}$$

where

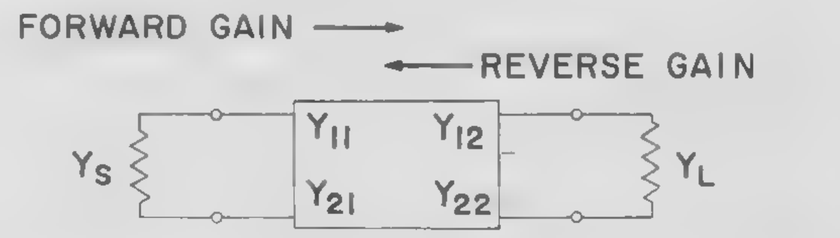
$$B = \left|\beta\right|^2 \frac{G_{11}}{G_{22}}$$

Therefore, for conjugately matched y_S and y_L,

$$GF = \frac{U}{B}$$

But, *GF* is independent of y_S and y_L. Therefore, the passive network represented by *B* is completely specified

[Continued on page 123]



$$\text{POWER GAIN} = \frac{\text{POWER DELIVERED TO LOAD}}{\text{POWER AVAILABLE AT SOURCE}}$$

$$\text{FORWARD GAIN} = /Y_{21}/^2 \frac{(Y_S + \overline{Y}_S)(Y_L + \overline{Y}_L)}{/(Y_{11}+Y_S)(Y_{22}+Y_L) - Y_{12}Y_{21}/^2}$$

$$\text{REVERSE GAIN} = /Y_{12}/^2 \frac{(Y_S + \overline{Y}_S)(Y_L + \overline{Y}_L)}{/(Y_{11}+Y_S)(Y_{22}+Y_L) - Y_{12}Y_{21}/^2}$$

FIGURE 1—Comparison of *Forward Gain* and *Reverse Gain* for a two-port.

* Circuits bridging the active device externally are not permitted.

** Mason, S. J., "Power Gain in Feedback Amplifiers," *IRE PGCT Transactions*, p.20-25; June, 1954.

*** In an investigation of stability, *Rollett* defined *k* in terms of immitance parameters and wrote the equation for G_{max} in a convenient form for this application: Rollett, J. M., "Stability and Power-Gain Invariants in Linear Two-Ports," IRE PGCT Transactions, p. 29-32; March, 1962.

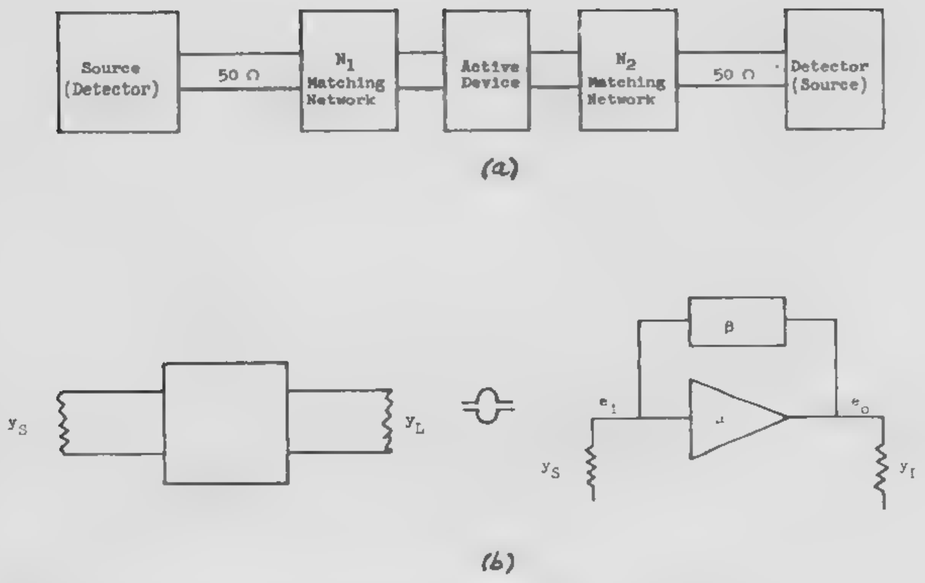


FIGURE 2a and *b*—Circuit diagram *(a)* illustrating gain figure independent of N_1 and N_2. A two-port represented as a feedback amplifier is shown in *(b)*.

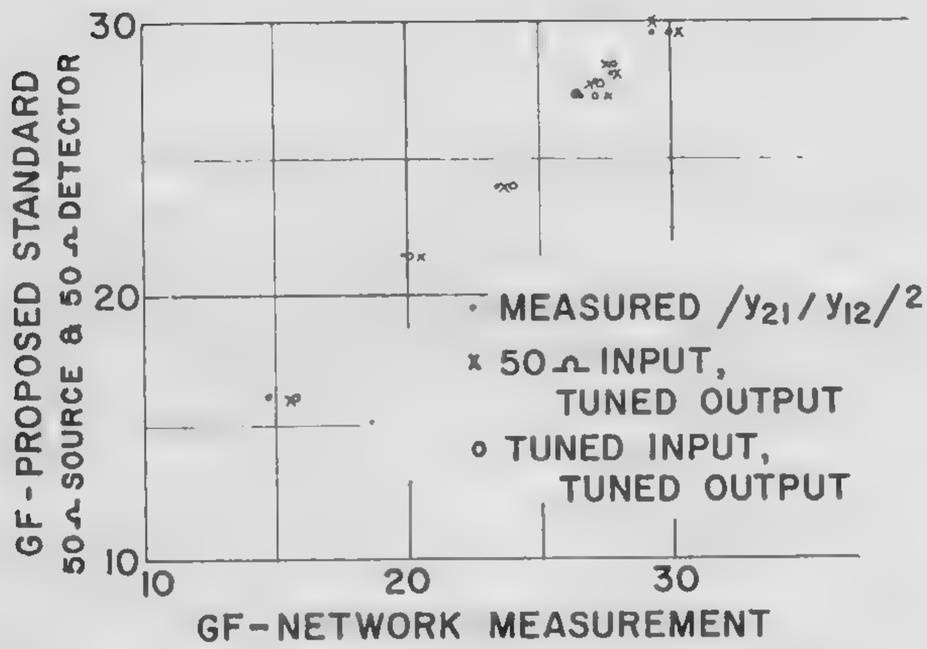


FIGURE 3—A *1000-Mc* common base gain figure (L-2255) showing agreement between the network measurements and the proposed standard.

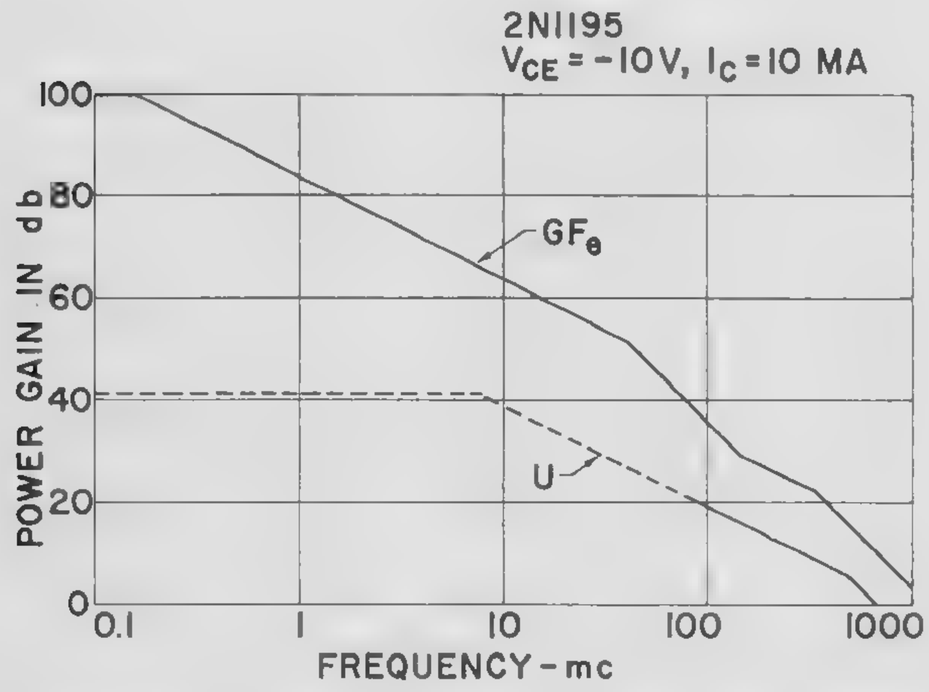


FIGURE 4—Typical unilateral gain and common emitter gain figure.

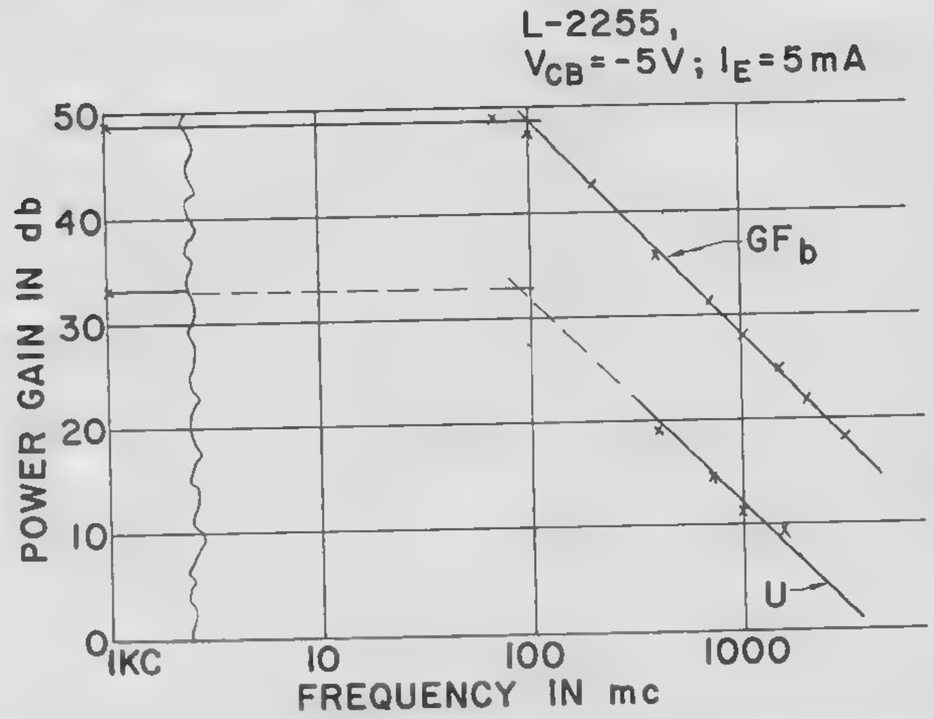


FIGURE 5—Typical unilateral gain and common-base gain figure.

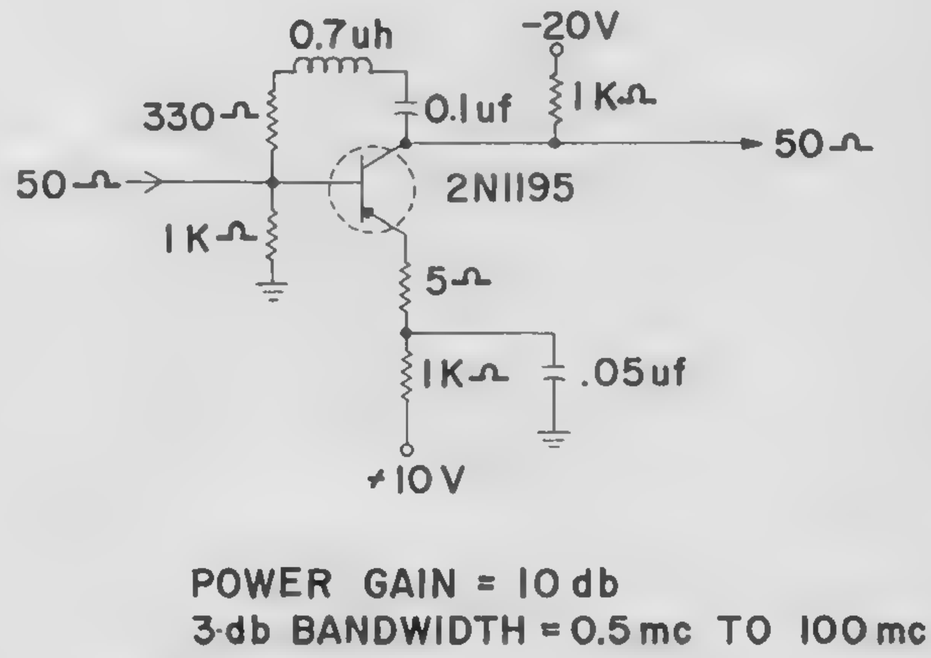


FIGURE 6—Wideband amplifier with feedback adjusted to provide flat *U* and *GF* (for amplifier) over the frequency range.

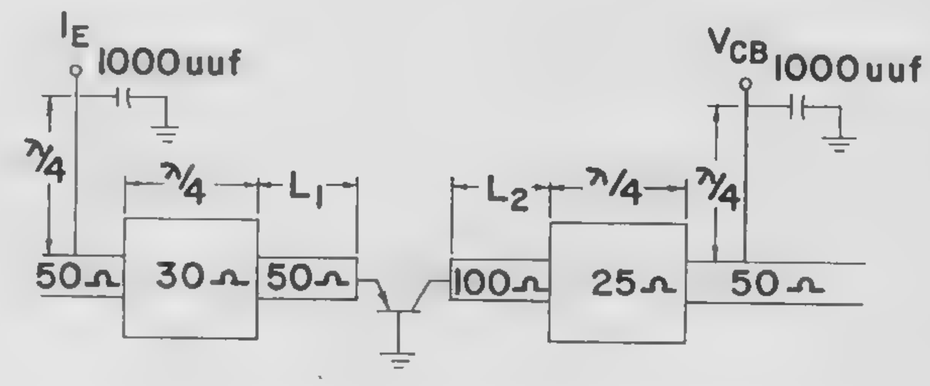


FIGURE 7—A *1000-Mc* stripline amplifier used for measurement of gain figure and maximum stable gain.

SESSION X: Linear Circuits

FAM 10.3: A Circuit and Noise Model of the Field-Effect Transistor*

N. G. Bechtel

Stanford Electronics Laboratory

Stanford, Calif.

THE FIELD-EFFECT TRANSISTOR may be viewed on a small-signal basis as a *RC* transmission line with gain from source to drain. A field-effect transistor structure is shown in Figure 1. A two-section, lumped-element approximation to the line can be derived by dividing the transistor into two sections, the one nearer the source having a fractional length λ, and the one nearer the drain having a length $1\text{-}\lambda$. This model is shown in Figure 2. The current generator $G_T V_a$ represents the gain in the device and results from modulation of the channel width by the gate-to-channel voltage. The resistances R_1 and R_2 represent the series resistance of the channel; C_1, C_2, and C_3 represent the capacitance of the gate depletion region; and G_1, G_2, and G_3 represent the leakage conductance of the gate.

A pi-model for the field-effect transistor, shown in Figure 3, can be derived from the model of Figure 2. At low frequencies the model reduces to that often stated for the field-effect transistor[1]. At all but very low frequencies, the leakage conductances are negligible in comparison to the gate susceptance.

At high frequencies the input conductance increases, while the transconductance decreases at the cutoff frequency ω_o. The output also increases due to the extrinsic drain resistance r_d. The cutoff frequency ω_o is given by

$$\omega_o \cong \frac{G_m}{C_{gd}}$$

The cutoff frequency also corresponds to the maximum frequency of oscillation of the device. Measurements on several transistors yielded λ values of *0.3* to *0.8* and cutoff frequencies from *5* to *350 Mc*.

Above the *l/f* noise region a simple noise model can be obtained by assigning thermal noise generators to the resistive elements of Figure 2 and shot-noise generators to the gate junction. This results in an input noise current $\overline{I_{n1}^2}$, an output noise current $\overline{I_{n2}^2}$, and their correlation $\overline{I_{n1}\ I_{n2}^*}$ given in Figure 4.

The noise factor, *F*, of the field-effect transistor for an arbitrary source conductance, G_s, can be written in the form

$$F = F_O + R_n \frac{(G_s - G_O)^2}{G_s}$$

where F_O is the optimum noise factor obtained, when G_s is equal to the optimum source conductance G_O. R_n is the equivalent noise resistance. In Figure 5 these noise parameters are written in terms of the noise model of Figure 4. Measurements indicate that this model is valid where *l/f* noise is not important.

For frequencies below *50 kc*, *l/f* noise may be important. This noise can be included in the model by adding excess noise components to the input and output noise currents. The *l/f* noise increases the equivalent noise resistance and the optimum source conductance at low frequencies.

* This work was supported by Nonr 225(24) through the Office of Naval Research.

[1] Dacey, G. C., and Ross, I. M., "Unipolar Field-Effect Transistor," *Proc. IRE*, vol. 41, p. 970-979; 1953.

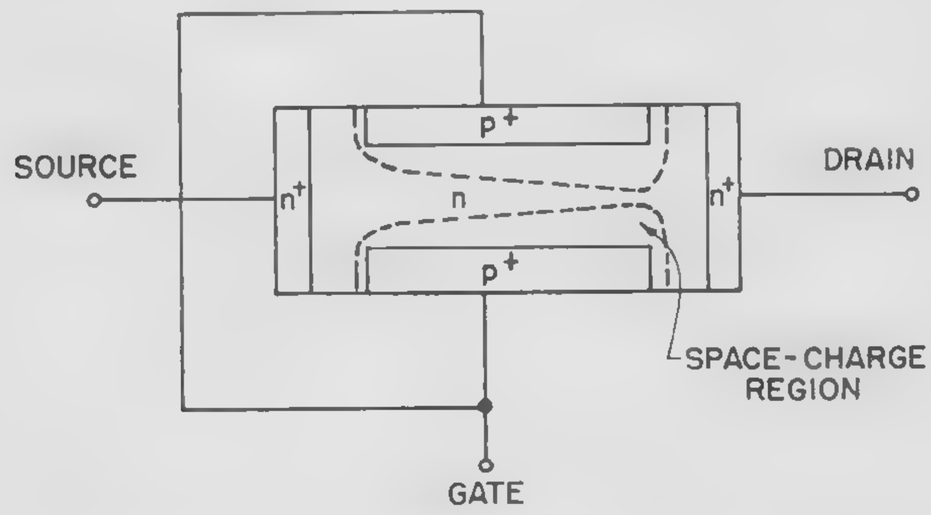


FIGURE 1—A field-effect transistor structure.

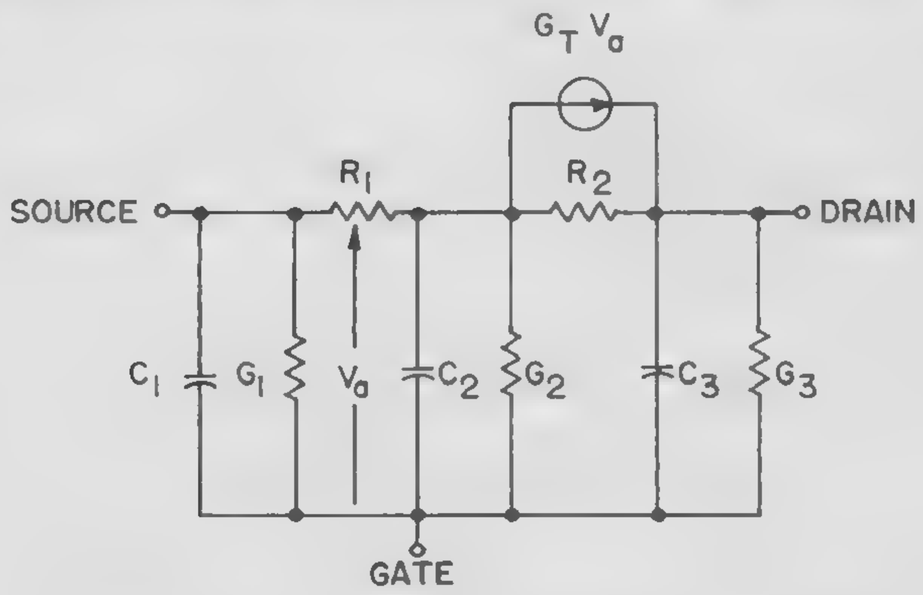


FIGURE 2—A two-section transmission line model for the field-effect transistor.

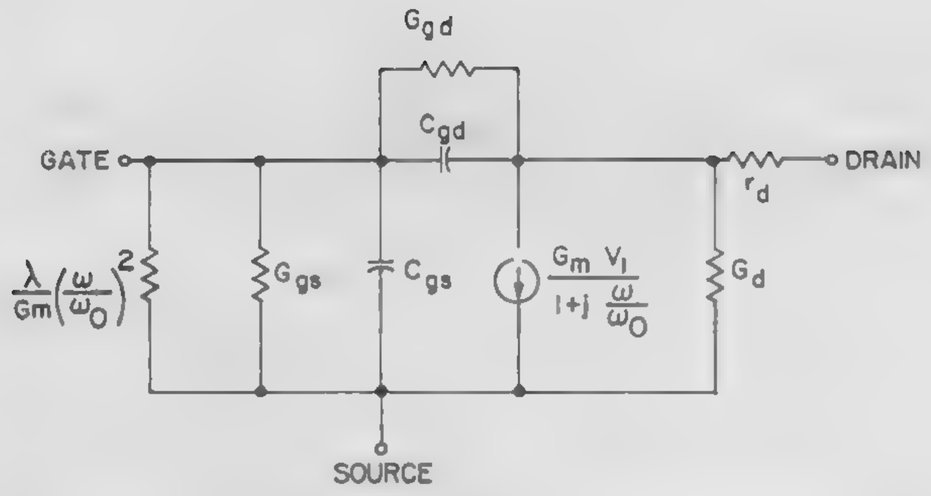
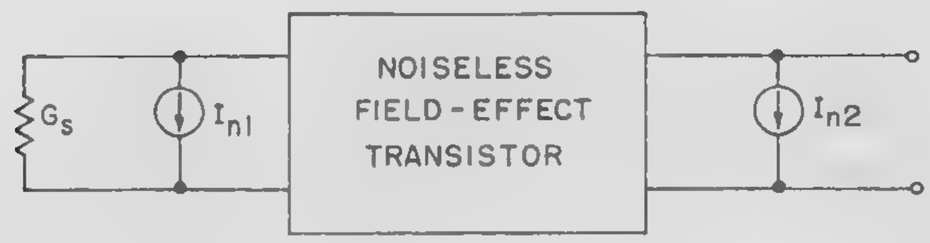


FIGURE 3—The pi model of the field-effect transistor.



$$\overline{I_{n1}^2} = 4kT\ Y_{11r}\,\Delta f + qI_g\Delta f$$

$$\overline{I_{n2}^2} = 4kT\left(Y_{22r} + \lambda Y_{21r}\right)\Delta f$$

$$\overline{I_{n1}I_{n2}^*} = 4kT\left(Y_{12}^* + Y_{21i}\right)\Delta f$$

FIGURE 4—The noise model of the field-effect transistor.

$$R_n \cong \frac{\lambda}{G_m}$$

$$G_o \cong \omega\left(C_{gs} + C_{gd}\right)$$

$$F_o \cong 1 + 2\,\frac{\lambda\omega}{G_m}\left(C_{gs} + C_{gd}\right)$$

FIGURE 5—Low-frequency noise parameters of the field-effect transistor.

SESSION X: Linear Circuits

FAM 10.4: Superconductive Resonant Circuits*

W. H. Hartwig

The University of Texas

Austin, Tex.

THE SURFACE IMPEDANCE of a superconductor is several orders of magnitude less than that of a normal conductor. The ratio of the real parts R_s/R_n is a function of frequency, the normal electron relaxation time, and reduced temperature; equation *(1)*, Figure 1. The ratio R_s/R_n is taken to be Q_n/Q_s of a superconductive resonant circuit, since neither frequency nor inductance changes appreciably when the circuit enters the superconductive mode. Lumped-parameter circuits (Figures 2, 3 and 4) are being studied to evaluate the concept of a tunable frequency standard and to examine the conduction processes in the *1-1000 Mc* frequency range.

In the *hf* and *vhf* range three dissipative mechanisms may dominate the residual resistance loss in the superconductor. The loaded Q_L can be represented as in equation *(2)*, Figure 1, where Q_o is the ultimate value limited by the residual resistance. Q_o is proportional to the three-halves power of reciprocal frequency, and has been measured in excess of 10^7 at *36 Mc*. $1/Q_D$ represents dielectric dissipation, Q_D being simply the cotangent of the loss angle; equation *(3)*, Figure 1. By reducing the volume of dielectric material this loss can be effectively minimized. $1/Q_R$ represents radiation loss which is eliminated by enclosing the circuit in a superconducting shield. The ultimate limitation is coupling loss $1/Q_c$ which can also alter the resonant frequency. Circuits incorporating capacitively-coupled input and output probes, as well as an equivalent circuit, where one inductive and one capacitive probe may be used are shown in Figure 5. With capacitive coupling, resonant frequency and Q depend upon the coupling. But with inductive and capacitive coupling, the resonant frequency can be made independent of coupling; Figure 5. The latter arrangement is very useful in design of a frequency-control device, since it permits a high and low impedance termination.

The loss due to loading, appearing as a temperature-independent asymptote in Figure 6, is subtracted to obtain the residual-resistance-limited curve for the constant frequency. Values for relaxation time calculated from Figure 6 are consistent with published values computed from *dc* conductivity.

The increase in surface resistance $\triangle R_s$ in a *dc* magnetic field, measured at *171* and *36 Mc*, was found to be proportional to H^2 (Figure 7), in agreement with theory[2]. Very good measurements of relative m^* for superconductors can be made, since effective mass is proportional to the inverse fourth root of the fractional change in surface resistance. The discontinuity in surface resistance occurs near the *dc* critical field for lead. The superconductors used are lead and lead-tin alloys, with the alloys having inferior properties. The failure of the circuit to enter completely the normal conducting mode above H_c is an anomalous behavior, presently attributed, in part, to the circuit geometry.

The feasibility of frequency-control devices, having a tuning range of over one octave, with Q's in excess of that attainable from commercial quartz crystals, has been established. In addition, basic properties of dielectrics and superconductors can be readily and accurately measured using these techniques.

* This work is being sponsored by USASRDL, Electronic Components Research Department, Contract No. DA-36-039 SC-87312.

[1] London, F., "Superfluids," vol. 1, *Dover Publications, Inc.*; 1961.

[2] Dresselhaus, G., and Dresselhaus, M., *Phys. Rev.* 118, p. 77; 1960.

[3] Hartwig, W. H., "Superconductive Frequency Control Devices," USASRDL Contr. No. DA-36-039 SC-87312, *Electronic Materials Res. Lab. Rpt. No. 119*, Univ. of Texas, Austin; Aug., 1962.

$$\frac{R_S}{R_n} = \sqrt{\frac{\omega\tau\phi(t)}{1+\omega^2\tau^2\phi^2(t)}\left[\sqrt{1+\omega^2\tau^2\phi^2(t)}-1\right]} = \frac{Q_n}{Q_S} \quad (1)$$

where: ω = rad./sec., τ = relaxation time,
$t = T/T_c$, $\phi(t) = t^4(1-t^4)^{-1}$,
R_S = supercond. surface res.,
R_n = normal surface res. @ T_c

$$1/Q_L = 1/Q_O + 1/Q_D + 1/Q_R + 1/Q_C \quad (2)$$

$$Q_D = \cot\delta = \epsilon'/\epsilon'' \quad (3)$$

where: ϵ', ϵ'' = real and imaginary parts of ϵ respectively

FIGURE 1—Ratio of surface resistance to normal resistance at the critical temperature versus frequency-relaxation time product derived from two-fluid model.

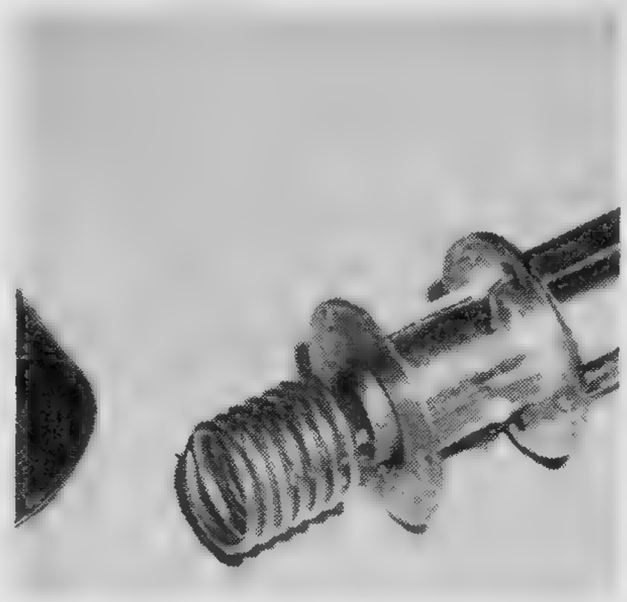


FIGURE 2—Superconductive resonant circuit with inductor and shield coaxial, *36 Mc* coated with *75%* Pb-*25%* Sn.

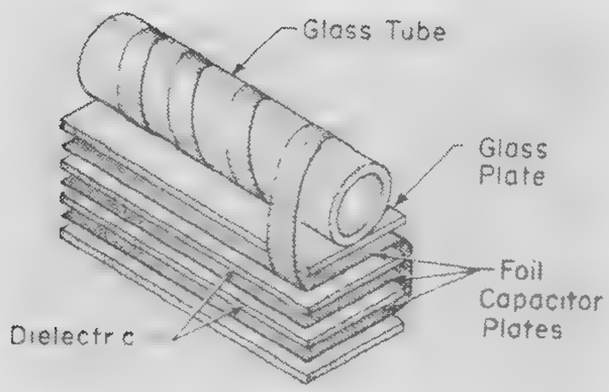


FIGURE 3—A *17.2-Mc* circuit using pure lead foil with glass coil form and dielectric. Dissipation in glass limited Q to less than *25,000*.

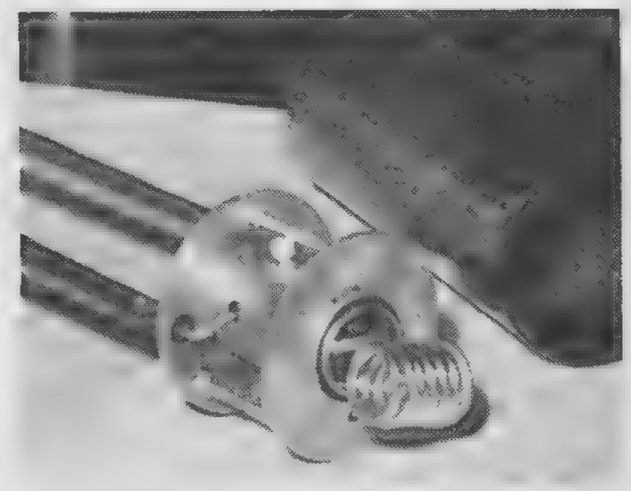


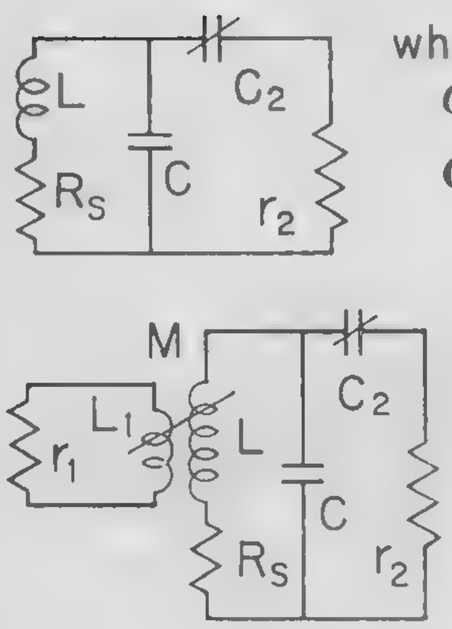
FIGURE 4—A *58-Mc* configuration with inductor axis normal to shield can axis. An unfavorable geometry since shield currents must cross joint in shield can top.

$$1/Q_C = (C_2/C)^2 r_2/\omega_0 L \quad (4)$$

where:

$$\omega_0 = 1/\sqrt{LC}$$

$$\omega \approx \omega_0/\sqrt{L(C+C_2)}$$



$\omega = \omega_0$ when

$$C_2/C = k^2 Q_1^2 \quad (5)$$

where:

$$k = M/\sqrt{L_1 L}$$

$$Q_1 = \omega_0 L_1/r_1$$

FIGURE 5—Equivalent circuits illustrating dependence of frequency and Q upon coupling. Resonant frequency can be made independent of coupling in lower circuit.

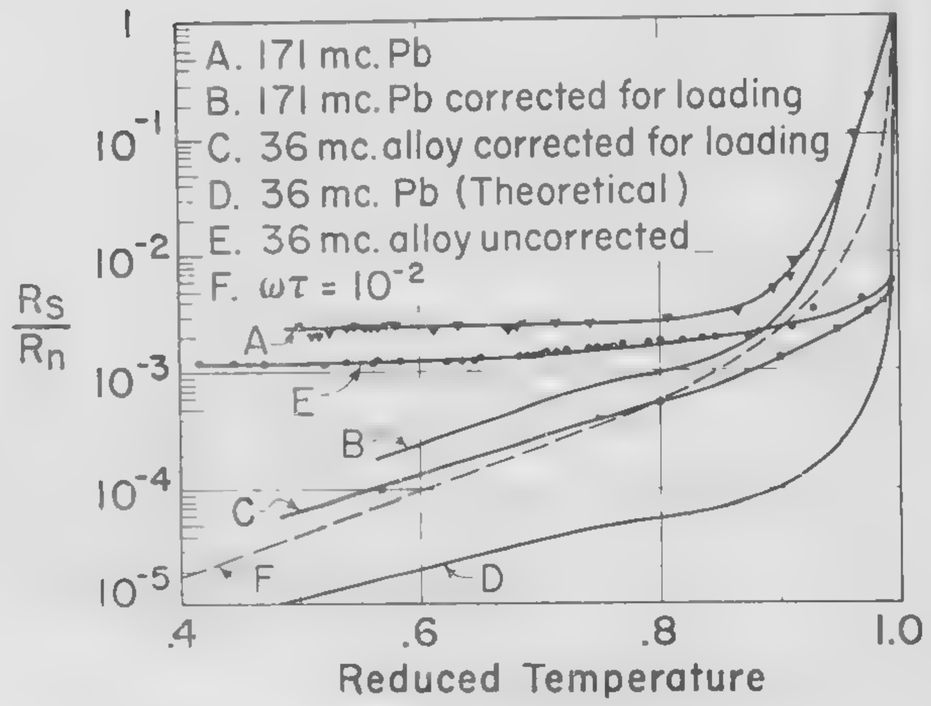


FIGURE 6—Residual resistance ratio as a function of reduced temperature showing measured values corrected for temperature-independent losses.

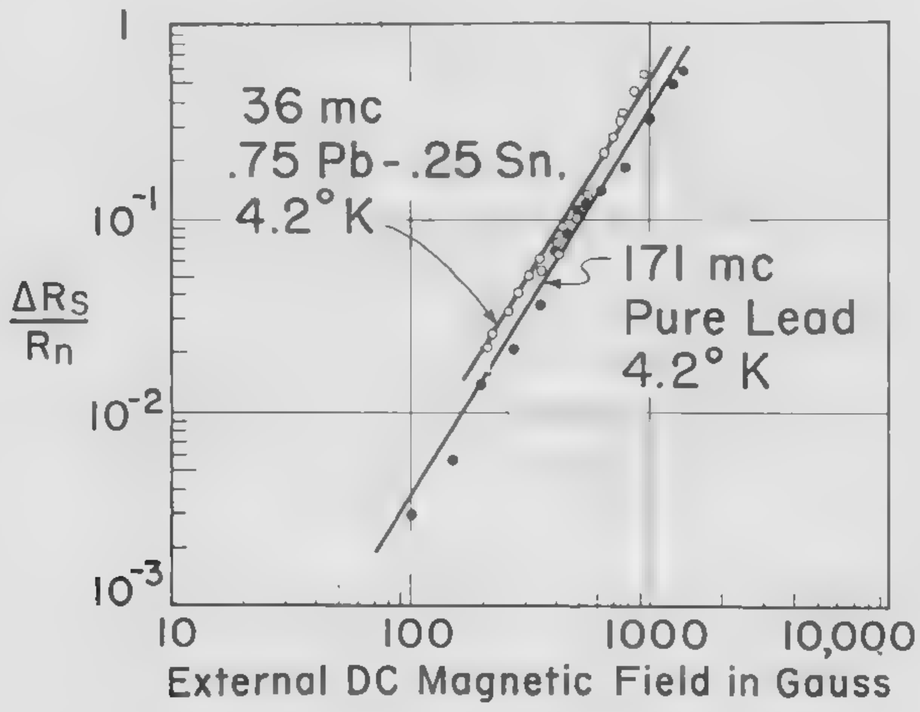


FIGURE 7—Increase in surface resistance due to external *dc* magnetic field.

SESSION X: Linear Circuits

FAM 10.5: A-2-w, 136-Mc FM Crystal-Controlled Transmitter

J. C. Boag, J. Saunders and J. M. Stewart

Research Laboratories, RCA Victor Co., Ltd.

Montreal, Canada

IN THE DESIGN of equipment for use in space applications, the important objectives are simplicity, reliable and stable operation over long periods of time and wide temperature ranges, rugged and radiation resistant construction, lightweight and high efficiency. For these reasons, and as warmup time normally cannot be tolerated, a solid-state unit is preferred.

The circuit of such a device appears in Figure 1. A crystal-controlled FM transmitter, it includes an oscillator operating at *17 Mc* followed by a single-stage buffer amplifier and alternate stages of varactor doublers and transistor amplifiers to obtain an output frequency of *136 Mc*. This approach has been found to offer a higher overall efficiency than where all of the power amplification is obtained at the crystal frequency. Additionally, the output power amplifier provides considerable isolation between the final varactor doubler and the load, thus reducing the sensitivity of the transmitter to variations in antenna impedance.

The oscillator (Figure 2) comprises a common-base transistor stage with the frequency of oscillation determined by a crystal operating in the series resonant mode in the collector to emitter feedback loop.

Frequency modulation is achieved by inserting a suitably-biased varactor diode D_1 and an inductor L_s in series with the crystal and applying the modulating voltage across the varactor. The function of L_s is to resonate the quiescent capacitance of the varactor to allow the crystal to operate at its natural series resonance, while that of L_p is to cancel partially the susceptance of the crystal passive capacitance and control modulation linearity.

Analysis shows that the angular oscillation frequency of the circuit is:

$$\omega = \omega_o \left[1 + \frac{L_p}{2L_m} \left(\frac{1 - \omega_o^2 L_s C_s}{(\omega_o^2 L_p C_s) - (1 - \omega_o^2 L_p C_p)(1 - \omega_o^2 L_s C_s)} \right) \right] \quad (1)$$

where ω_o, L_m and C_m are the crystal series resonant frequency, motional inductance and motional capacitance, respectively, and C_p is the crystal passive capacitance.

The relationship between the varactor capacitance C_s and the voltage across it, V, is assumed to be of the form:

$$C_s = \frac{1}{K(V + \phi)^\gamma}, \text{ where } \gamma \text{ is a constant exponent over}$$

a useful range of voltage.

It can be seen from equation *(1)* that for $\gamma \neq 1$, a nonlinear modulation characteristic is obtained. In practice, however, it is found possible to choose a value of L_p to provide a point of inflexion in the modulation characteristic at the bias point, $(V = V_o, C_s = C_{so})$, to yield very low modulation distortion; less than 3%. The optimum value for L_p is given by:

$$L_p = \frac{(1+\gamma) - (1-\gamma)\,\omega_o^2 L_s C_{so}}{\omega_o^2 \{C_s(1-\gamma) + C_p[(1-\gamma) - (1-\gamma)\,\omega_o^2 L_s C_{so}]\}} \quad (2)$$

Inserting the value found in equation *(2)* into *(1)*, the oscillation frequency in equation *(3)* is obtained:

$$\omega = \omega_o \left[1 + \frac{C_m}{4\gamma C_{so}} \cdot \left(1 + \gamma - (1-\gamma)\,\omega_o^2 L_s C_{so} \right) \left(1 - \omega_o^2 L_s C_{so} \right) \right] \quad (3)$$

By differentiation, the modulation sensitivity at the bias point is found to be:

$$\left(\frac{d\omega}{dV} \right)_{V = V_o} = \frac{\omega_o C_m}{8 V_o C_{so}} \left[1 + \gamma - (1-\gamma)\,\omega_o^2 L_s C_{so} \right]^2 \quad (4)$$

Figures 3 and 4 show plots of the oscillator frequency and modulation sensitivity as functions of the dimensionless parameter $\omega_o^2 L_s C_{so}$ and the varactor exponent γ.

After the buffer stage (which operates class-*A*, common-base) a choice exists as to whether varactor doublers, triplers or quadruplers should be used. As the same minimum number of presently available transistors are required to provide the necessary output power independent of the design chosen, the method shown in Figure 1 allows the use of economical, low-power, low cutoff frequency varactors in all doubler stages.

One typical doubler stage is outlined in Figure 6. The doublers are placed between common-base transistor stages. The varactor diodes are current driven in parallel resonance at the fundamental frequency with the second harmonic series resonated to provide drive for the following class-C transistor stage. This type of varactor circuit configuration is, in effect, an impedance transformer providing a match between the high-output impedance of one stage and the low-input impedance of the following stage. Parallel resonant traps are connected in series with the output of each doubler providing a rejection of the fundamental of the order of *30 db*.

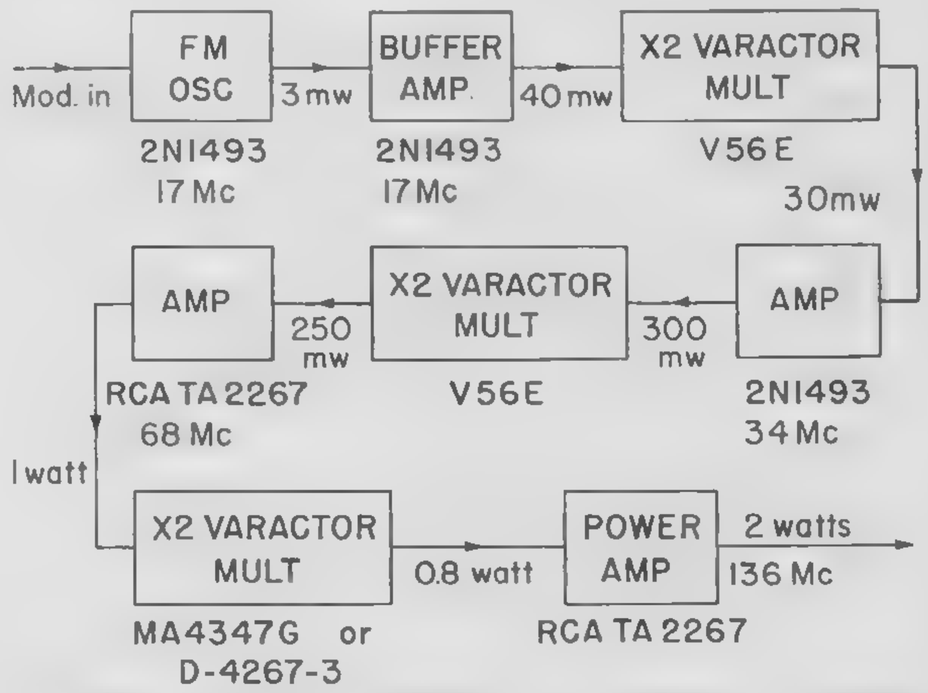


***FIGURE 1*—Block schematic of transmitter showing alternating arrangement of transistor amplifiers and varactor doublers.**

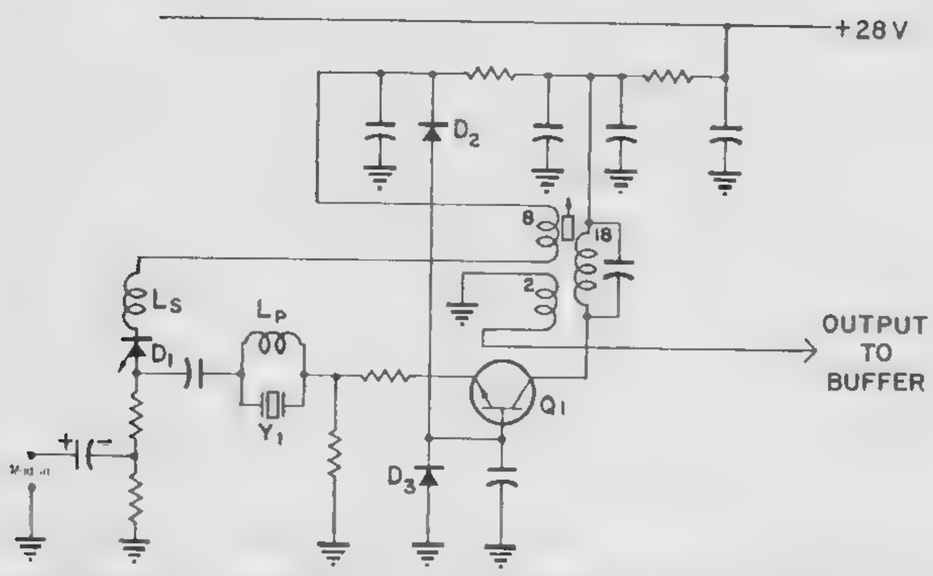


FIGURE 2—Schematic of oscillator showing varactor diode frequency modulator: D_1 = *V7E*; D_2 *and* D_3 = 1N755; Q_1 = 2N1493. Choice of *17 Mc* as oscillator frequency allows operation of crystals in their fundamental mode.

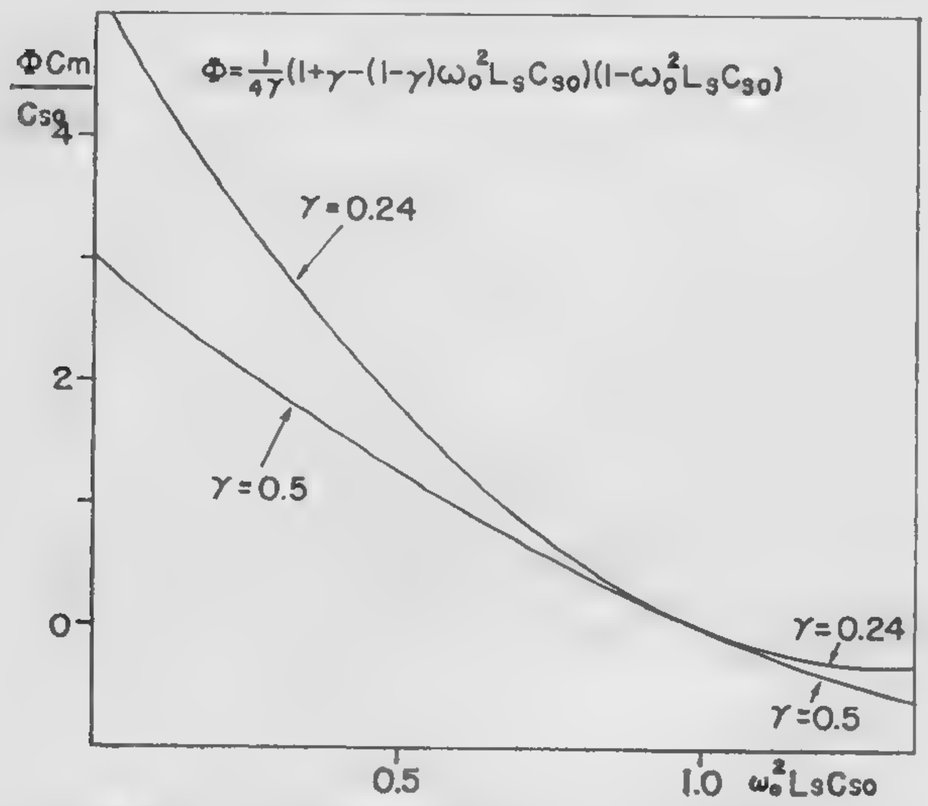


FIGURE 3—Fractional oscillator frequency as a function of the varactor exponent γ normalized to ω_o.

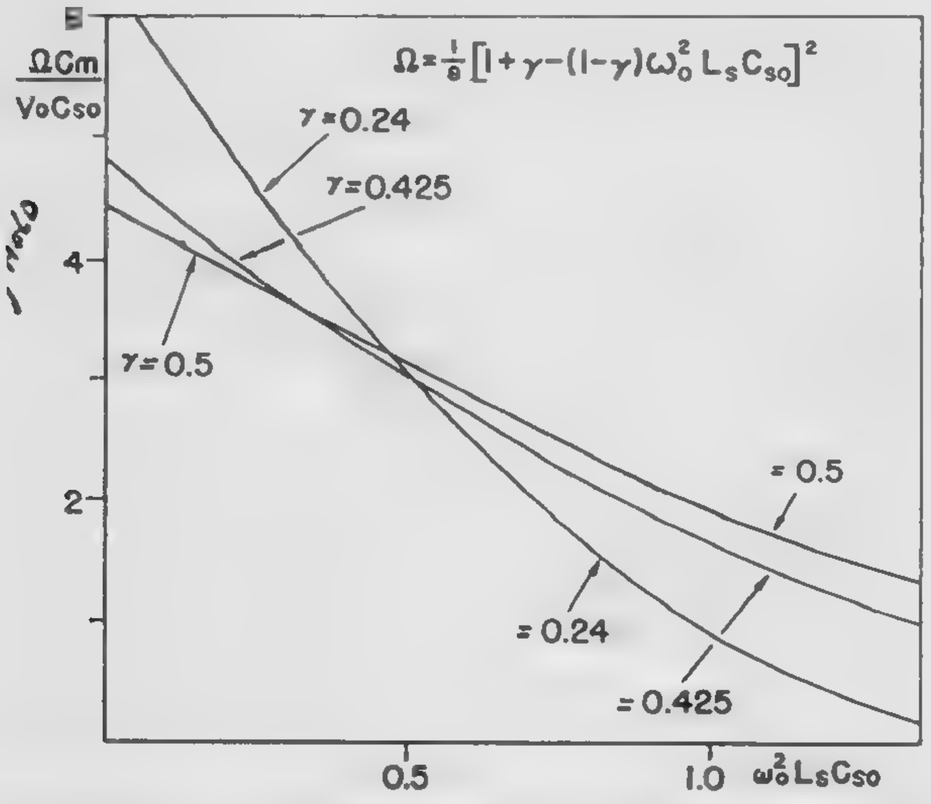


FIGURE 4—Fractional frequency modulation sensitivity as a function of the varactor exponent γ normalized to ω_o.

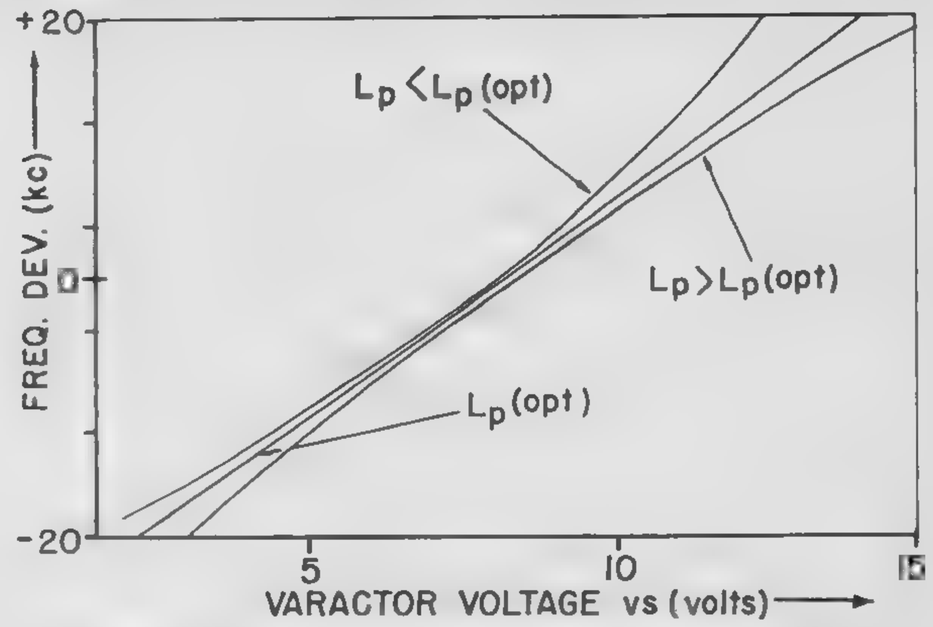


FIGURE 5—Dependence of modulation linearity on L_p with modulation sensitivity approximately *2 kc/v* at oscillator frequency of *17 Mc*.

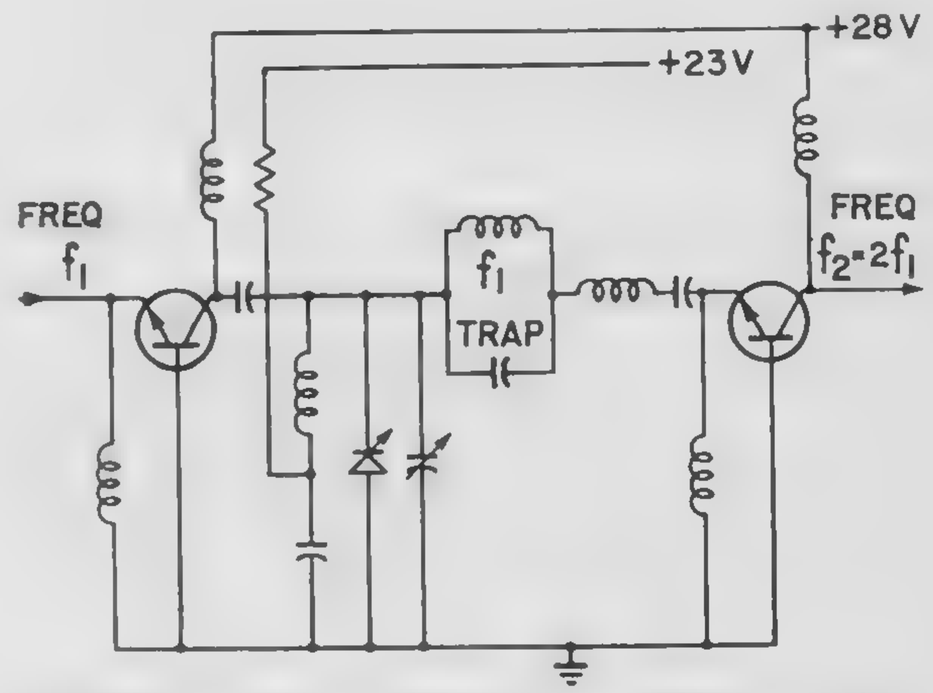


FIGURE 6—Basic schematic of varactor doubler coupling two common-base amplifier stages. Varactors are biased externally, using a zener-diode regulated *dc* voltage for stable operation for wide temperature and supply voltage ranges.

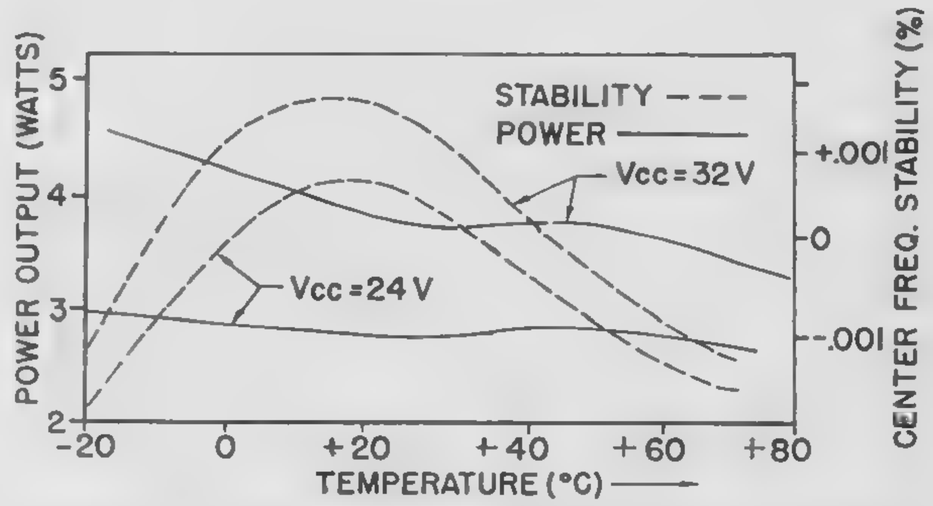


FIGURE 7—Transmitter power output and frequency stability as a function of temperature and supply voltage, showing capability of *2-w* power output with overall efficiency greater than *30%*.

SESSION XI: Integrated Circuits

Chairman: J. G. Linvill

Stanford University, Stanford, Calif.

FPM 11.1: Parasitic Effects in Integrated Circuits*

H. Dicken

Motorola Semiconductor Products, Inc.

Phoenix, Ariz.

IN FULLY-INTEGRATED CIRCUITS, as shown in Figure 1, where both the active and passive circuit elements are diffused into a single crystal of silicon, several detrimental parasitic effects are inherent in the structure. Substrate transistor action associated with circuit elements, such as diffused resistors and diodes, will completely change the circuit performance unless eliminated by proper design.

The construction of an integrated circuit involves many complex and interacting steps. Starting with a *n-type* epitaxial layer on a *p-type* substrate, the fabrication steps include: three basic photo-masking and diffusion processes, an interconnection masking and a metallization. The result of these steps is a four-layer structure; Figure 2. Each *p-n* junction of this structure has associated with it a capacitance which is a function of the layer with the lower impurity concentration. As a result, the designer must consider the following capacitances (per square mil of junction at zero volts bias) which are inherent in the diffused structure: $C_1 = 0.02$ pf, $C_2 = 0.1$ pf, $C_3 = 1.1$ pf, and $C_4 = 0.01$ pf. C_4 is not affected by bias.

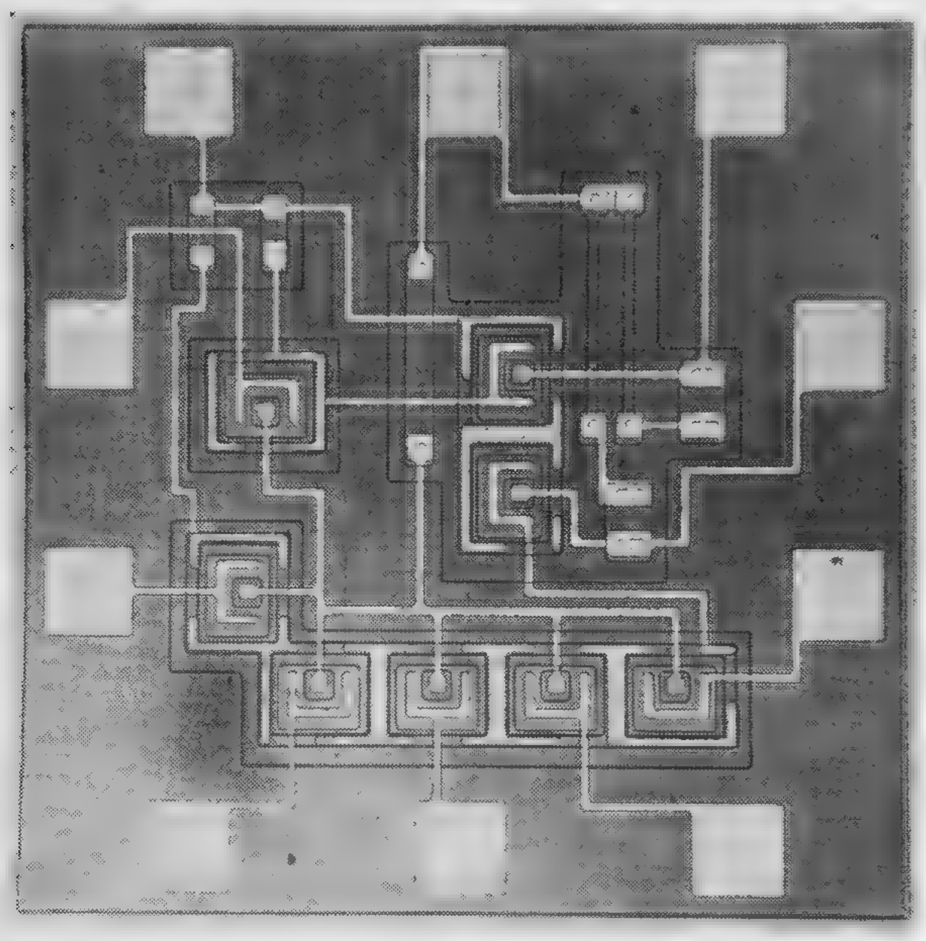
One circuit element which illustrates most of these parasitic effects is the resistor, which in integrated circuits is formed by a diffusion process. The *n-type* silicon layer is used for isolation, while the *p-type* layer, approximately three microns deep, determines the resistance value; Figure 3. This method of fabrication produces both a distributed capacitance and a distributed transistor effect; Figure 4. The values of these capacitances are as noted for C_1 and C_2. Their parasitic effects become significant only at high frequencies, above *10 Mc.*

The distributed *pnp* transistor with a beta range of *0.5* to *5* is a result of the relatively narrow (approximately 15 microns) *n-type* epitaxial layer between the *p-type* substrate and the *p-type* resistor diffusion. Conduction will occur whenever the *p-n* junction of the resistor and the epitaxial layer is forward biased and the *p-type* substrate is at a lower potential. In a properly-designed circuit, the *n-type* layer should be kept at the highest circuit potential. The trace of a typical unit of this type is shown in Figure 5.

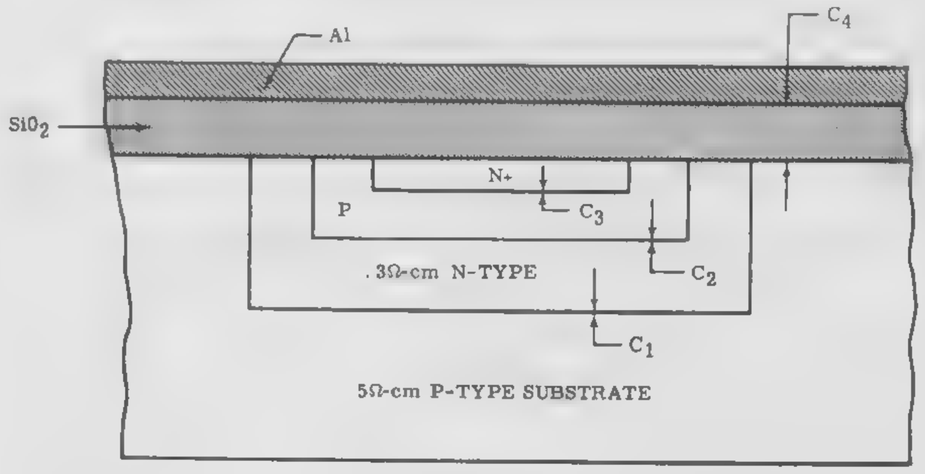
The substrate *pnp* transistor action as described can completely change the circuit performance. A typical example of this problem, which could be eliminated by proper design, is an integrated *NAND* gate where the base bias resistor and the *p-type* substrate are connected to a negative supply voltage.

Referring back to Figure 4, one may note that when one end of the *p-type* resistor is at a negative potential while the other end is at a positive base potential, the bias conditions are such that the distributed pnp transistor will conduct, thus shorting the resistor to the substrate. This effect is shown in the switching characteristics in Figure 6. The correct switching characteristics (Figure 7) are obtained when the *n-type* layer is biased to the highest circuit potential. It is possible to simulate and predict these effects from a standard component circuit; Figures 6 and 7. A test circuit, consisting of low beta *pnp* transistors (Figure 8) is connected to the standard circuit to produce exactly the same parasitic effects as would occur in a fully integrated circuit. By this method, the designer is able to check for such effects even before a photo-mask is drawn.

* Much of this work was done under Air Force Contract #AF33(616)8276 on "Compatible Techniques for Integrated Circuits."



(Left)
FIGURE 1—A completed fully integrated logic circuit.



(Above)
FIGURE 2—Capacitance associated with each junction of a typical integrated circuit.

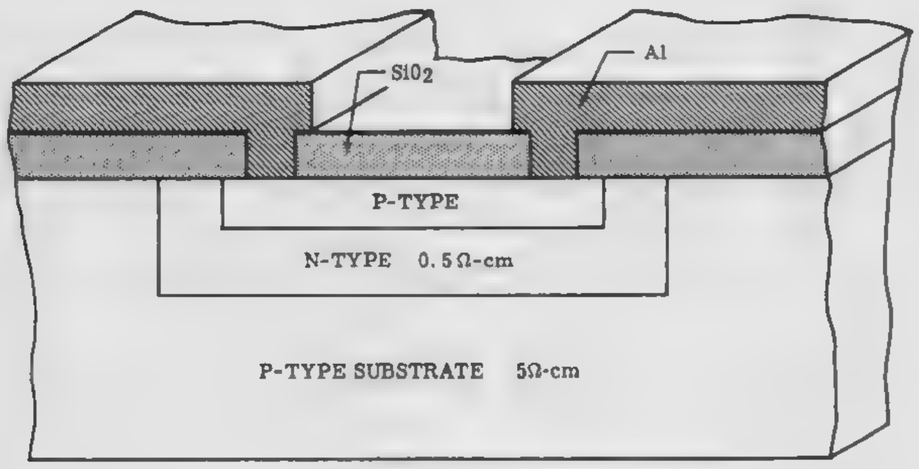


FIGURE 3—A cross-sectional view of a diffused resistor.

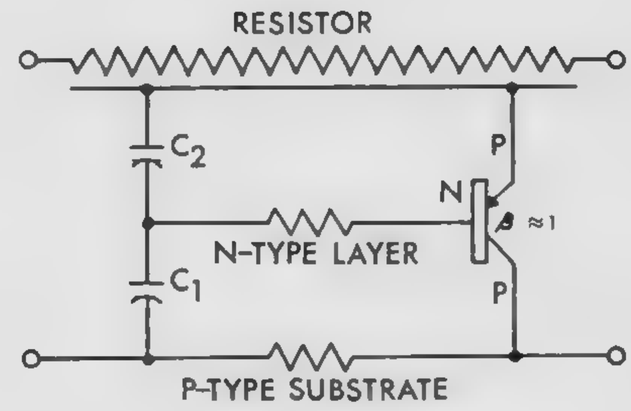


FIGURE 4—Equivalent circuit of a diffused resistor.

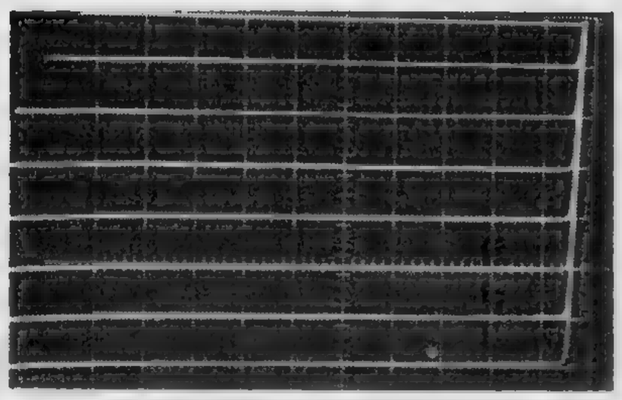


FIGURE 5—Characteristic curves of a substrate *pnp* transistor: *1 ma/div* vert; *1 v/div* horiz; *0.2 ma*/step.

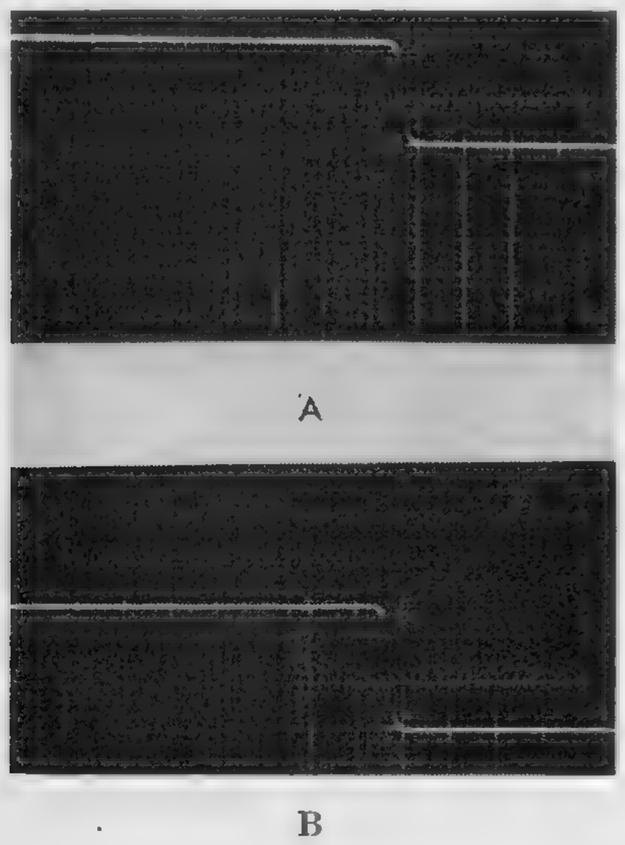


FIGURE 6—Switching characteristics of a *NAND* gate with parasitics: (A) standard component circuit; (B) integrated circuit . . . 0.5 *v/div* horiz input and 0.5 *v/div* vert output.

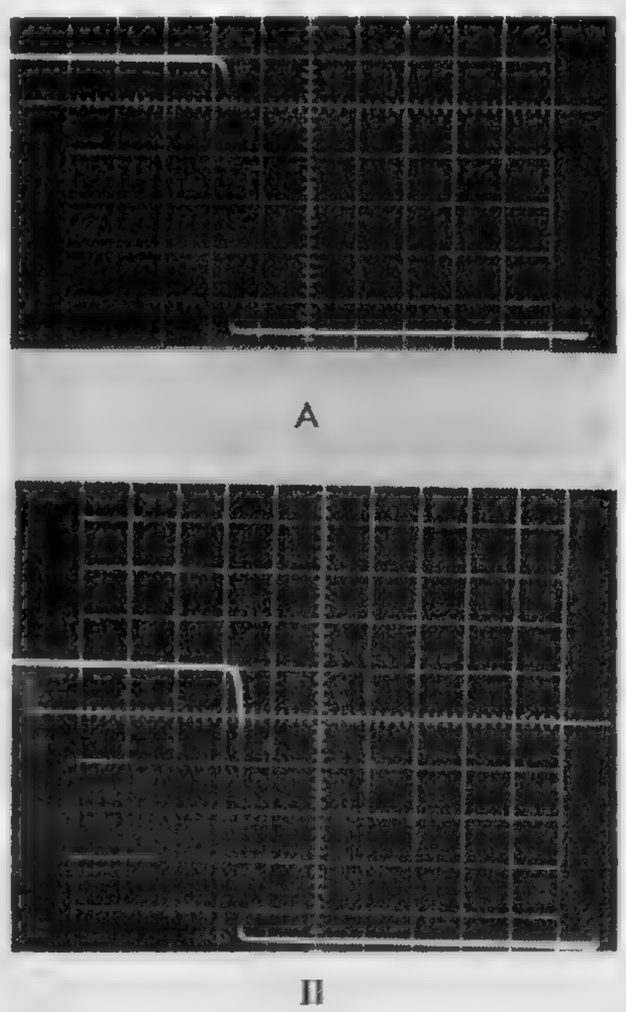


FIGURE 7—Switching characteristics of a NAND gate: (A) standard component circuit with corrected parasitics; (B) standard component circuit without parasitics . . . *0.5 v/div* horiz input and 0.5 *v/div* vert output.

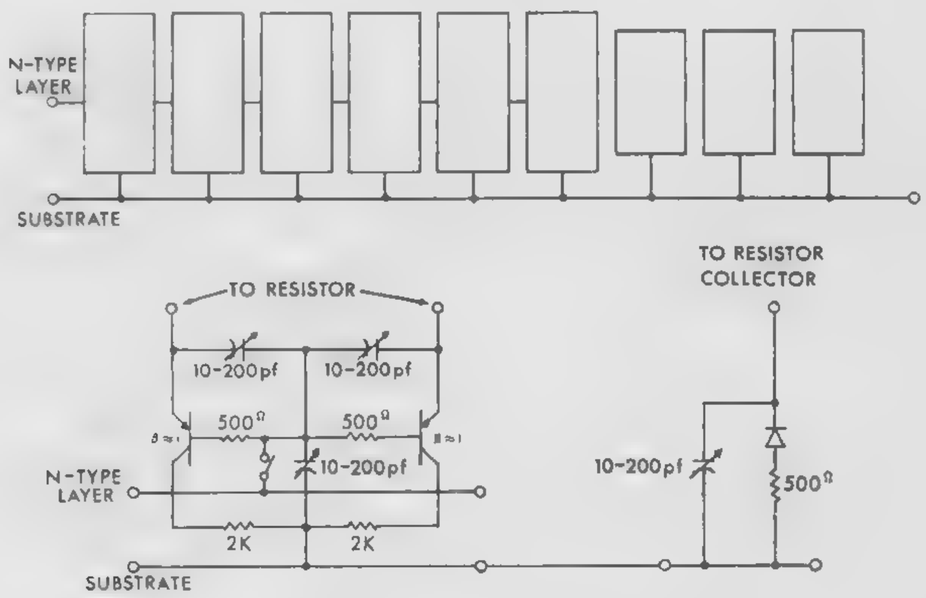


FIGURE 8—Parasitic test circuit.

SESSION XI: Integrated Circuits

FPM 11.2: A Unipolar-Bipolar Transistor Configuration for Integrated Audio Amplifiers

H. C. Lin, M. J. Geisler and K. K. Yu

Molecular Electronics Div., Westinghouse Electric Corporation

Pittsburgh, Pa.

Conventional transistor audio amplifiers for phono applications require large capacitors for bypass and coupling and high resistances for biasing the input circuit when a high-impedance pickup is used. It is difficult to incorporate large values of resistance or capacitance in silicon integrated circuits. However, by using a unipolar and a bipolar transistor together, high input impedance can be achieved without the use of large resistors.

The use of a unipolar transistor in conjunction with a bipolar transistor has been proposed before. The basic circuit of such a *unibi* amplifier is shown in Figure 1. The drawback of this amplifier is that the base current of the bipolar transistor is equal to the constant channel current of the unipolar transistor. As is generally known, a constant base current bias suffers from temperature instability and poor interchangeability of transistors.

A new circuit, which eliminates these drawbacks, has been developed. The basic circuit is shown in Figure 2. Two unipolar transistors are connected in series as the input stage. Assume that the unipolar transistors have *p-type channels*. The upper unipolar transistor has a constant current characteristic as shown in Figure 3. The drain, d_1, of the upper unipolar transistor is connected to the source, s_2, of the lower transistor. If the two unipolar transistors have approximately the same pinch-off current (Figure 3) and the output current, i_o is small compared with the pinch-off current, s_2 will assume a potential nearly the same as the gate, g_2. If a signal is applied to g_2, s_2 will follow the signal voltage. The upper unipolar transistor, being a constant current device, will not load the signal to reduce the available output current, i_o, or to introduce distortion.

A practical amplifier circuit is shown in Figure 4. Source s_2 is connected to the base of the bipolar transistor, Q_1. Transistors Q_1, Q_2 and Q_3 are connected in cascade as emitter followers. The emitter voltage (both *dc* and *ac*) at Q_3 therefore follows the base voltage of Q_1. Due to cathode-follower action of the unipolar transistor, the base voltage of Q_1 in turn follows the input voltage at g_2. Thus the emitter of Q_5 follows closely the input voltage.

The overall transconductance of this amplifier is represented by the equation shown in Figure 5. For high sensitivity, R_E should be low and I_{E3}, gm, h_{fe}, large. For low distortion, R_E should be made much larger than $1/g_m\, h_{fe1}\, h_{fe2}\, h_{fe3}$ and $3\ kT/qI_{E3}$.

The temperature stability of such a circuit is good because the voltage at the base of the first bipolar transistor is fixed by the gate voltage. If this voltage is made much greater than base-to-emitter voltage, variations due to changing temperature or transistor substitution will not change the emitter voltage at Q_3 appreciably.

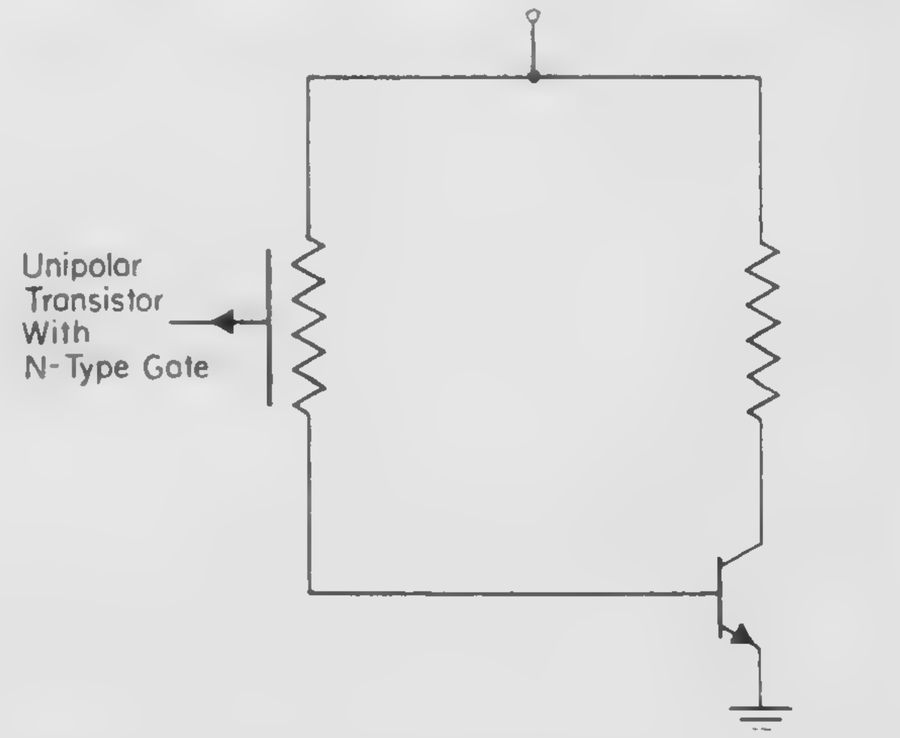
This circuit also has the advantage that the absolute transconductances of the unipolar transistors are not critical so long as the characteristics are well matched, a feature that lends itself to functional block fabrication.

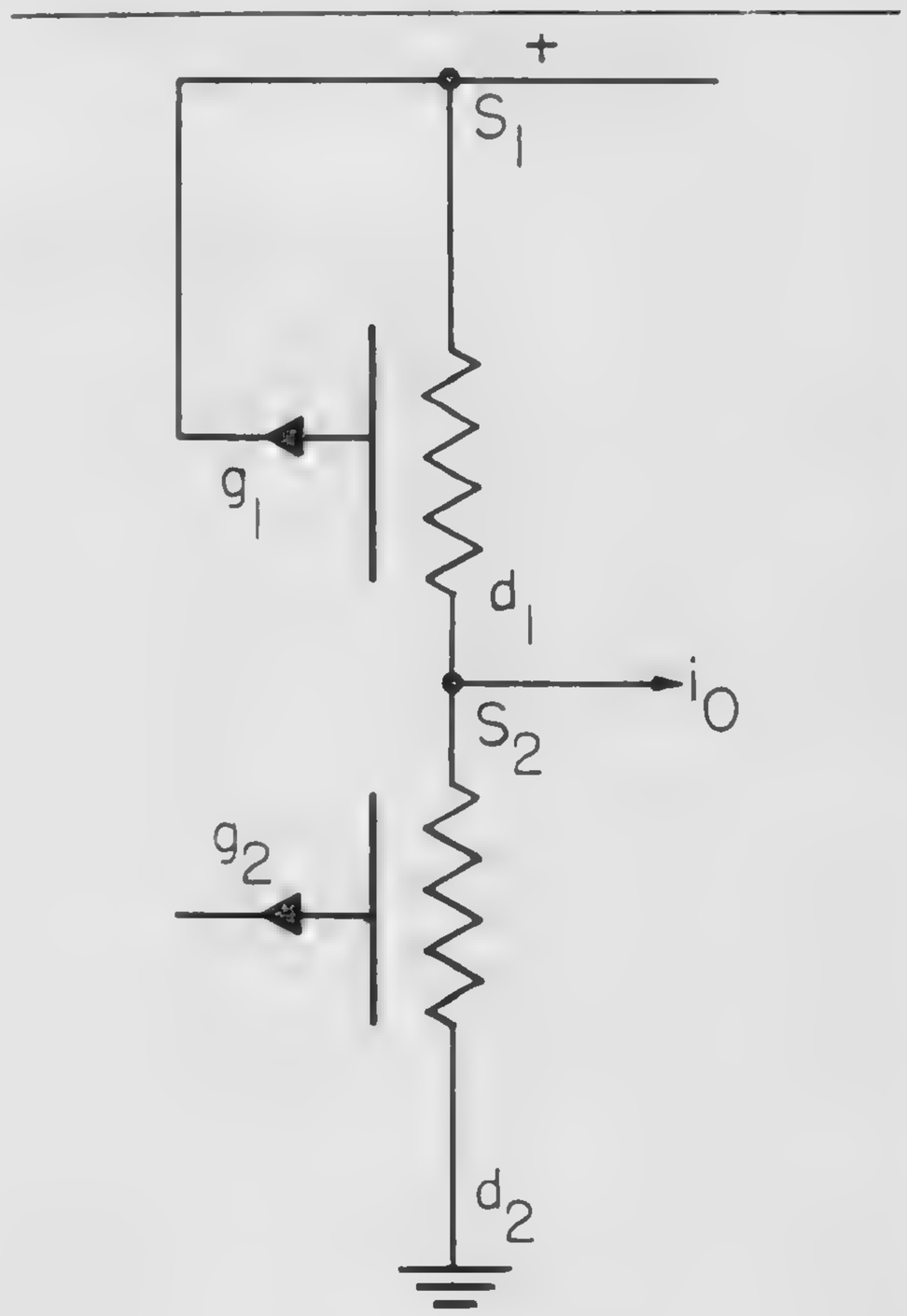
If unipolar transistors with *n-type* channels are used in conjunction with *npn* transistors, the circuit shown in Figure 4 may be modified to that shown in Figure 6.

This amplifier circuit has been fabricated in silicon integrated form.

The performance of a typical integrated amplifier is:

Max. sine-wave output, P_o	*3 w*
Sensitivity (at *3-w* output)	*0.5 v rms*
Harmonic distortion	*2.5%*
Frequency response ($\pm$ *1.5 db*)	*50-15000 cps*





(Right, top)
FIGURE 1—Unibi **amplifier.**

(Right)
FIGURE 2—**Unipolar transistor input stage.**

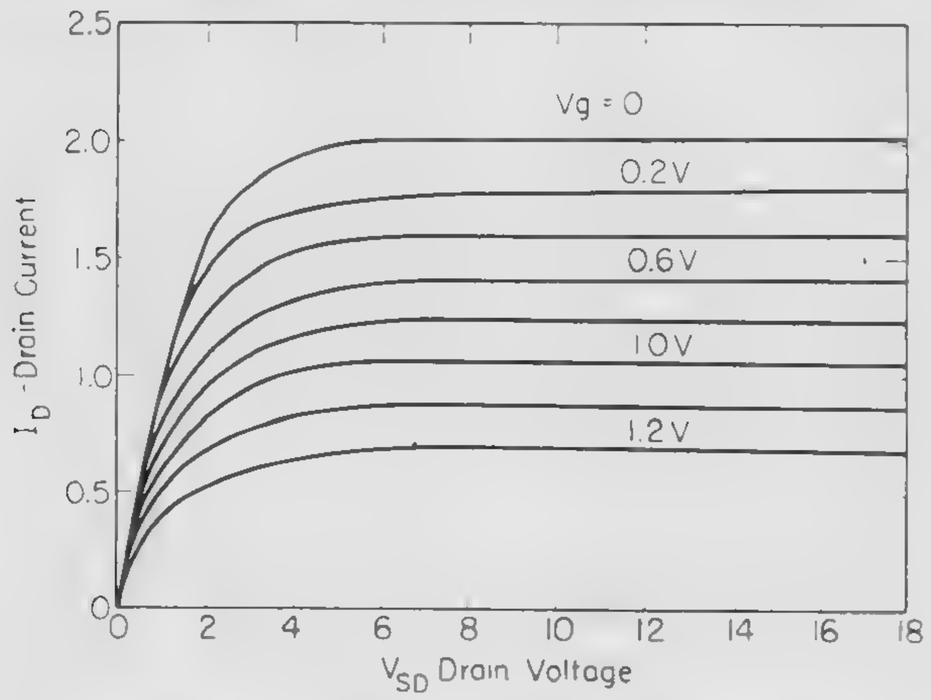


FIGURE 3—**Unipolar transistor characteristic.**

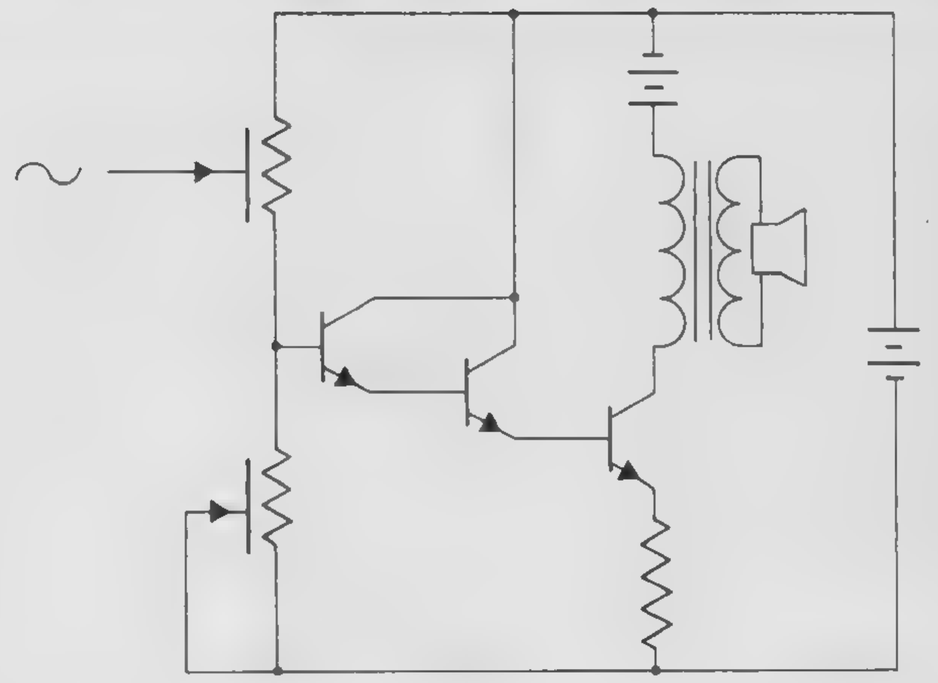


FIGURE 6—**Amplifier using unipolar transistors with *p*-type gates.**

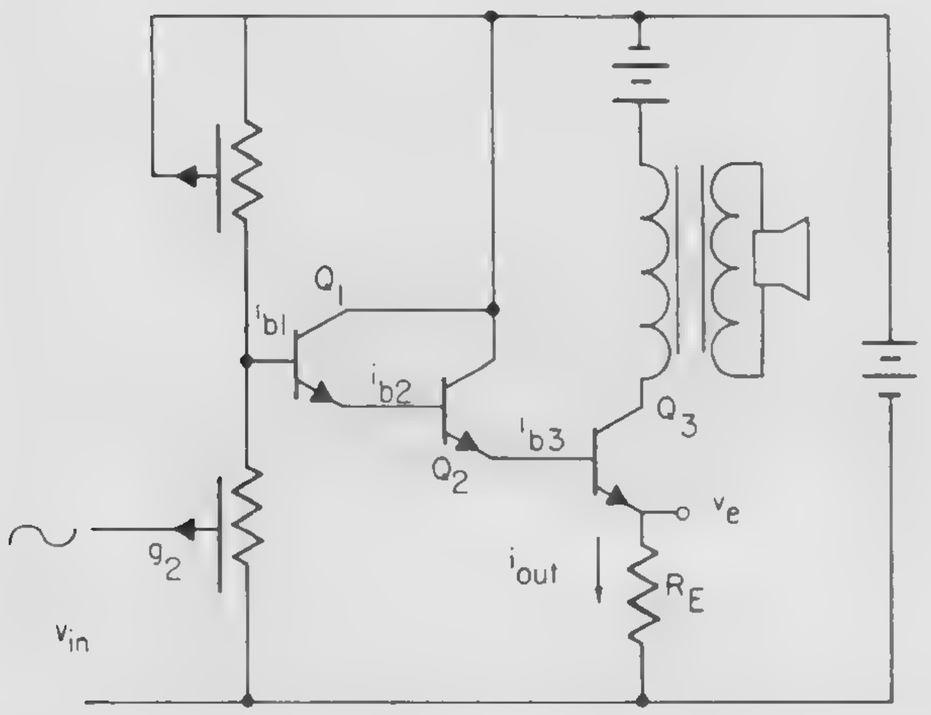


FIGURE 4—**Amplifier using unipolar transistors with *n*-type gates.**

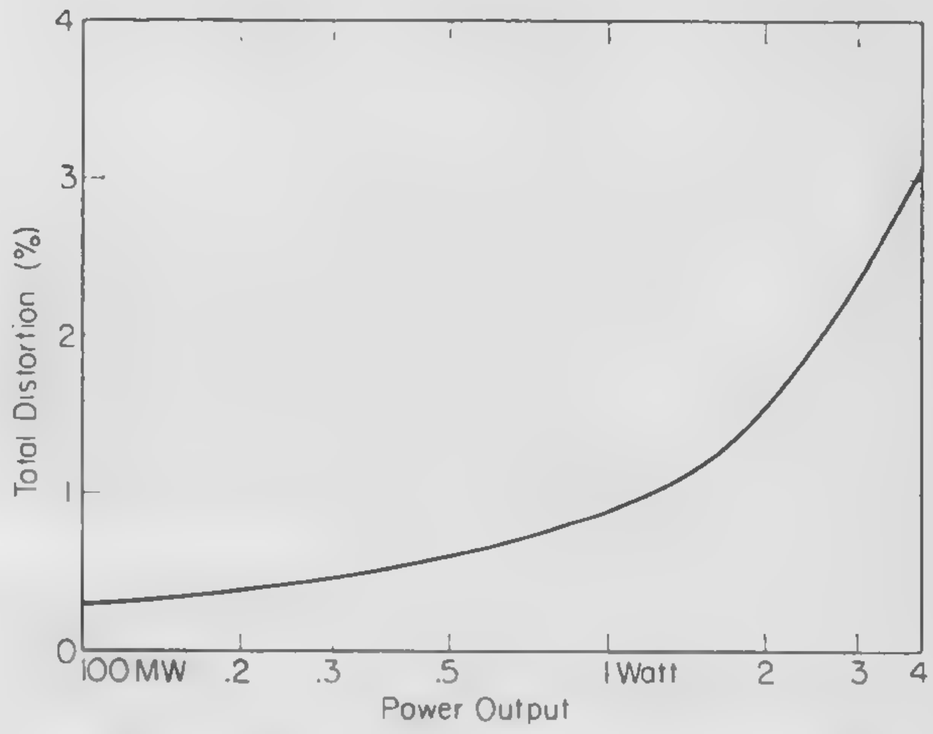


FIGURE 7—**Typical distortion versus power output curve.**

$$G_m = \frac{i_{out}}{v_{in}} = \frac{1}{R_E + 1/g_m\, h_{fe1} h_{fe2} h_{fe3} + 3KT/qI_{E3}}$$

Where g_m = transconductance of unipolar transistor

$h_{fe} \simeq$ common emitter current gain

I_{E3} = dc emitter current of Q_3

FIGURE 5—**Characteristic equation of the amplifier.**

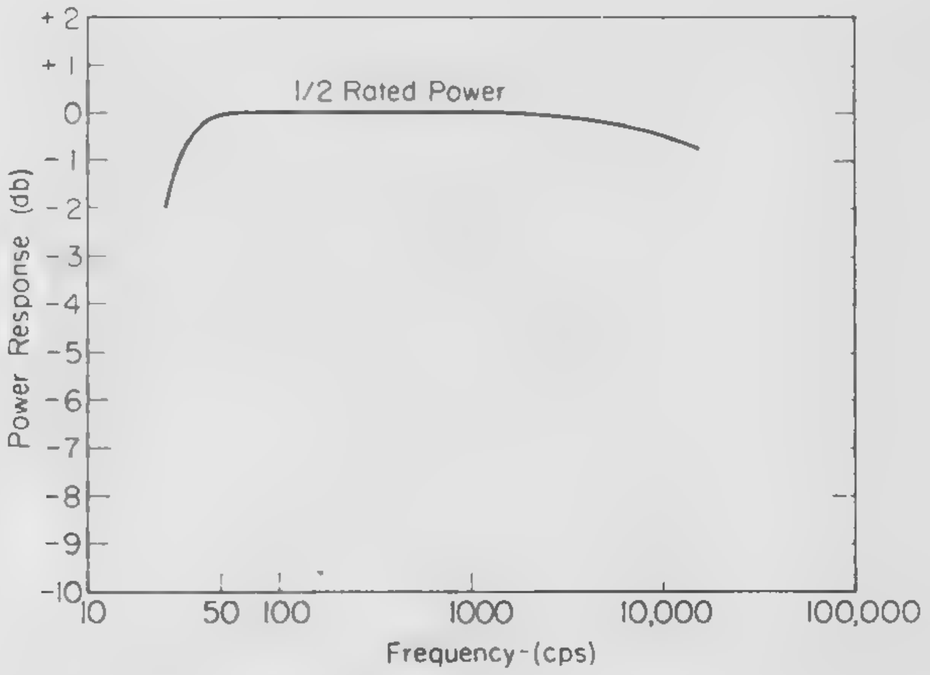


FIGURE 8—**Typical frequency response curve.**

SESSION XI: Integrated Circuits

FPM 11.3: Semiconductor Networks for Linear Amplification Using the Switching Mode

L. J. Housey

Texas Instruments, Inc.

Dallas, Tex.

THE RECENT NEED for audio power amplification through the use of integrated circuitry has forced aside the classical methods of class *A* and *B* operation. This has come about because of the small size and limited power capability of semiconductor networks. Replacing these methods is the technique of obtaining linear power amplification by using *pulse duration modulation; PDM.* This technique achieves linear amplification by operating transistors in the switching mode. The theoretical limit of efficiency approaches *100%*, and practical efficiencies exceeding *90%* can easily be achieved.

In one of its forms, the *PDM* signal is composed of a train of pulses whose leading edge occurs at some constant repetition rate, but whose trailing edge is varied by the modulating signal. The frequency spectrum of such a signal consists of the following components[1]: *(1)*—*dc* term, *(2)*—the frequency spectrum of the modulating signal, *(3)*—the fundamental of the pulse repetition frequency and all its harmonics, and *(4)*—an ensemble of all possible pairs formed by the sum and difference of the modulating spectrum and the harmonics of the pulse frequency. Thus it can be seen that the *dc* term and the modulating signal can easily be recovered by passing the *PDM* through a low-pass filter. Also, for convenience the *dc* may be blocked.

Figure 1*a* shows a simple form for amplifying and recovering an audio signal. Switch S_1 is driven by a *PDM* signal, and switch S_2 is driven by its complement. The low-pass filter removes the carrier and its harmonics, and if the duty cycle of the *PDM* signal is *50%* when it is unmodulated, then the *dc* term is zero. Thus, the only frequency components which dissipate power in the load are those of the modulating signal. If the switches are assumed to be ideal and the filter is assumed to be lossless, the efficiency approaches *100%* as a limit.

In reducing this ideal setup into practice, transistors would be used as switches; and associated transistor circuitry would be used to obtain the complementary *PDM* signals. A block diagram of this arrangement is shown in Figure 1*b*. The driver switch performs several important functions. It amplifies the input signal; it provides complementary signals to the power switches; and it provides important timing to insure that there is no overlap of the *ON* condition of the power switches.

The operation of the driver switch can be understood through study of Figures 2 and 3. Assuming that the input voltage is positive, Q_1, Q_3 and Q_4 are *ON*, while Q_2 and Q_5 are *OFF*. Power is being delivered to the load through the upper power switch. When the input voltage goes negative, Q_1 turns *OFF*. Its collector rises until Q_2 turns *ON*. The upper power switch is turned *OFF* rapidly through the diode D_2 and the transistor Q_2. Also on the negative-going input signal, Q_4 turns off; but its collector rises slowly, giving an increased time delay until the lower power switch is turned *ON*.

When the input signal swings positive, the inverse operation takes place. The lower power switch is quickly turned *OFF* through diode D_5 and transistor Q_4, while the upper power switch is delayed in turning *ON* by the slow rise of the collector voltage of Q_2. Thus both the power switches are never *ON* at the same time.

All of the components of the driver switch are made by diffusing them into a single bar of silicon. Figure 4 shows a simplified cross-section of the components. The bar is mounted in the standard network package which is *1/8"* x *1/4"* x *1/32"* in size.

The power switches are mounted in a separate package, either a standard network package or a transistor header. In a network package power outputs of *1* to *5 w* can be obtained. If higher power outputs are required, the power switch should be mounted in a package that can easily be *heat sinked*, such as a power transistor header. Under these conditions, power outputs of *30* to *40 w* are possible.

A typical arrangement for driving a servo motor is shown in Figure 5. The *dc* servo motor is driven in one direction when switches *A* and *B'* are closed and in the opposite direction when switches *A'* and *B* are closed. In this example, the motor becomes its own loss-pass filter. At the null condition the net current through the motor is zero. This condition could be obtained if both *PDM* input signals were *50%* duty cycle and *180°* out of phase; Figure 6. The duty cycle of each input is varied in a complementary manner to obtain rotation in either direction.

Usable too is an alternate scheme in which the *PDM* inputs at the null conditions are short pulses of the same polarity; Figure 6. One input is delayed with respect to the other by a space equal to one-half the pulse spacing. At null, both pulses are of the same width, and the net current through the motor is zero. To rotate the motor, the pulse width of one input is increased while the other pulse width is decreased to zero.

Acknowledgments

The author appreciates the help of the members of Autonetics Inertial Navigation Division for their contribution to the circuit development and servo-amplifier applications.

[1] Black, H. S., "Modulation Theory," *D. Van Nostrand Co.* Ch. 17, p. 263-281; 1953.

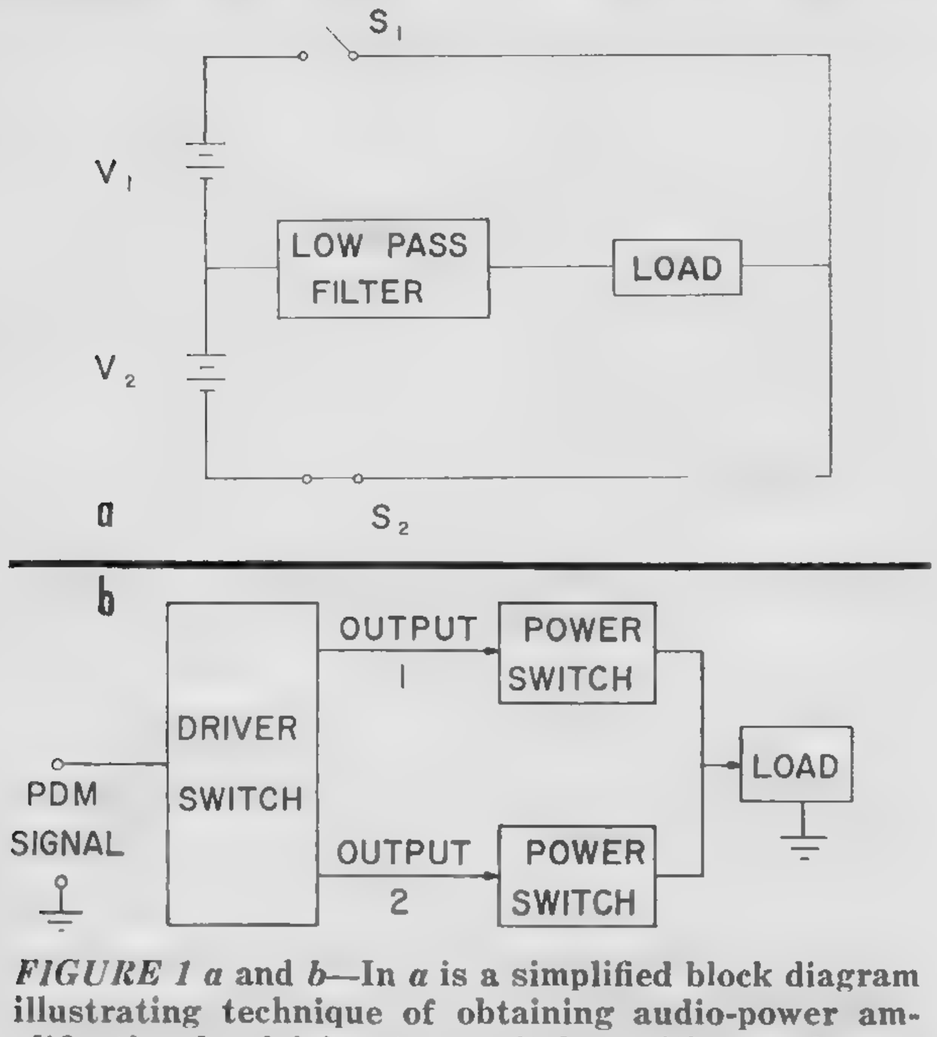


FIGURE 1 a and *b*—In *a* is a simplified block diagram illustrating technique of obtaining audio-power amplification by driving two switches with complementary *PDM* signals. A block diagram showing role of driver switch in providing input signals for the power switches is in *b*.

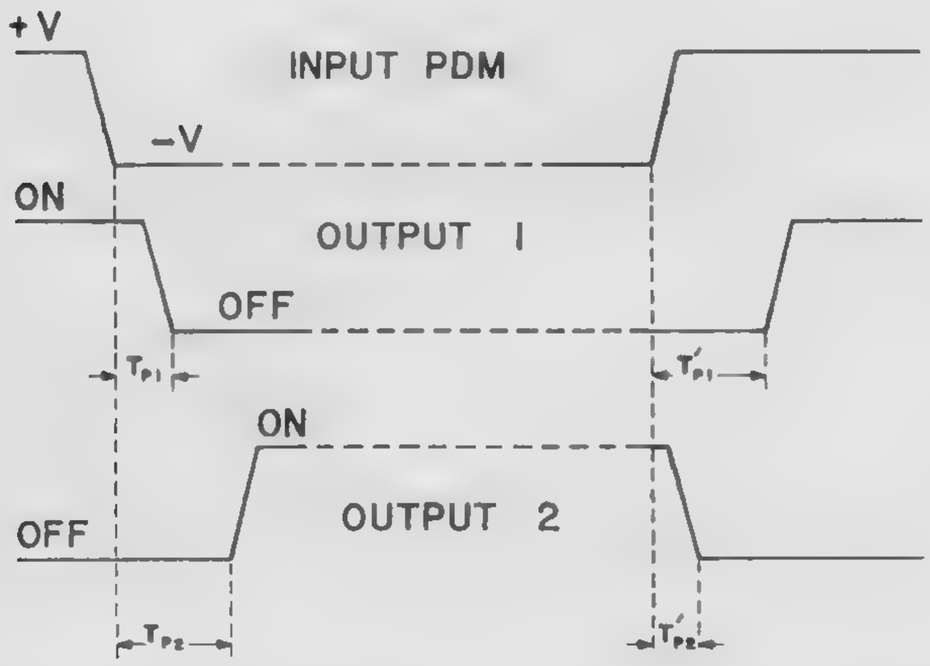


FIGURE 3—Timing waveform of the driver switch output: $T_{p1} < T_{p2}$ and $T'_{p2} < T'_{p1}$ thereby insuring that there is no overlap of the *ON* condition of the output switches.

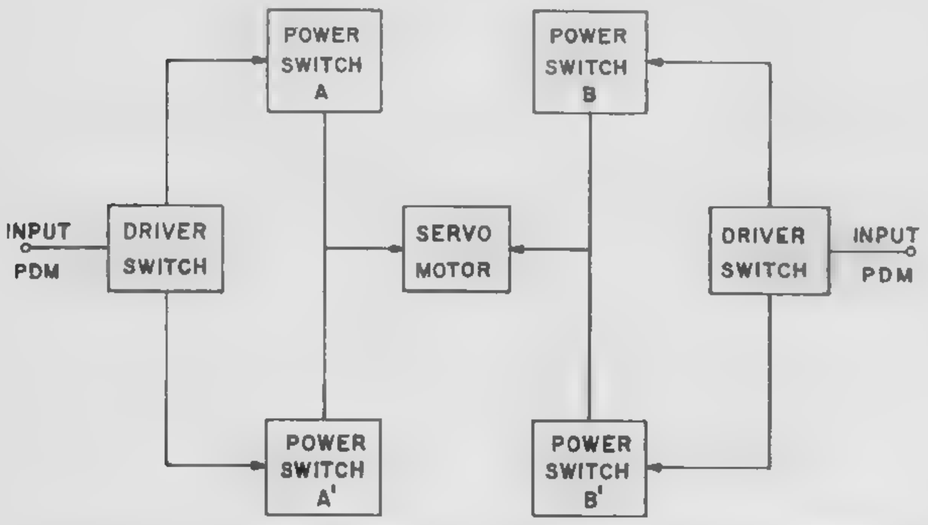


FIGURE 5—Block diagram of typical servo amplifier application showing two pairs of power switches for driving motor in either direction.

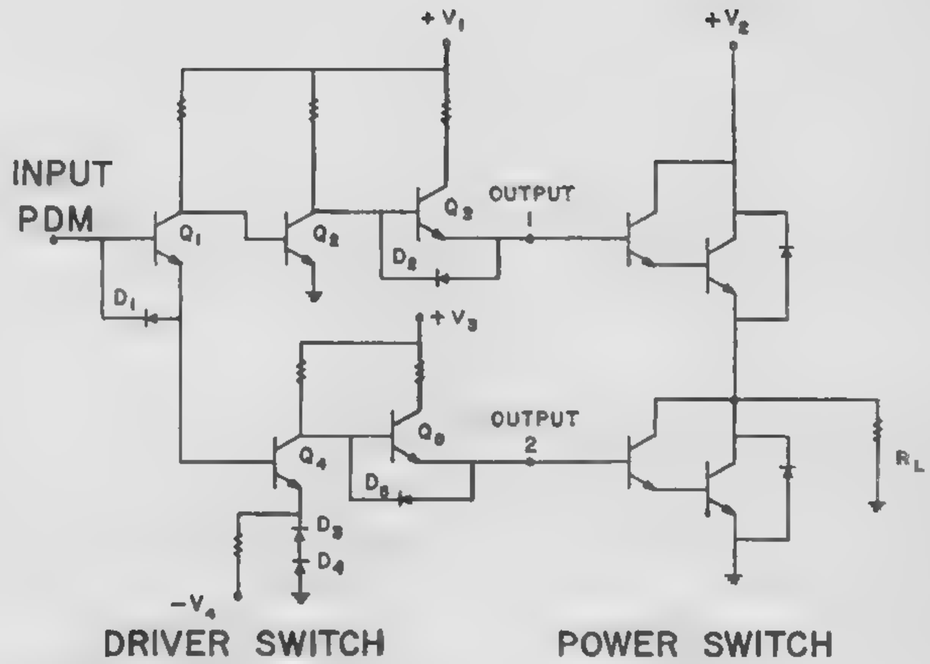


FIGURE 2—Circuit schematic of driver switch and power switches.

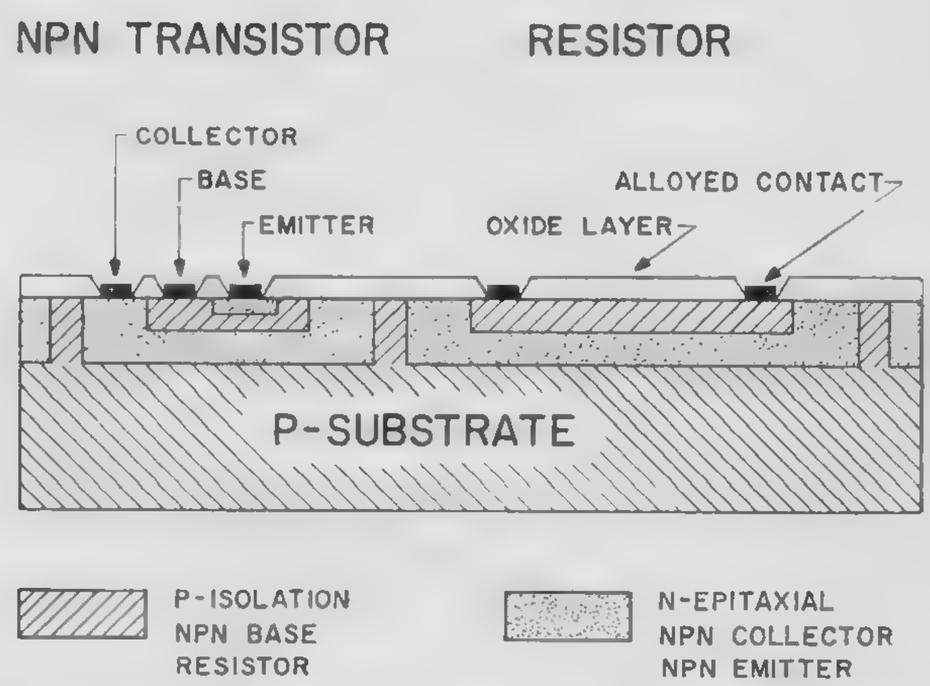


FIGURE 4—Cross-sectional view of the diffusions required to make the driver switch on a single bar of silicon. An isolation diffusion, a base diffusion, and an emitter diffusion are used.

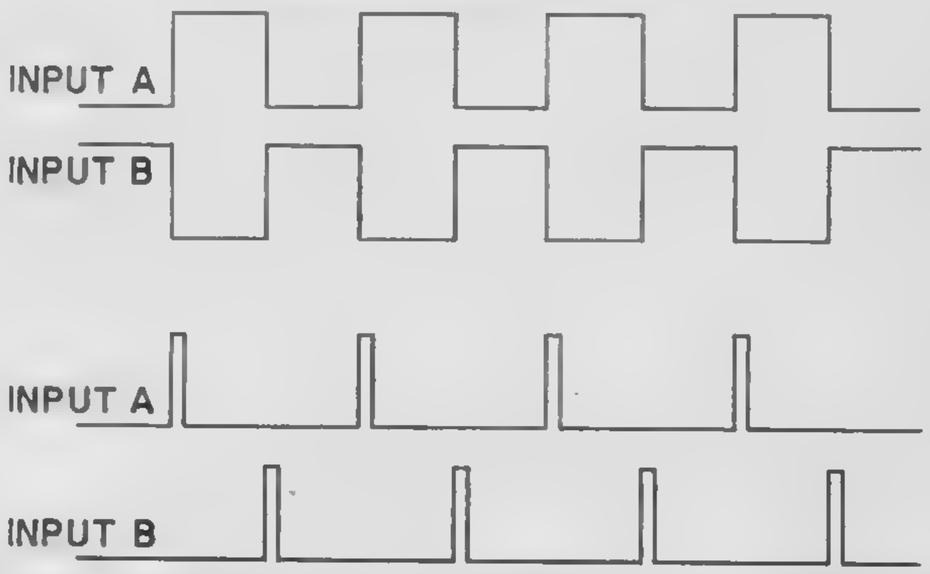


FIGURE 6—Waveforms of *PDM* signals at null condition for two different types of control.

SESSION XI: Integrated Circuits

FPM 11.4: Relative Merits of Current Mode Logic Microminiaturization

J. A. Narud, W. C. Seelbach and N. Miller

Motorola Semiconductor Products, Inc.

Phoenix, Ariz.

THE DESIGN of ordinary logic circuits usually involves a number of compromises between many conflicting requirements. For example, the demand for high speed is usually in conflict with the requirements that a circuit should have low power dissipation, high noise immunity, and large fan-out capability. In addition, trade-offs due to manufacturing considerations usually are made between circuit complexity on one hand and logic flexibility on the other.

The advent of microminiaturization imposes some additional requirements on the design of a logic circuit that is peculiar to the device technology involved. First, parasitic couplings between the various parts of the circuits are introduced through neighboring regions and through the substrate. These coupling effects can be both passive and active in nature. Also, because components cannot be selected in an integrated circuit, individual elements and component parameters will necessarily have much larger tolerances than their discrete counterparts. For example, it is difficult, at present, to fabricate integrated resistors with tolerances better than $\pm$ *20%*.

The basic logic gate having a fan-in capability of 5 (Figure 1) consists essentially of an *npn* current mode switch[1], with emitter followers coupling the signal from the collectors of the gate to the output. The emitter followers serve as *dc* translators so that the *dc* level at the outputs of the gate is compatible with the level requirements at the various inputs; additionally, since the emitter followers have a low output impedance, gates are provided with a large fan-out capability.

If a positive signal represents a logical *1*, the gate performs the logical operations *OR* and *NOR*, respectively; and with a negative signal used for a logical *1*, the logical operations *AND* and *NAND* are generated.

The fixed bias V_b for the gate is supplied by the regulator circuit; Figure 2. This regulator circuit also compensates for drift in *dc* output level due to variations in temperature and power-supply voltage. Tracking is thus obtained over the temperature range from $-55°C$ to $125°C$ and for $\pm 20\%$ variations of the power-supply voltage.

A novel and useful way of characterizing logic circuits is to specify the input, transfer and output characteristics of the logic circuits, in addition to the usual specifications used to characterize logic circuits. These characteristics, essentially nonlinear equivalents of the two-port *black box* parameters of linear networks, are especially useful *(1)*—in the design of the circuit itself, *(2)*—for its application to logical systems and *(3)*—for final test in the production of integrated circuits. It should be noted (Figure 3*a*) that the input resistance to the logic gates is high, in the order of *63,000* ohms for a logical *0* and a logical *1* input, and *2500* ohms in the transition region. The saturation region is of no interest since the gates do not saturate in normal operation.

Figure 3b shows the transfer characteristics for both the *OR* and the *NOR* outputs of the gate. It should be noted that the transition region is about *200-mv* wide, that the minimum logical swing is *800 mv*, and that the noise immunity of the circuit is *400 mv*.

Finally, we have in Figure 3c the output characteristics of the logic gates for a logical *0* and a logical *1* output condition. Together with the input characteristics, this characteristic is useful in estimating loading effects and *dc* fan-out capacility of the gates.

The logic circuits are inherently fast for a number of reasons. First, since most of the logical decisions are performed at the low impedance level of the common emitter load, and since the output impedance of the gates is low, deteriorating effects of parasitic and load capacitances are minimized. Secondly, the signal paths through the gate are essentially through emitter followers and common base stages which are inherently fast. Finally, due to feedback, the input capacitance of the gate is small; and since the circuits were intentionally designed to avoid saturation of the transistors, additional delay due to storage time effects are eliminated.

The transient response of the gate with a fan-out of *1* is shown in Figure 4. The output of the gate was loaded with a lumped capacitance of *20 pf* to take into account typical wiring capacitance. It will be seen that the propagation delay is about *3.5 nsec* and that the rise and fall times are *3* and *3.4 nsec*, respectively.

Also, in regard to noise and crosstalk, the logic block has several inherent advantages. First, inductive type crosstalk between adjacent signal lines is minimized, since only a small amount of current is transmitted from one circuit to the other due to the high input impedance of the gates. Secondly, cross talk due to mutual capacitances between inputs is sufficiently attenuated, because of the inherent low output impedance of the logic family. Finally, noise generated in grounds and power supply lines is practically non-existent since the current demand of the logic blocks is constant independent of which state a gate is in.

In Figure 5 we have the half-adder logic gate which, in addition to the regular sum and carry output, also provides a *NOR* output. It should be noted that multiple emitters are used on the transistor performing the sum function. The *AND* function can be performed in the collector by the use of multiple emitters, while the *OR* functions are performed at the common emitter node. The *OR* function can also be performed by connecting the output emitter followers together.

The basic flip-flop (Figure 6) performs the *SET* and *RESET* operation, but when combined with logic gates, the *J-K* and toggle operations can be readily obtained. The propagation delay of the half-adder is identical to that of the gate, and the maximum flip-flop delay is twice the delay of the logic gate.

[1] Yourke, H. S., "Millimicrosecond Transistor Current-Switching Circuits," *Transistor and Solid-State Circuits Conference;* February, 1957.

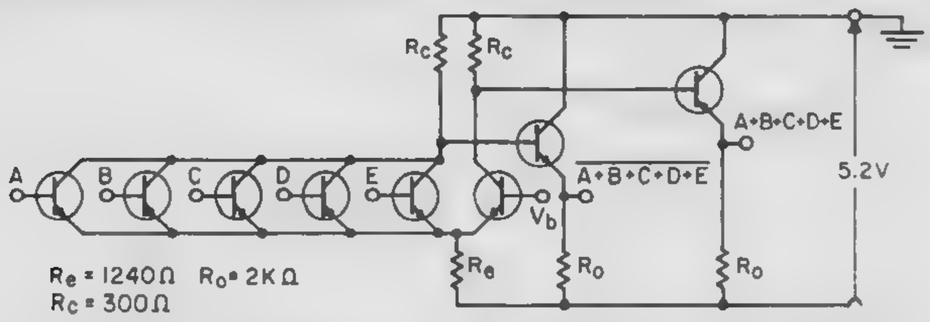


FIGURE 1—**Basic five input logic gate with emitter follower level transistors for level compatibility and low output drive impedance.**

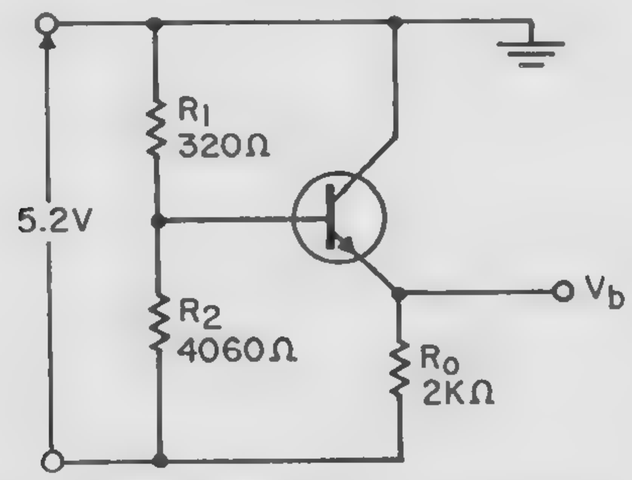


FIGURE 2—**Bias regulator circuit which provides temperature and power supply compensated reference voltage to logic gates.**

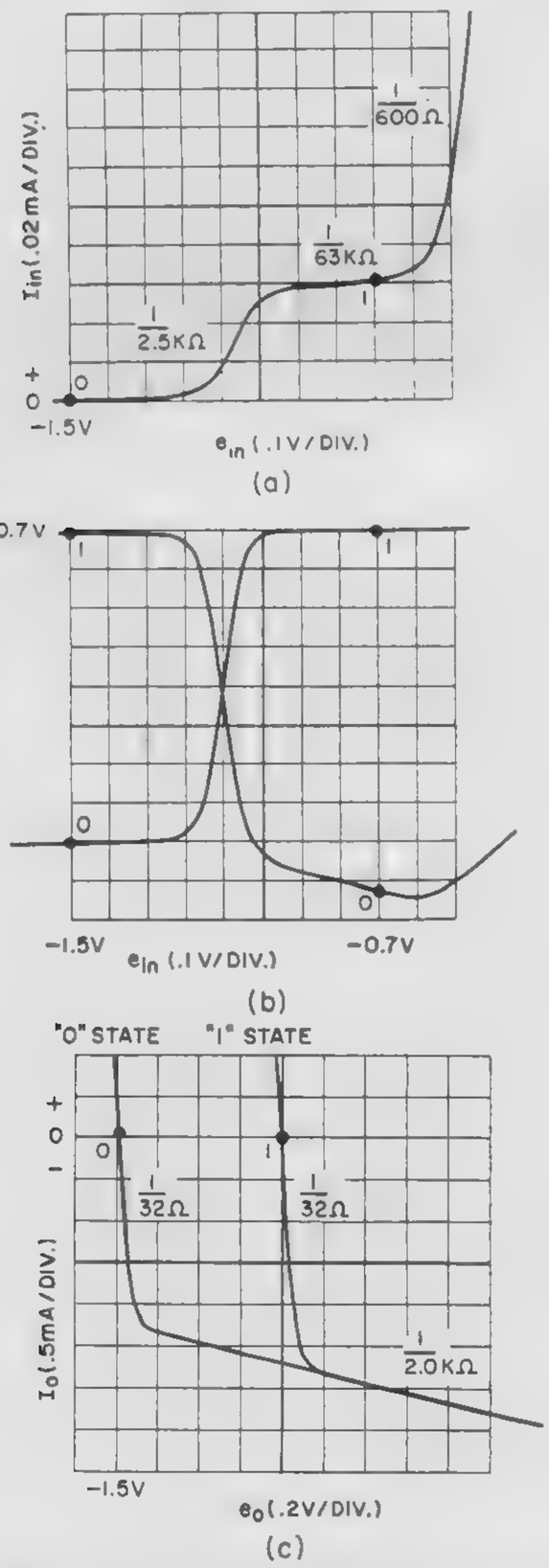


FIGURE 3—**The *dc* input characteristics *(a)*; transition characteristics *(b)*; and output characteristics of the logic gate *(c)*.**

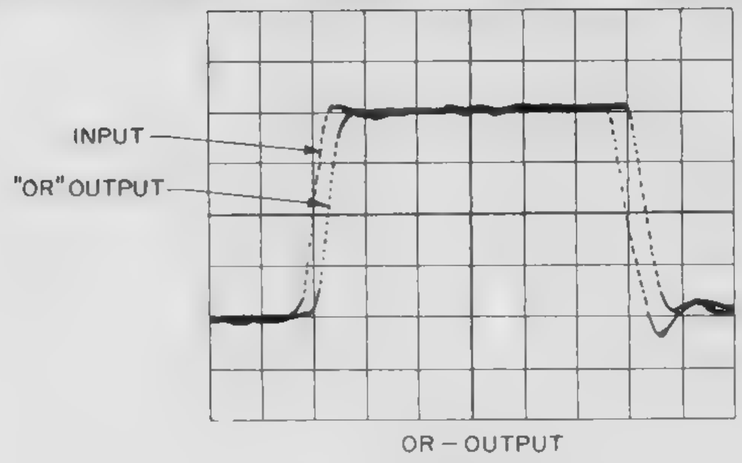


FIGURE 4—**Transient responses of the logic gate with a fan-out of 1: horizontal scale . . . *10 nsec/div*; vertical scale . . . 0.2 *v/div*.**

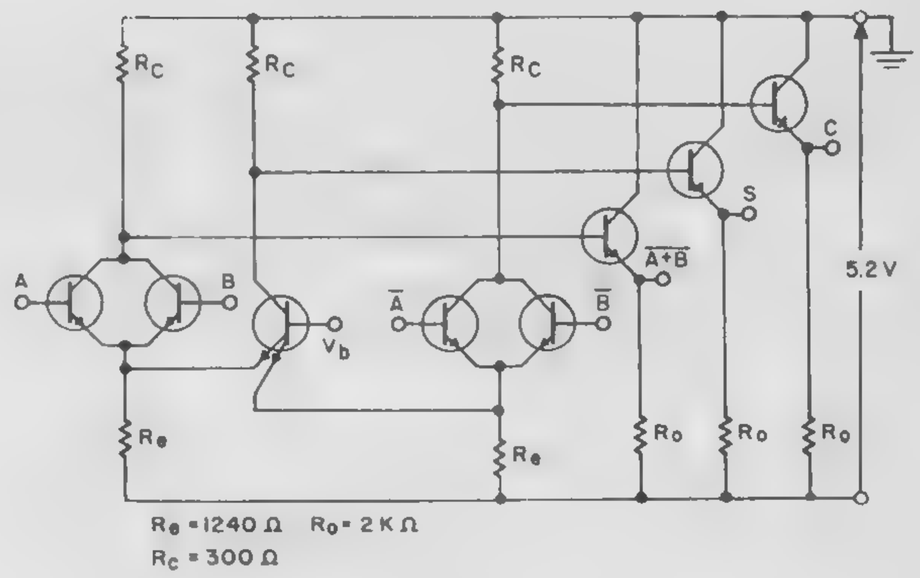


FIGURE 5—**Logic half-adder circuit employing a multiple emitter transistor. Note sum output available by connecting *C* and $\overline{A + B}$ outputs together.**

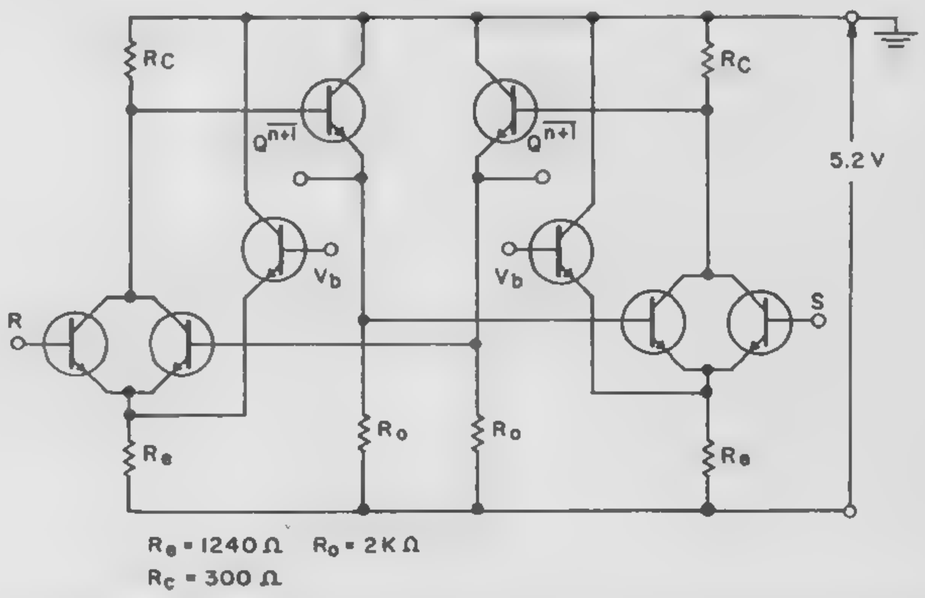


FIGURE 6—**Logic *R-S* flip-flop consisting essentially of two cross-coupled gates.**

SESSION XI: Integrated Circuits

FPM 11.5: A Semiconductor Network Multiplex Switch

G. Luecke

Texas Instruments, Inc.

Dallas, Tex.

W. E. Owen

Louisiana State University

Baton Rouge, La.

THIS PAPER will describe a semiconductor switch circuit suitable for miniaturized construction. A conventional circuit is shown in Figure 1. Transistors Q_1 and Q_2 are connected in series and operated in inverted fashion, with the collector and emitter connections interchanged. Complete *dc* isolation is obtained by driving the base-to-collector junctions from a transformer. The voltage-regulating diode and the *5000-ohm* resistors determine the base currents of Q_1 and Q_2. While this system works very well for circuits using conventional components, it is not practical for semiconductor networks because of the difficulty involved in constructing a transformer in a *70* x *200*-mil network package.

The operation of a capacitor-driven multiplex switch is illustrated in Figure 2. Here, the capacitor C is charged from the *dc* supply voltage V_{dc} during the *OPEN* or *OFF* period of the switch. After being charged, the capacitor is disconnected from the charging source and discharged through the base-to-emitter junctions of Q_1 and Q_2. The discharge current causes these transistors to conduct. The switch is therefore *CLOSED* or *ON*. During the *ON* period, the capacitor is completely disconnected from the charging source, and there can be no leakage to ground through the switch during the ON period.

The circuit diagram of a practical capacitor-driven multiplex switch, suitable for construction in semiconductor network form, is shown in Figure 3. A square-wave voltage is applied across terminals *1* and *2*. During the time that terminal *1* is positive with respect to *2*, CR_1 and CR_2 are forward biased and the capacitor will charge through CR_3. During this period the voltage drop across CR_3 produces a negative voltage at the bases of Q_1 and Q_2 with respect to their collectors. Therefore, Q_1 and Q_2 will not conduct and the switch will be *OFF*. During the period that terminal *1* is negative with respect to *2*, CR_1 and CR_2 are reverse biased and will not conduct. Therefore, the capacitor will discharge through the base-to-collector junctions of Q_1 and Q_2, closing the switch.

It is desirable to replace R_3, of Figure 3, with a constant-current circuit that will supply uniform base currents to Q_1 and Q_2 during the *ON* period and will permit the use of a small capacitance for *C*. Figure 4 shows a field-effect transistor circuit used for this purpose. The capacitor-discharge current during the *ON* period of the switch, is determined by the characteristics of Q_3 and the field-effect transistor source resistance, R_4. The base current to the switch transistors may be adjusted to optimum value by making R_4 variable.

The system shown in Figure 4 has been constructed, using conventional components, and provides excellent operation for both positive and negative input and output voltages at frequencies up to *50 kc*. Figure 5 shows the base-driving current, as a function of time, for the circuit of Figure 4 and a capacitance of *0.0045* μf. It will be noted that the base current is essentially constant for *20* μ*sec*. Maximum current is obtained at *—55°C* and the smallest initial current corresponds to a temperature of *100°C*. Figure 6 shows the improvement in temperature characteristics that results from connecting a forward-biased diode in series with R_4.

Low offset voltages, characteristic of inverted operation of the switch transistors, are accompanied by relatively low breakdown voltages. Therefore, inverted switch operation is used for switching low voltage levels, where small offset voltages are important, and normal switch operation is used for switching high voltage levels, where high voltage breakdown is necessary.

Signal Source Resistance	*100 ohms*
Output Load Resistance	*10,000 ohms*
On Resistance	*50 ohms*
Offset Voltage	*250* μv
On Leakage To Ground	10^{-7} *a*
Chopping Rate	*5* to *50 kc*
Chopped Signal Levels	± 5 *v*
Drive Required for ± 5-*v* Level	*12-v* peak-to-peak square wave on a *—9 v* *dc* level
Power Dissipation	*10 mw*

***TABLE 1*—Projected performance characteristics of the semiconductor network SN307 multiplexer. Construction of a capacitor-driven switch in semiconductor network form is in progress.**

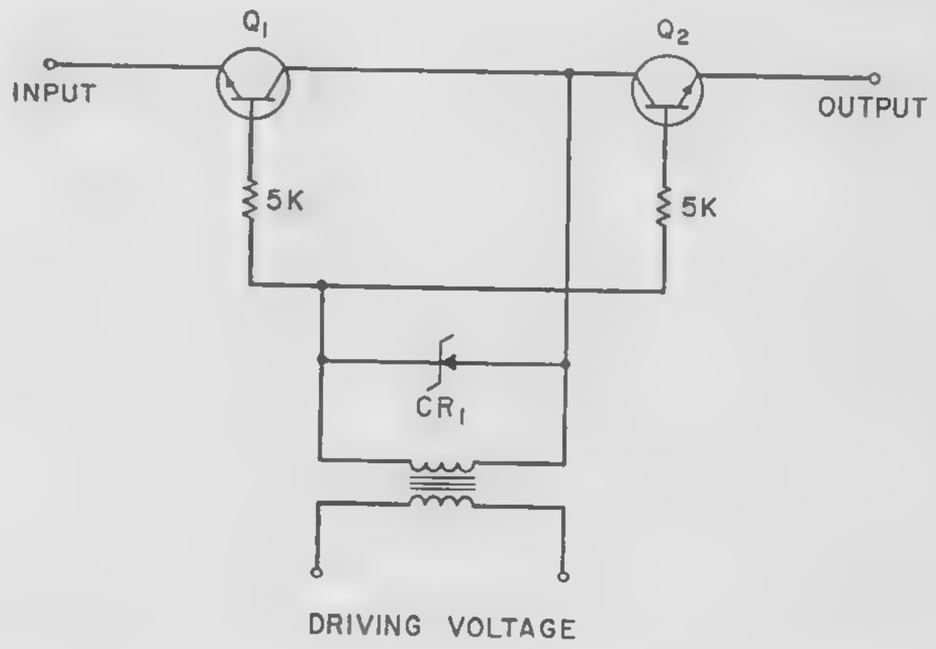


***FIGURE 1*—Conventional transistor multiplex switch circuit.**

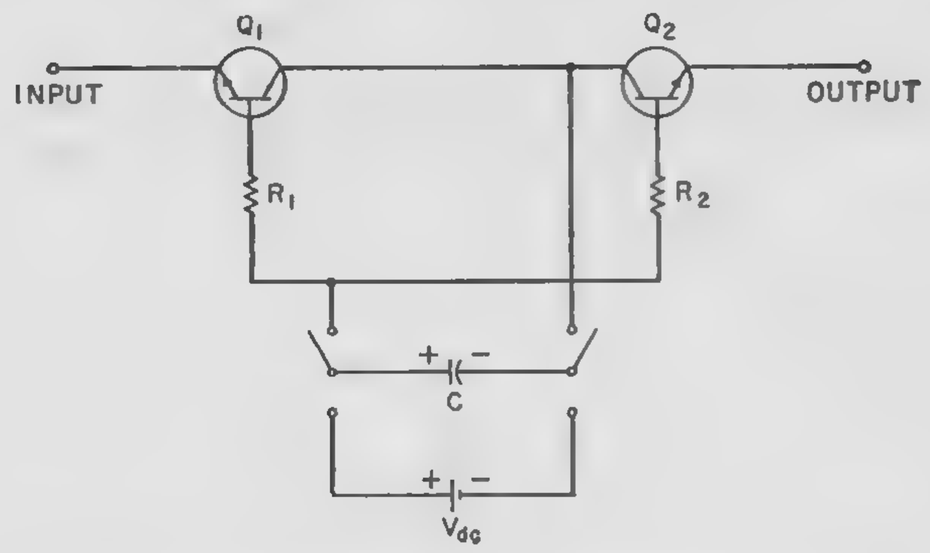


FIGURE 2—Capacitor-driven transistor multiplex switch.

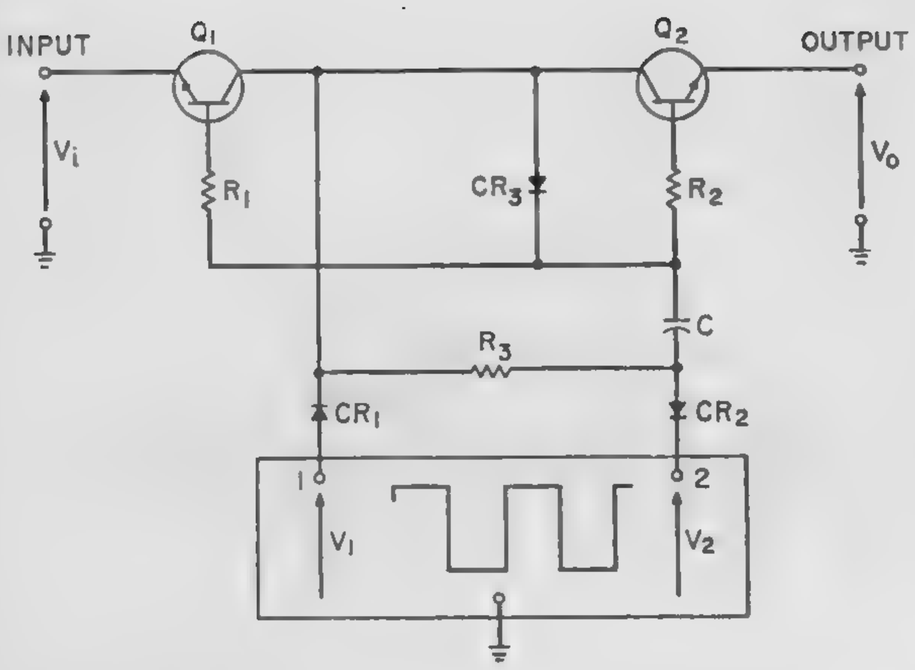


FIGURE 3—A practical capacitor-driven transistor multiplex switch.

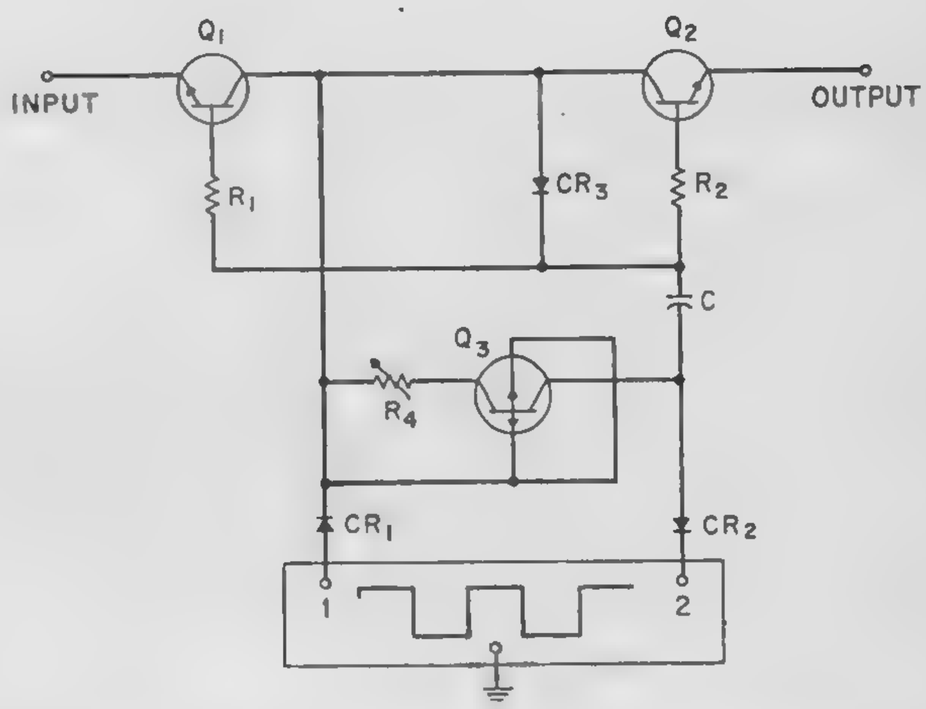


FIGURE 4—Multiplex-switch circuit with adjustable constant-current drive.

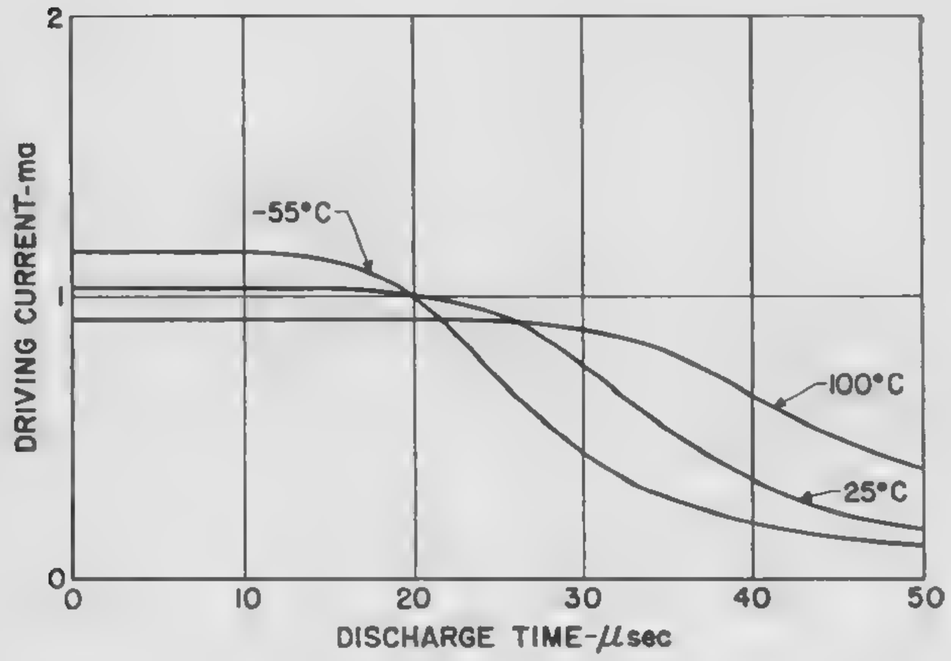


FIGURE 5—Performance of field-effect transistor drive circuit. The period for essentially constant-current drive may be increased to any desired value by a proportionate increase in the capacitance of *C*.

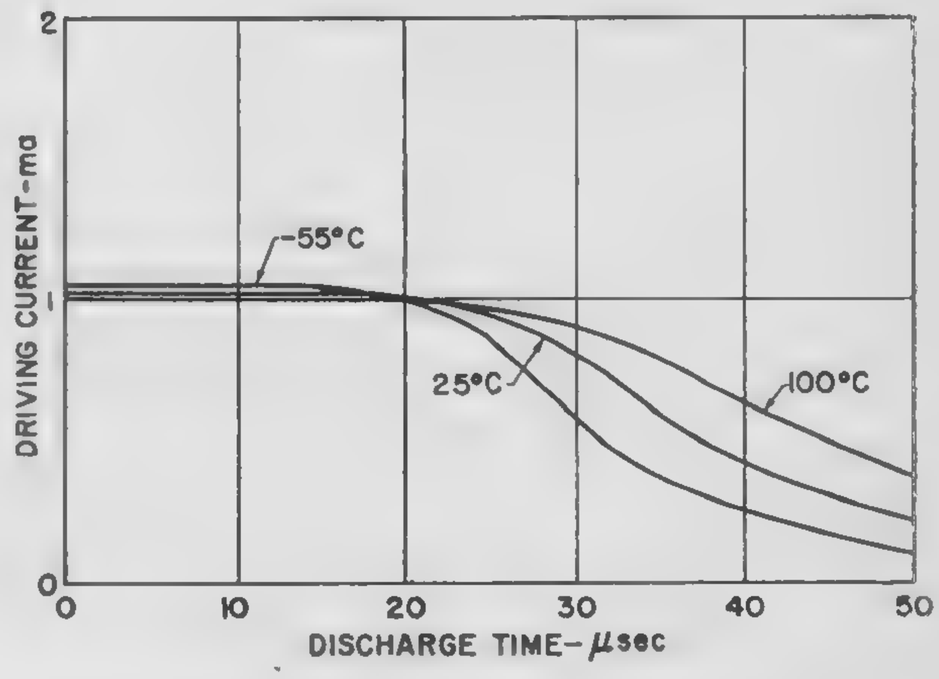


FIGURE 6—Performance of drive circuit with temperature compensation.

SESSION XII: Optoelectronics

Chairman: E. I. Gordon
Bell Telephone Laboratories, Inc., Murray Hill, N. J.

FPM 12.1: GaAs Infrared Source for Optoelectronic Applications

J. R. Biard, E. L. Bonin, W. N. Carr, G. E. Pittman

Texas Instruments, Inc.

Dallas, Tex.

MANY OPTOELECTRONIC circuitry applications not previously exploited require a high-efficiency, high-speed optical source with long life expectancy. This paper will describe a junction diode fabricated in GaAs which rather uniquely fills the foregoing requirements.

Radiation at a photon energy corresponding to slightly less than the GaAs energy band gap is obtained by forward biasing the *pn* junction. The spectral output obtained from a typical experimental infrared source[1] shown in Figure 1 is seen to peak at *1.40 ev* for a junction at room temperature. For operation in the spontaneous emission mode, the energy of the photon radiation increases upon cooling to *1.48 ev* at *100°K*. A detailed plot of the radiation energy maximum E_p as a function of temperature for low current densities is shown in Figure 3. The shift of the emission peak shows the same variation with temperature as the band gap E_g. At room temperature and *100°K* the photon output is confined to a radiation band of half width measuring *0.041* and *0.024 ev* or *250* and *140 Å*, respectively.

The overall quantum (electron to photon) efficiency η has been measured using three independent techniques. Good correlation between experimental data has been obtained as shown in Figure 3. The quantum efficiency is typically *0.1%* at room temperature and for some devices is as high as *0.27%*. The quantum efficiency typically increases by a factor of *ten* upon cooling to the liquid nitrogen temperature range for units operating in the spontaneous emission mode. Better units have quantum efficiencies as high as *2.4%* at *95°K*. An analysis of the optical geometry of the source indicates that by permitting all of the internally generated radiation to leave the GaAs, the overall quantum efficiency η could be increased by a factor of at least *22*.

The spatial radiation pattern of the infrared unit is shown in Figure 4. The radiation is concentrated in a *60°* solid angle about the normal from the GaAs source.

Microwave Modulation Capability

The microwave modulation capability of the GaAs infrared source units was successfully demonstrated using a *pin* silicon diode detector in a tuned mount. Amplitude modulation of the infrared source was successfully obtained at various frequencies between *500* and *900 Mc* as limited by the range of the test equipment. No tendency toward cutoff for the infrared source was noted in this frequency range, and higher modulating frequencies should be possible.

The GaAs infrared source is particularly suited for exciting both Si and Ge photosensitive devices, since the *1.4 ev* photon energy is well above the threshold energy required for hole-electron pair generation in both these materials. The complete electrical isolation obtainable between networks, using the infrared source as an input, is used in the molecular low-level photo-chopper of Figure 5. The GaAs source is coupled to the double-emitter silicon photo-transistor structure by the light pipe. Optical generation of minority carriers takes the place of the collector-base drive normally used in transistor choppers.

A *Darlington* circuit, using an optical input and output shown in Figure 6, performs an *OR* logic function with a fan-in of *3*. The circuit remains clamped in the *ONE* position upon introduction of an input light pulse and is useful for performing threshold type logic with unconditional reset.

Infrared Source For Triggering

With sufficient optical coupling, mechanisms such as avalanche injection may be triggered in photo-sensitive devices using the GaAs source. Circuits using the infrared source to trigger *pnpn* switches have been designed and tested.

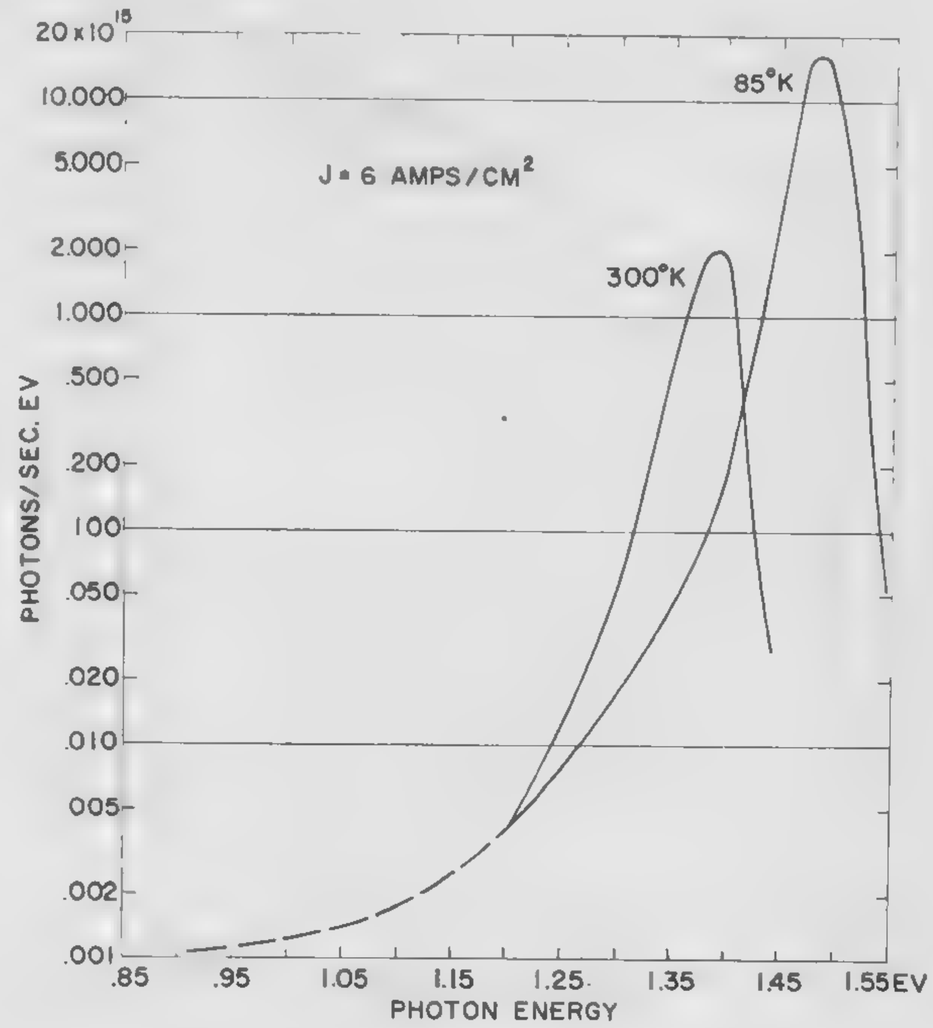


FIGURE 1—Radiated photon flux versus photon energy.

[1] SNX 100.

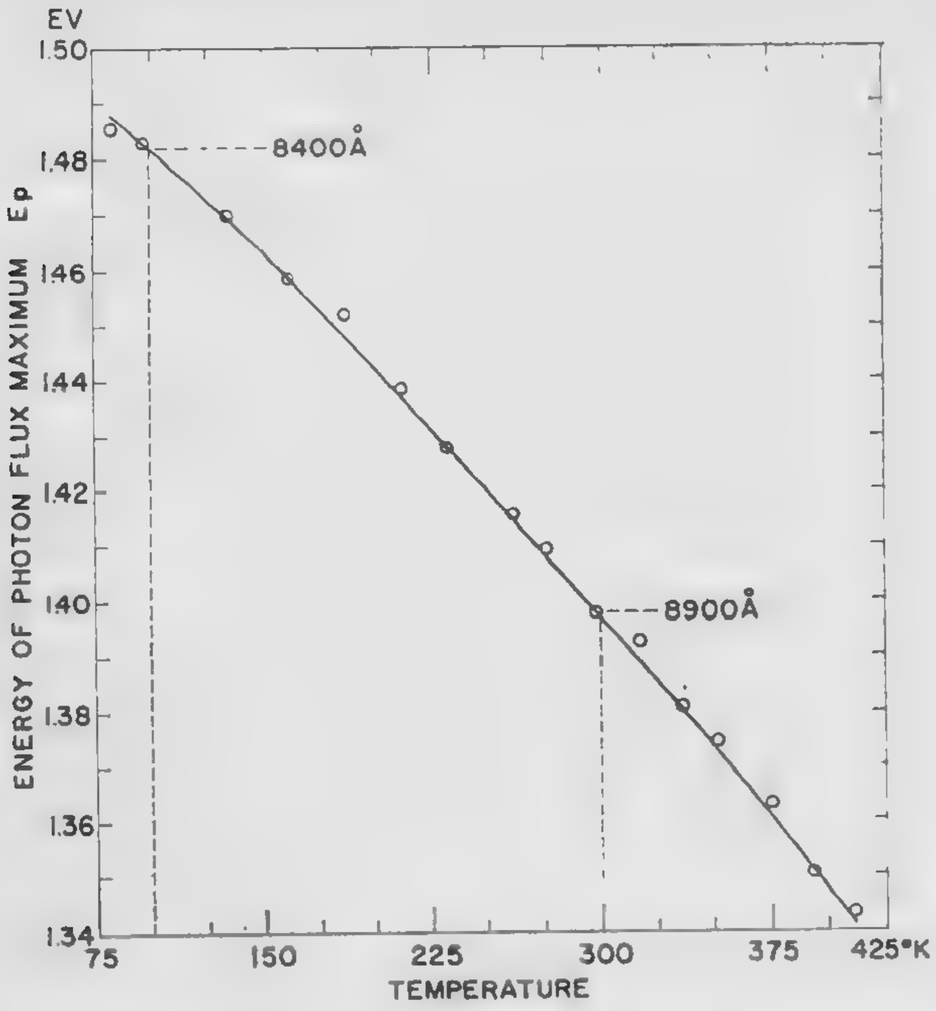


FIGURE 2—Energy of maximum photon flux versus junction temperature.

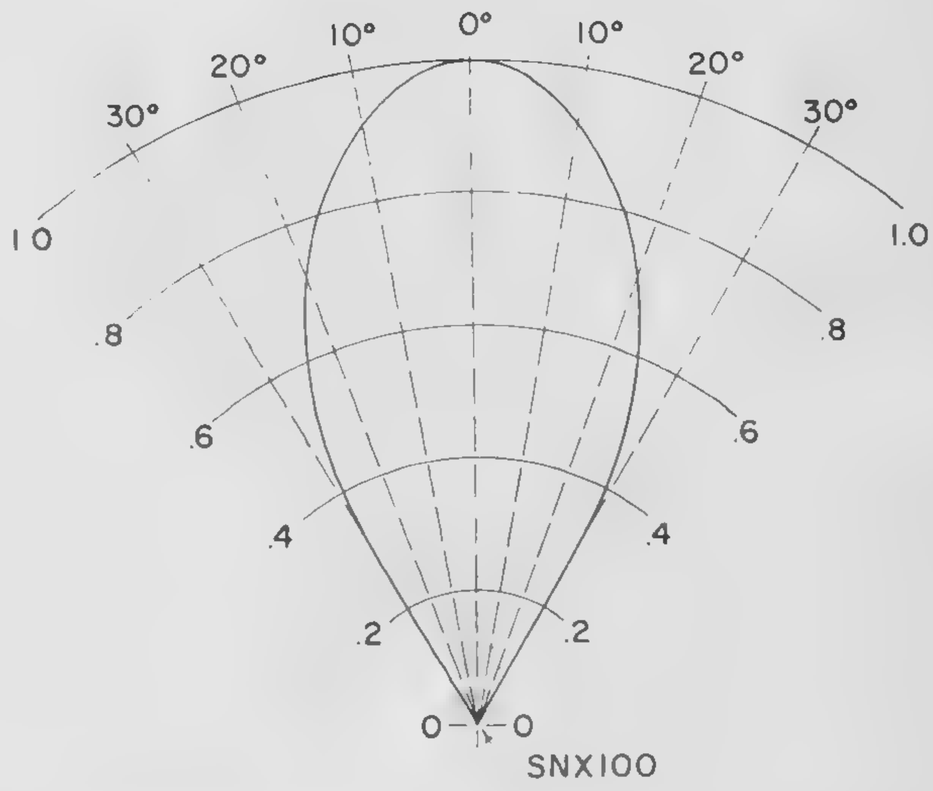


FIGURE 4—Spatial radiation pattern of experimental infrared source.

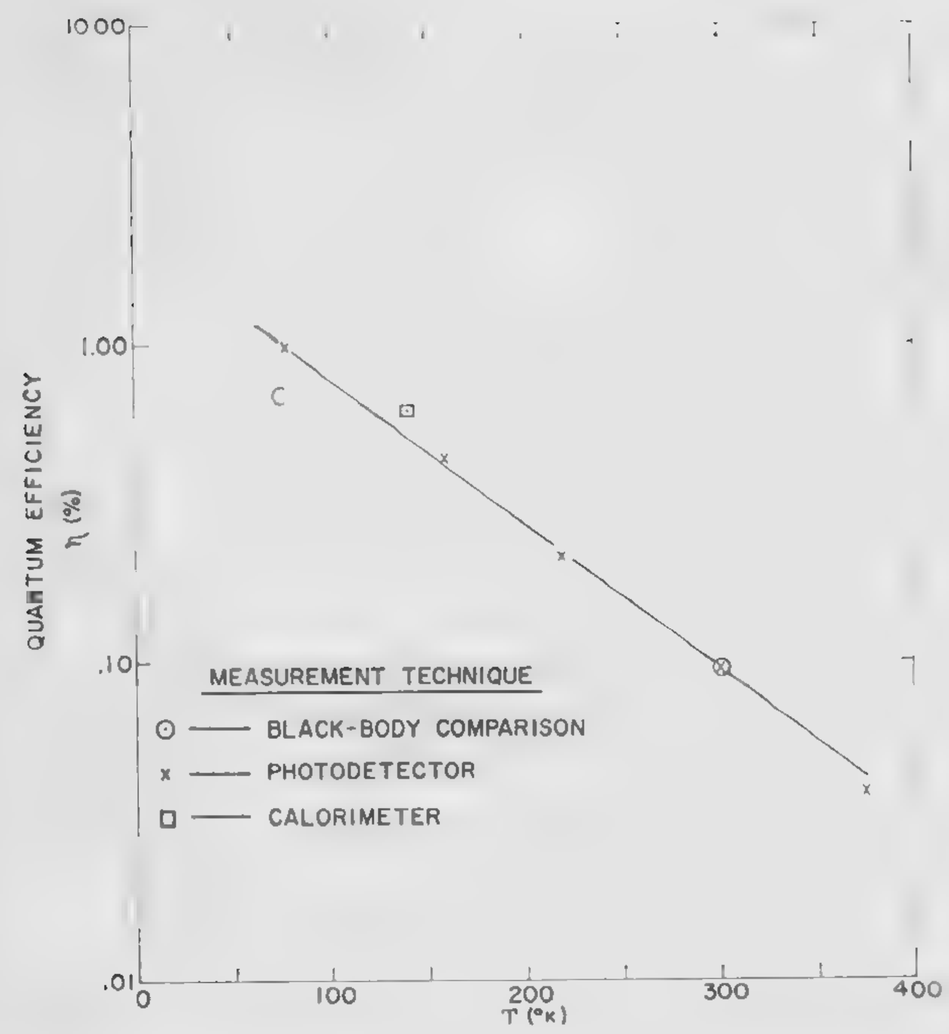


FIGURE 3—External electron to photon conversion efficiency (η) versus junction temperature °K.

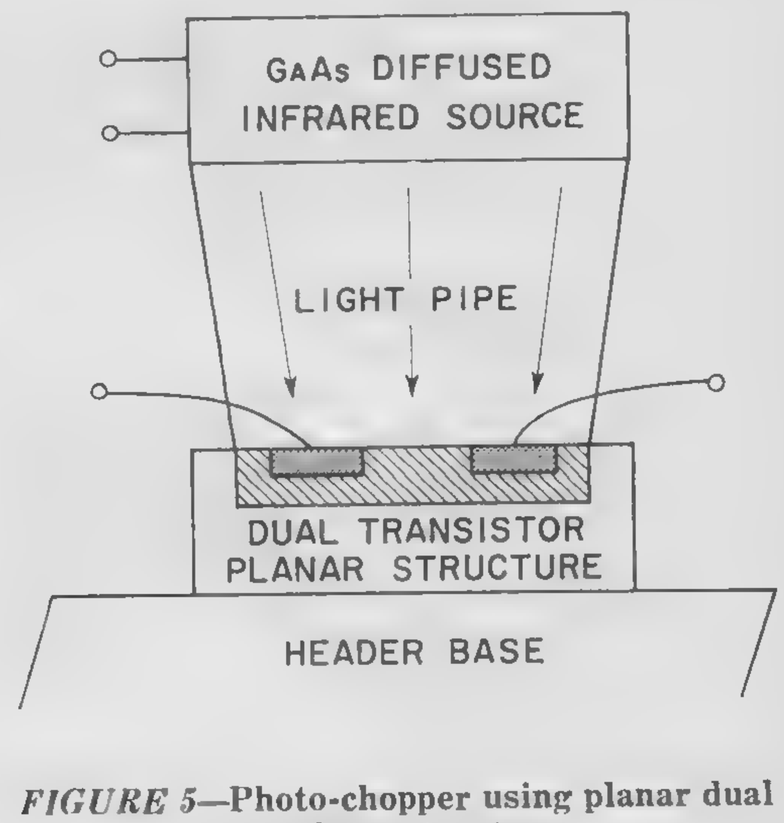


FIGURE 5—Photo-chopper using planar dual transistor structure.

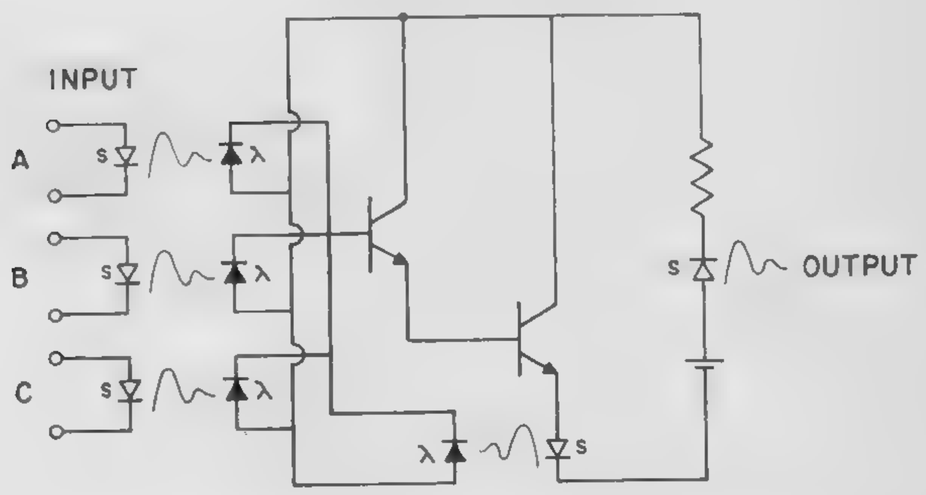


FIGURE 6—*OR* gate with fan-in *3* using optical coupling.

SESSION XII: Optoelectronics

FPM 12.2: Gallium Arsenide Injection Laser

F. H. Dill, Jr.

Thomas J. Watson Research Center, IBM Corporation

Yorktown Heights, N. Y.

LASERS have aroused great interest in the electronic field, both as coherent, highly directional light sources and for their promise in broadband communication. This paper will describe a GaAs infrared laser in which the pumping is provided by injection of carriers across a *pn* junction. The coherent light produced by recombination of the injected carriers can be modulated directly by varying the input current. This represents a major advance over optical or electrical discharge pumping in ease and simplicity of pumping and modulating the laser beam.

The high efficiency of recombination radiation from forward-biased GaAs diffused junctions has been reported by many[1]. In the spontaneous emission region, which occurs at low current densities, a broad spectral line is observed in the near infrared at about *8400 Å* with a linewidth at *77°K* of about *140 Å*. This light is generated with an efficiency approaching one photon produced for each electron which passes through the junction. The light appears to be generated in a region about *10-microns* thick on the *p* side of the junction and is due to recombination of injected electrons from the conduction band[2]. At higher current densities the photons generated can stimulate excited electrons in the conduction band to recombine, producing more photons which are similar in frequency, phase, and direction. This stimulated emission appears as a narrowing of the spontaneous spectral line and was first observed by *Nathan*[3] and *Hall*[4]. By providing suitable optically resonant structures so that particular wavelengths are favored, a laser which gives an extremely narrow optical line can be constructed. At currents well below the threshold for laser action the laser will show only the spontaneous emission. At the threshold, however, a very sharp line rises up out of the background radiation decreasing the linewidth dramatically; Figure 1.

A typical injection laser is illustrated in Figure 2. The *pn* junction is parallel to the top surface with the top *p* side contacted by an indium sphere. The reflecting surfaces perpendicular to the plane of the junction are made by cleaving the crystal to produce optically flat and parallel *{110}* faces. Lasers with four cleaved sides are made by initially diffusing into a wafer oriented in the *{100}* direction.

There are two basic types of modes which can be supported in a rectangular laser. Because of the high absorption of *8400 Å* light by GaAs, only those modes which lie entirely within the thin excited layer can survive. The first of these modes shown in Figure 3*a* utilizes total internal reflections. The relative *Q* of these modes is high because the losses at the surface are small. Lasers with four cleaved faces have shown the lowest threshold for laser action. At *77°K* these lasers have been operated at under *300 ma*. This threshold drops below *20 ma* in liquid helium. Such lasers can easily be run continuously[5]. Because the internal reflection modes are trapped within the crystal one might expect difficulty in observing the coherent light. The cleaved surfaces have enough imperfections so that this condition presents little problem. Only a few of these diodes show strong directional characteristics.

If two opposite surfaces of the laser do not contribute to internal reflections then only the *Fabry-Perot* modes shown in Figure 3*b* are allowed. Non-contributing surfaces can be produced by either sawing or etching. These structures require a higher level of excitation than the internal reflection modes, since more than *60%* of the light is lost at each reflection. A gain of at least *2.5* must be obtained in each pass through the crystal. Thresholds here typically run in the range of *6 a* at *77°K*. In the *Fabry-Perot* lasers, however, the coherent light beam is confined to a small angle which is desirable for a number of applications.

As an electronic device the injection laser differs from previous lasers chiefly in size, method of pumping, and in the characteristic time associated with the recombination of carriers. In size, the actual excited region which generates light is a thin sheet *½-mil* thick, *5-mils* wide, and *20-mils* long. The length and width can be greatly extended, but the thickness is not likely to change significantly. This very small volume implies a power limit far below that possible with large optically pumped crystals. The small size also limits the directionality of the beam because of diffraction. This problem can be eliminated by the use of a lens of focusing lens or mirror.

The method of pumping the laser is very significant since it is direct and electrical. This provides a convenient means of regulating the input power and thus of modulating the beam. Modulation has been very difficult with other lasers.

The third major difference is the recombination time associated with excited electrons. For GaAs spontaneous emission this time is 10^3 to 10^9 times shorter than for materials used for other lasers. This should have a very important bearing on the modulation rate achieved by varying the pumping power. Stimulated emission recombination times are considerably shorter than those for spontaneous emission, but the latter should be a rough guide as to the modulation rate that can be accepted by a laser. The spontaneous emission from GaAs has been modulated at very high rates[1] and it is certainly reasonable to expect modulation at *kMc* rates from GaAs injection lasers.

Acknowledgments

The author would like to acknowledge particularly the help of *S. E. Blum* in providing crystals, *Miss A. R. Benoric* and *E. W. Harden* for fabricating lasers, and many members of the staff of the Thomas J. Watson Research Center for measurements and discussion.

[1] Pankove, J. I., and Berkeyheiser, J. F., "A Light Source Modulated at Microwave Frequencies," *Proc. IRE*, p. 1976-77; Sept., 1962.
Keyes, R. J., and Quist, T. M., "Recombination Radiation Emitted by Gallium Arsenide," *Proc. IRE*, p. 1822; August, 1962.
Black, J., Lockwood, H., and Mayburg, S., post-deadline paper, *Baltimore American Physical Society Meeting;* March, 1962.

[2] Michel, A. E., Walker, E. J., and Nathan, M. I., *IBM Journal;* January, 1963.

[3] Nathan, M. I., Dumke, W. P., Burns, G., Dill, Jr., F. H., and Lasher, G., "Stimulated Emission of Radiation from GaAs PN Junctions," *Appl. Physics Letters*, p. 62-64; November 1, 1962.

[4] Hall, R. N., Fenner, G. E., Kingsley, J. D., Soltys, T. J., and Carlson, R. O., "Coherent Light Emmission from GaAs Junctions," *Phys. Review Letters*, p. 366-368; Nov. 1, 1962.

[5] Howard, W. E., Fang, F. F., Dill, Jr., F. H., and Nathan, M. I., *IBM Journal;* January, 1963.

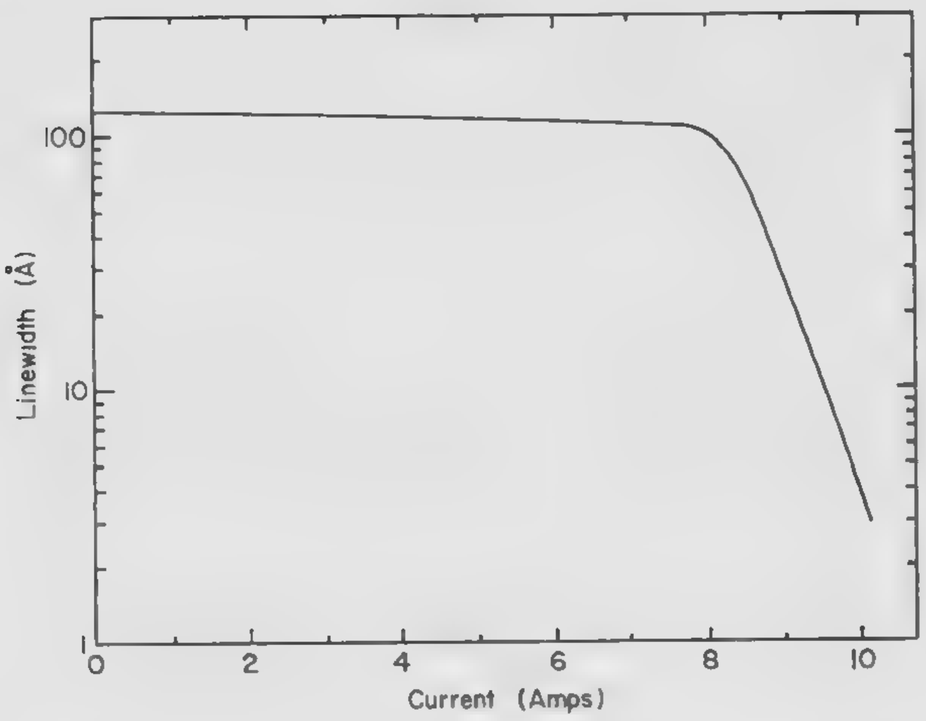


FIGURE 1—Curve of spectral linewidth as a function of current density for a GaAs injection laser.

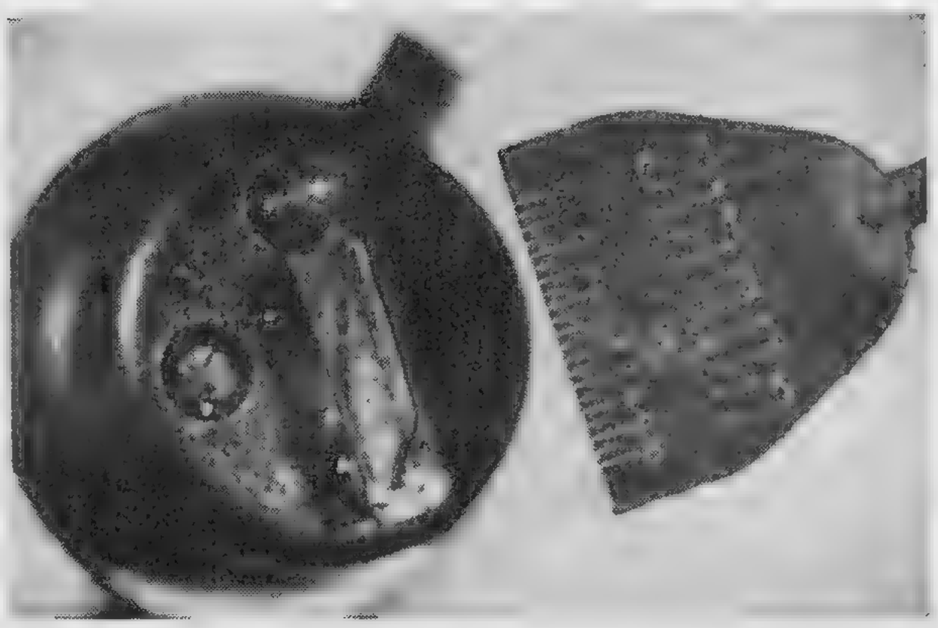


FIGURE 2—Photo of a GaAs laser with scale *0.1"* long.

FIGURE 3a and *b*—A typical internal reflection mode in a rectangular laser is shown in *(A)*; a *Fabry-Perot* mode in a rectangular laser in *(B)*.

SESSION XII: Optoelectronics

FPM 12.3: Cuprous Chloride Light Modulators*

F. Sterzer, D. J. Blattner, H. C. Johnson, S. Miniter

Electron Tube Division, RCA

Princeton, N. J.

Most solid-state optical modulators use crystals that exhibit the linear electrooptic effect. In these crystals, the index of refraction, n, is a linear function of applied electric field, E. The changes in refractive index are very small. Even for crystals exhibiting the largest known effect, $\triangle n/E$ has a value on the order of only 10^{-11} m/v. Still, the effect is large enough to produce phase differences of *180°* between linearly-polarized waves in crystals of practical size, and thus can be used to rotate the direction of polarization of a light wave.

In the basic modulator, a crystal is aligned with its optic axis along the direction of the light beam and is placed between crossed polarizers; Figure 1. When no electric field is applied, no light is transmitted through the analyzer. If an electric field is then applied across the crystal, the plane of polarization of the light passing through the crystal is rotated and light is transmitted through the analyzer, provided certain relationships between the direction of polarization of the light incident on the crystal, the directions of its crystallographic axes, and the direction of the applied electric field are satisfied. The intensity of the transmitted light as a function of the applied voltage varies as $\sin^2\left(\frac{\pi V}{2V_{\lambda/2}}\right)$, as shown in Figure 2. The term $V_{\lambda/2}$ is the voltage required for maximum transmission.

Our modulators use crystals of cuprous chloride grown from the melt by the *Bridgman* method[1]. The crystals are transparent from *0.4* to *20.5 microns* and have a relative complex dielectric constant $\varepsilon'/\varepsilon_o - j\varepsilon''/\varepsilon_o$ which ranges from $6.4(1-j\,0.002)$ to $8.7(1-j\,0.001)$ at a frequency of *6 Gc*. Although the optical quality of the crystals is good, the largest reasonably-unstrained samples have volumes of only a few cubic millimeters.

The minimum low-frequency values of $V_{\lambda/2}$ for CuCl (measured at *5461 Å*) are *6.2 kv* and $7.2\frac{c}{b}$ *kv*, respectively, in the longitudinal and transverse operations; shown in Figure 1[1a, 2]. These minimum values are obtained when the crystal is oriented with its *(100)* plane perpendicular to the electric field in the longitudinal case, and with its *(111)* plane perpendicular to the electric field in the transverse case. The power, P_{in}, required to produce a voltage of amplitude V across the crystal can be calculated as follows:

$$P_{in} \approx \frac{V^2}{2}\,\omega\,\varepsilon'\frac{ab}{c}\,tan\,\delta$$

where $tan\,\delta$ is the loss tangent of the crystal material, and a, b, and c are the dimensions of the crystals as defined in Figure 1.

CuCl modulators have the following important advantages over modulators using dihydrogen phosphate crystals; e.g., KDP, ADP[3]:

(1)—None of the dihydrogen phosphates transmits wavelengths longer than *1.7 microns*. Thus, unlike CuCl, they cannot be used to modulate infrared radiation above *1.7 microns*.

(2)—Because the dihydrogen phosphates are uniaxial in the absence of an electric field, the angular aperture of modulators using ADP or KDP is orders of magnitude smaller than the angular aperture of modulators using CuCl. Figure 3 shows photographs of divergent light transmitted by a round ADP modulator and by a wedge-shaped CuCl modulator. With the ADP modulator, only the very center of the pattern is usable; with the CuCl modulator, there is nearly complete extinction and complete transmission for all light rays. Figure 4 shows the calculated angular apertures of a modulator using a single CuCl crystal and of a *compensated* modulator using two crystals in series. The calculations are for crystals placed between crossed circular polarizers.

(3)—Because the dihydrogen phosphates exhibit only a longitudinal effect‡, they require either transparent electrodes (which are not operable at high frequencies) or electrodes with holes (which operate only with fringing fields). CuCl modulators, using the transverse effect, do not suffer from these limitations; Figure 2.

CuCl light modulators have been operated in both longitudinal and transverse modes. Visible and infrared radiation (*2.4 microns*) were modulated. The highest modulation rate *(1 Gc)* was obtained in a reentrant cavity modulator of the type shown in Figure 5.

CuCl is a promising material for the construction of wideband microwave light modulators. Figure 6 shows a proposed traveling-wave modulator; the CuCl is placed in a ridged waveguide, and the width of the crystal is adjusted to maintain synchronism between the microwave electric field and the light beam being modulated.

* Sponsored by Electronic Technology Laboratory, ASD, AFSC, Wright-Patterson AFB, Ohio, under Contract AF33(616)-8199.

[1] Processed at RCA Semiconductor Division.

‡ The dihydrogen phosphates can be used in a transverse mode only with extremely monochromatic light.

[1a] West, C. D., "Electrooptic and Related Properties of Crystals With the Zinc Blende Structure," *J. Opt. Soc. Am.*, p. 335; April, 1953.

[2] Namba, S., "Electrooptical Effect of Zinc Blende," *J. Opt. Soc. Am.*, p. 76-79; January, 1961.

[3] Billings, B. H., "The Electrooptic Effect in Uniaxial Crystals of the Type XH_2PO_4," *J. Opt. Soc. Am.*, p. 797-808; Oct., 1949.

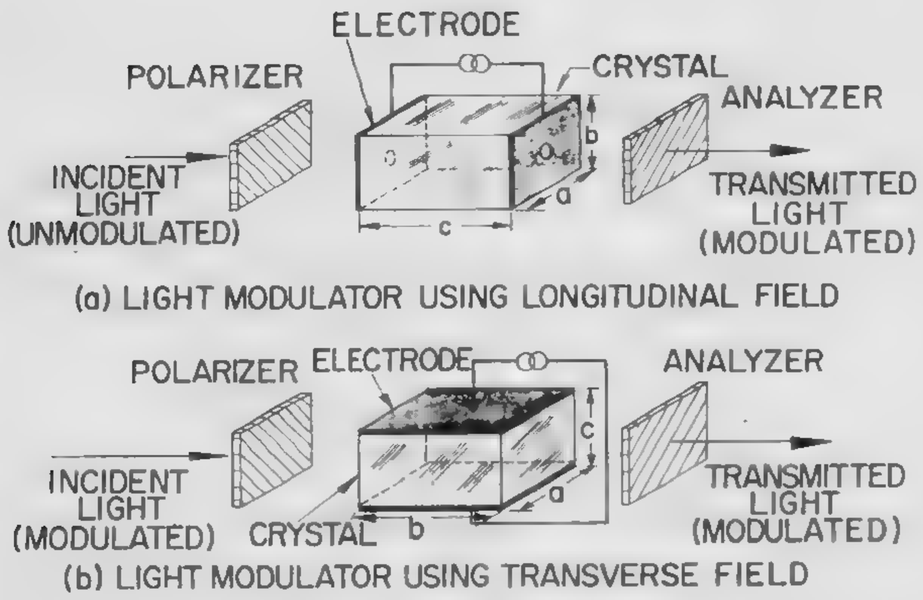


FIGURE 1—Basic modulators using electrooptic crystals.

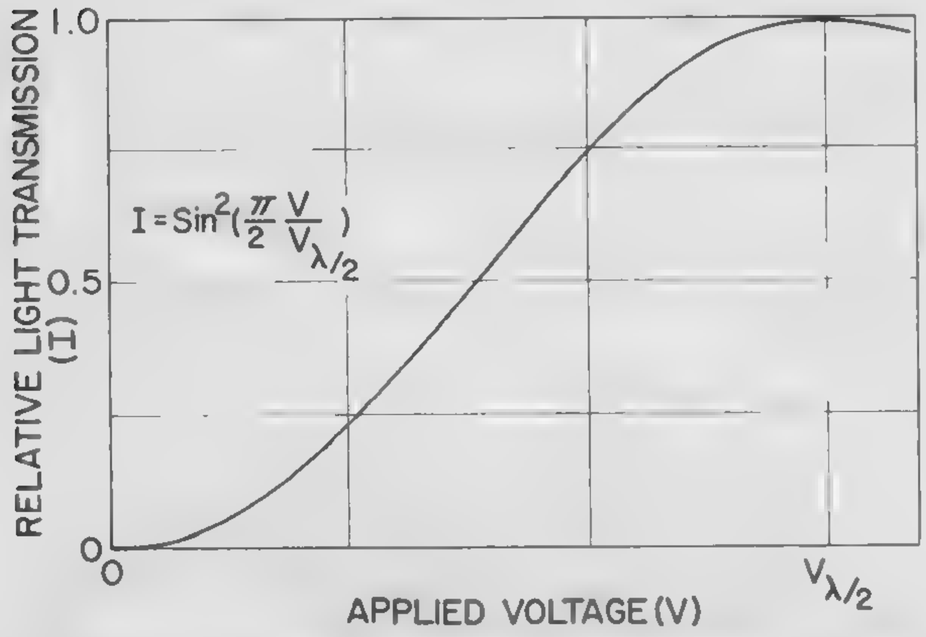


FIGURE 2—Light modulator transmission *versus* applied voltage.

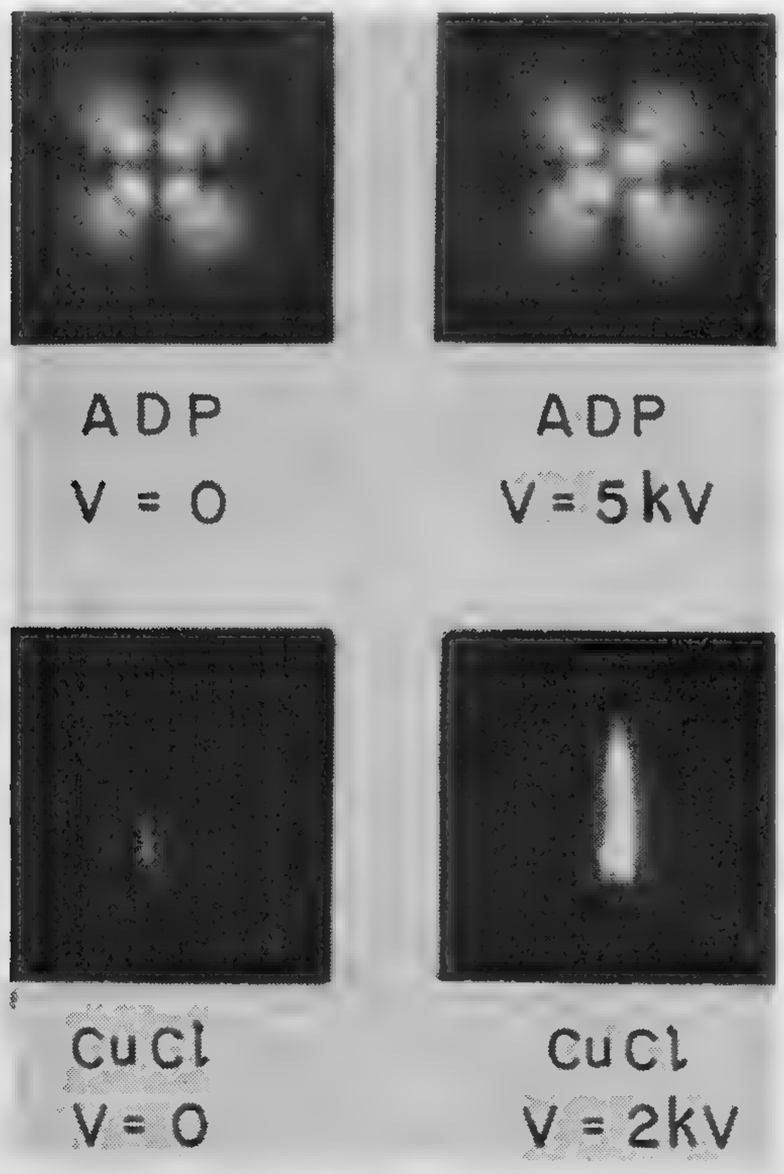


FIGURE 3—Photographs illustrating the superior angular aperture of CuCl light modulators.

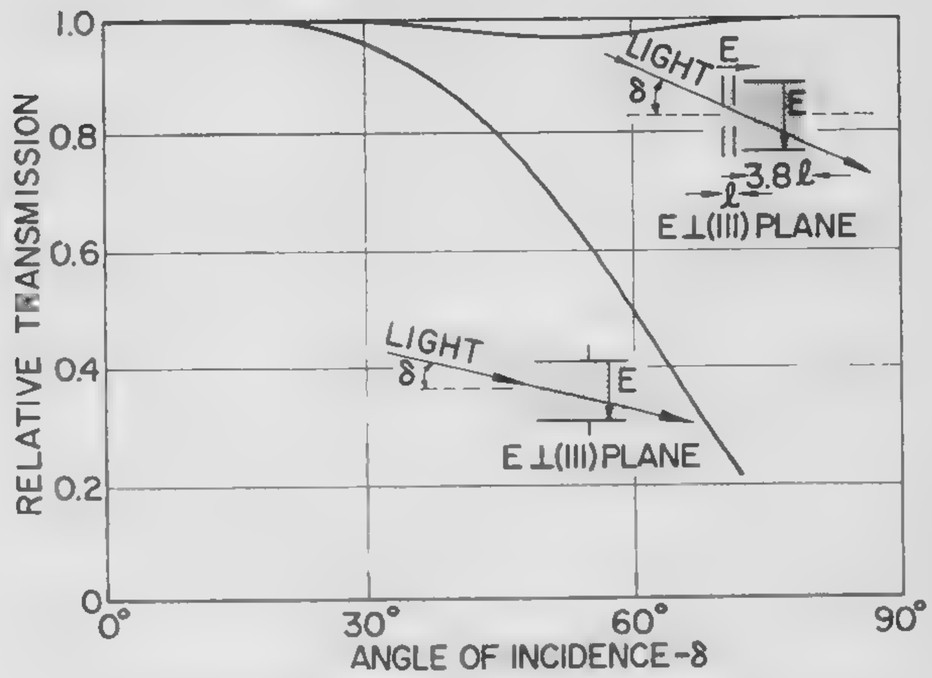


FIGURE 4—Angular apertures of CuCl light modulators.

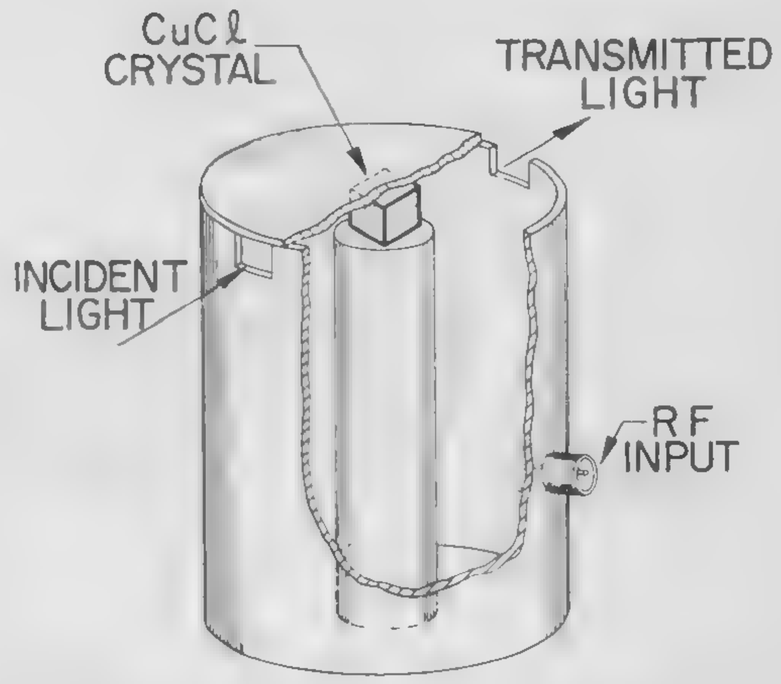


FIGURE 5—Reentrant cavity microwave light modulator.

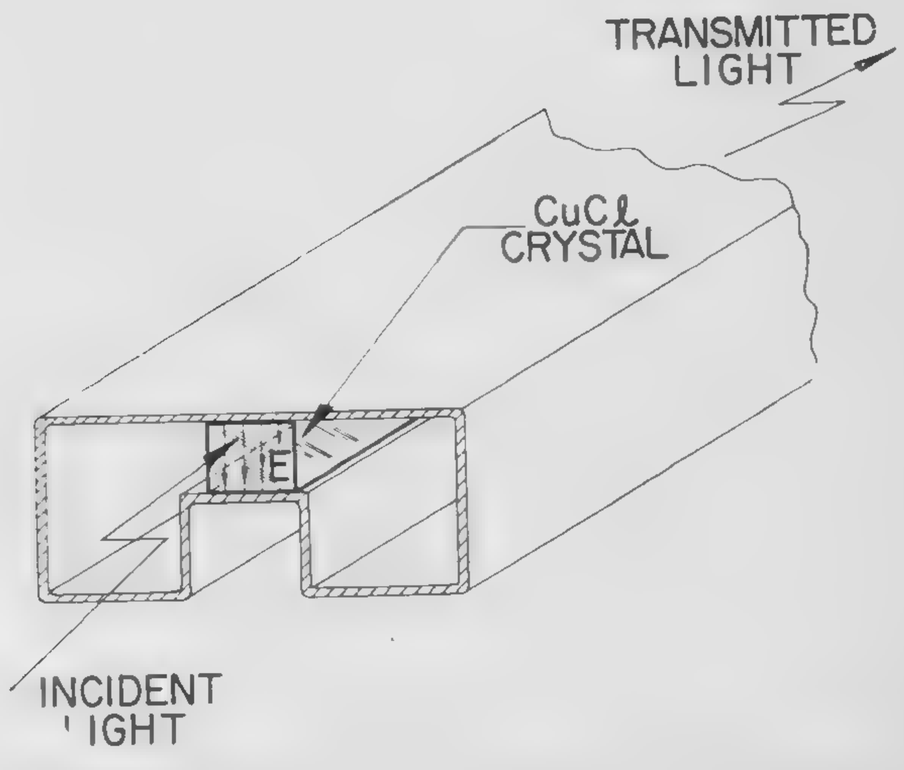


FIGURE 6—Traveling-wave modulator using CuCl in ridged waveguide.

SESSION XII: Optoelectronics

FPM 12.4: The PIN Junction Photodiode as a Detector of Light Modulated at Microwave Frequencies

L. K. Anderson

Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

A REVERSE-BIASED *PIN* junction with a sufficiently thin intrinsic region can be used as a demodulator of light modulated at microwave frequencies[1-4]. Recently, *Riesz*[4] has described a germanium photodiode with a surface *PIN* junction, a cross-section of which is shown in Figure 1. Most of the light incident on the diode passes through the thin N-layer and is absorbed in the nearly intrinsic π-layer. The carriers produced are swept out by a large reverse bias and collected in the p-region and at the gold electrodes evaporated on to the N-layer. The π-layer is about *2.5 microns* thick, so that transit times as short as 5×10^{-11} seconds, corresponding to a cutoff frequency in the vicinity of *20 Gc*, may be realized.

The production of electron-hole pairs is virtually instantaneous, so that the modulation frequency response of this form of detector is determined primarily by *(i)* transit time effects and *(ii)* circuit parameters of the diode; in particular, the shunt capacitance and series resistance.

A high-frequency equivalent circuit for the *Riesz* diode is shown in Figure 2, together with an expression for the modulation-frequency power available from the diode. The capacitance C is determined by the area and thickness of the π-layer, the series resistance R_s largely by the sheet resistivities of the N-layer and the gold electrode. The detection process is represented by a current generator $i(\omega)$ whose value is given by:

$$i(\omega) = q\eta \mathrm{MK}\varphi_o f(\omega\tau), \qquad (1)$$

where q is the electronic charge, η the quantum efficiency of the semiconductor (close to unity for incident radiation of energy higher than the band gap), M the amplitude modulation index of the incident light, K the fraction of the incident photon flux φ_o reaching the active area of the diode, and $f(\omega\tau)$ a transit time reduction factor.

The form of $f(\omega\tau)$ depends on such details as the relative velocities of holes and electrons and the depth of penetration of radiation into the π-layer. Figure 3 shows $f(\omega\tau)$ for the special case of equal hole and electron drift velocities. The parameter $b \equiv aW = au\tau$, where a is the optical absorption coefficient, W the thickness of the π layer, u the drift velocity, and τ the transit time, is a measure of the depth of penetration of radiation into the junction. The value $b = \infty$ then corresponds to all the radiation being absorbed at the boundary of the π-layer, for which case $f(\omega\tau)$ reduces simply[5] to $\dfrac{\sin(\omega\tau/2)}{\omega\tau/2}$.

The power available from the diode at any modulation frequency is proportional to $K^2|f(\omega\tau)|^2/R_sC^2$. In an optimum design the junction width is chosen so as to achieve as low a capacitance as possible consistent with a short transit time. The electrode structure used to establish ohmic contact on the illuminated side of the junction (Figure 1) is selected so as to achieve as low a series resistance as possible without intercepting an excessive fraction of the incident light. An analysis of the problem shows that for the case $b = \infty$ the optimum junction width is such that the transit time is one half the rf period, while an optimum electrode structure consists of a large number of interconnected conducting strips covering approximately half the active area of the diode.

A complete, quantitative measurement of the modulation sensitivity of a photodiode requires the use of a *cw* light source in conjunction with an optical modulator capable of operation over the entire frequency range of interest, although qualitative data can be obtained by observing beats between axial modes of an optical maser[2]. Useful information can also be obtained somewhat directly, but more simply by measuring the noise spectrum at the output of the diode when it is illuminated with unmodulated light. The circuit of Figure 1 applies to this case if $i(\omega)$ is taken as a noise current generator. If the experiment is performed by chopping the incident light and using a phase sensitive detector, the thermal noise from R_s will not be measured and hence need not be considered. In general $i(\omega)$ will consist of the shot noise of the incident photon stream, as modified by the transit time reduction factor $f(\omega\tau)$, plus contribution due to excess noise generated in the diode. Most of these, such as recombination and flicker noise are negligible, but there may be an additional contribution from collisions within the π-layer. When the collision frequency is much higher than the operating frequency the effect of this mechanism is to add white noise at the output.

Noise Spectra Measurements

The noise spectra of several photodiodes have been measured. Figure 4 shows the frequency dependence of the noise power observed in a *2.3-Mc* bandwidth for a tuned *Riesz*-type diode illuminated with sufficient white light to produce *30 μa* of *dc* photocurrent. The straight line is the theoretical noise power expected in the absence of transit time effects $[f(\omega\tau) = 1]$ when $i(\omega)$ arises solely from full shot noise in the *dc* photocurrent. A measured value of $1/R_sC^2$ was used in establishing the curve. At low frequencies the observed response follows the predicted *6-db*/octave fall-off. At higher frequencies the observed points fall below this curve, the departure being a measure of the transit-time reduction factor. The data are consistent with the predicted cutoff frequency of *20 Gc*.

---

[1] Lucovsky, G., Lasser, M. E., and Emmons, R. B., "Coherent Light Detection Utilizing Solid State Photodiodes," *Electrochemical Society Spring Meeting, Electronics Div Abstracts*, p. 284-5; May, 1962.

[2] Inaba, H., and Siegman, A. E., "Microwave Photomixing of Optical Maser Outputs With a PIN-Junction Photodiode," *Proc. IRE*, p. 1823-4; August, 1962.

[3] Kibler, L. U., "A High-Speed Point Contact Photodiode," *Proc. IRE*, p. 1834-5; August, 1962.

[4] Riesz, R. P., "High-Speed Semiconductor Photodidodes," *Rev. Sci. Instr.*, p. 994-8; September, 1962.

[5] Gaertner, W. W., "Depletion-Layer Photoeffects in Semiconductors," *Phys. Rev.*, p. 84-7; October 1, 1959.

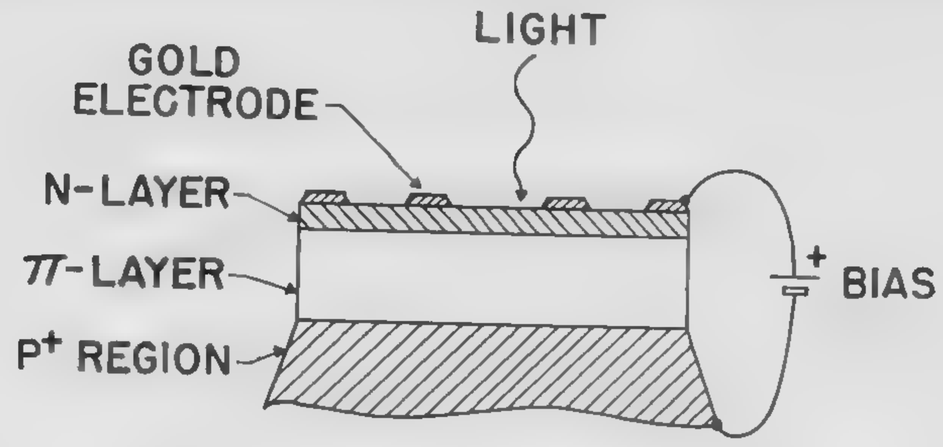


FIGURE 1—Schematic cross-section of a surface junction *PIN* photodiode.

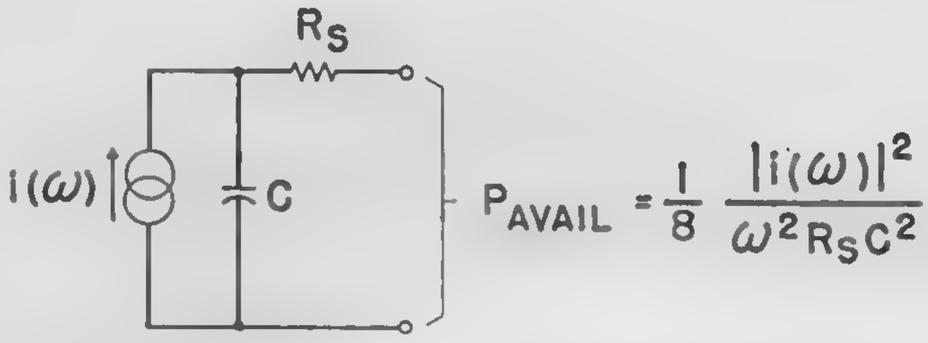


FIGURE 2—High frequency equivalent circuit for a reverse-biased photodiode.

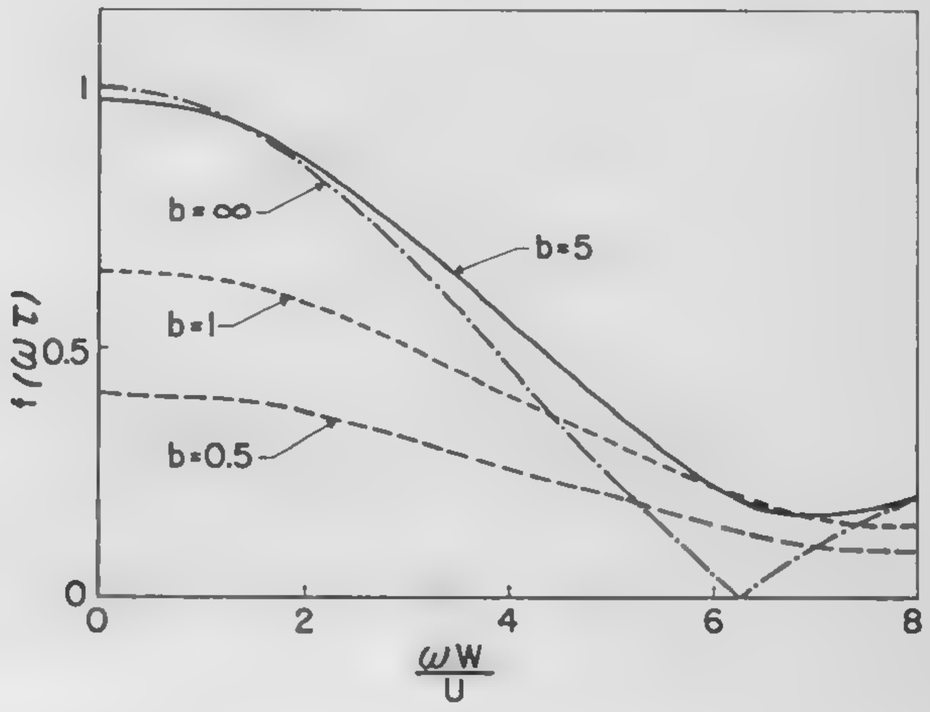


FIGURE 3—Transit time reduction factor as a function of the transit angle $\omega W/u$. The parameter b measures the depth of penetration of radiation into the junction.

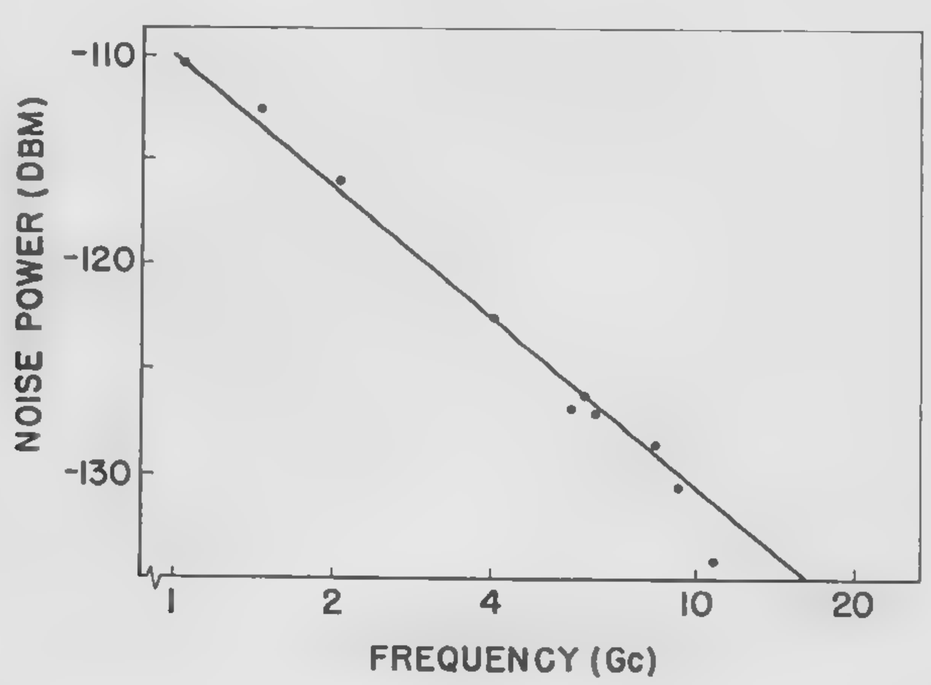


FIGURE 4—Frequency dependence of the shot-noise power output of a conjugate matched photodiode.

SESSION XII: Optoelectronics

FPM 12.5: Switching Light with Light: Absorption Edge Modulation*

R. V. Bez

Sylvania Electric Products Inc.

Needham Heights, Mass.

As THE SPEED of operation of electronic digital computers increases, new problems arise such as radiation losses, mutual coupling, echoes or resonances due to line mismatch, and clock-phasing errors. Many mathematical problem solutions can be resolved by parallel or matrix methods. These factors have engendered consideration of a computer design based upon operational optics using light, rather than wires and electrons.

An optical computer component may utilize present methods such as electrical, magnetic, pressure acoustic or temperature sensitive glass, liquid or crystals. However, the electrical or mechanical interface wiring and driving circuitry is still complex. An idealized computer would use the energy from one optical image to perform a convolution with other optical images. To this end, there is a need for an element which will have its transmittance of one optical signal variable as a function of a second optical signal.

Semiconductors offer selective optical absorption by one or more of four processes:

(1)—Excitation of electrons from the valence band, across the *forbidden gap*, to the conduction band.
(2)—Absorption by free carriers.
(3)—Transitions within the gap due to energy levels resulting from impurities or defects.
(4)—Excitation of the lattice.

The last process is in the far infrared. The lattice is also excited by *Brownian* (thermal) and acoustical sources. The second process may have a *smeared* energy level or may be quantitized by magnetic field spin splitting. The first process should lie in the visible region for many pure materials and provide a short wavelength cutoff. The third process leads to many effects, such as multiple absorption and response peaks, multiple time constants due to trapping and multiple pumping of electrons into the conduction band. These intermediate levels also allow a carrier to decay to the ground state either by emitting at long wavelengths or *without* emitting radiation. This last process is possible because the energy associated with a jump may be as small as the magnitude of the lattice energy and so appear as heat in the material.

Incident photons release electron-hole pairs from the ground (or intermediate states) to the conduction band. If a field is present and an electrical circuit completed, the electrons will flow through the circuit. If no return circuit is present, the electrons and holes will recombine or become trapped by several mechanisms. In germanium the hole mobility is less than that of the electron, thus leading to the problem of *hole storage* time. The lifetime is *30 μsec* in *p-type* Ge and *60 μsec* in *n-type* Ge. For silicon the values are *90 μsec* for *p-type* and *240 μsec* for *n-type*. These lifetimes may be effectively shortened by using a thin sample, so that diffusion will rapidly bring the charges to surface recombination centers or to electrodes. Present-day diodes have switching speeds of less than 10^{-9} sec.

In table I appears a list of a few semiconductors and data on refractive index, optical band gap energy, electron mobility, hole mobility, and absorption edge at two temperatures. It will be noted that increasing temperature shifts the absorption edge to lower energies. This may be explained as an increase in the energy of the ground state, thus narrowing the effective forbidden band gap. This thermal excitation is statistical; thus it smears the valence band edge and destroys *sharp* cutoff. The presence of impurities, having levels near the band edges will also destroy the sharpness of the cutoff.

A parameter called *low effective electron mass* is the result of a broad *smeared* conduction band. This broad band is caused by overlapping energy levels of the lattice and is typical of metals. Metal-like semiconductors may also have a very large electron mobility and so be useful for high-frequency operation. Another viewpoint is that if the electrons have a wide range of energy wave (or state) probabilities, they also have a low effective mass. When the atomic lattice spacing constant is small compared to the effective atomic radii, interactions occur over greater ranges than just *nearest neighbors* and so lead to low effective electron mass. Thus, varying the lattice spacing by piezo, temperature, or pressure effects will also modulate the absorption edge.

A listing of materials which have low effective electron mass, high mobility for fast switching, and are practical because of physical characteristics and available purities appears in table II. The absorption edge of indium antimonide shows a shift from *.17 ev* to *.3 ev* as the electron concentration varies from 10^{17} to 2×10^{18} per cm^3; page 447 of reference *1*. This electron concentration may be achieved by direct current injection through contacts or by subjecting the sample to intense illumination. As the quantum efficiency is high, the number of photons required is not much greater than the number of electrons liberated from the ground state.

A future semiconductor may normally be opaque to red light and be switched to transparent by green light. The red photons will not change the electron concentration, but the green light will.

---

* This work was partially accomplished while the author was with Raytheon and American Optical.

Hannay, N. B., "Infrared Absorption of Semiconductors," Semiconductors, *Reinhold Pub. Co.*, p. 447; 1959.

Dixon, J., and Ellis, J., "Optical Properties of n-Type Indium Arsenide in the Fundamental Absorption Edge Region," *Physical Review*, p. 1560-1566; Sept. 1, 1961.

Brooks, H., "Electrical Properties of Germanium and Silicon" Advances in Electronics and Electron Physics, vol. III, *Academic Press Inc.*, p. 165; 1955.

"IRE Standards on Measurements of Minority Carrier Lifetime" *Proc. IRE*, p. 1293-1299; Aug., 1961.

Shockley, W., "Electrons, Holes and Traps," *Proc. IRE*, p. 973-990; June, 1958.

Papers on "Photoconductors," *Proc. IRE*, p. 1819-1869; Dec., 1955.

Winogradoff, N. N., "Photoconductivity of CdS-Type Photoconductors in the Vicinity of the Absorption Edge," *Journal of Applied Physics*, p. 506-509; March, 1961.

Fan, H. Y., "Infrared Absorption in Semiconductors," *Reports on Progress in Physics*, The Physical Society (London), Vol. XIX, p. 107-155; 1956.

Halpern, A., and Pinker, R., "Color Centers in ZnS Single Crystals," *The Journal of Chemical Physics*, p. 2031-2034; June, 1961.

"Advances in Semiconductor Science," *Proc. of Third Int'l. Conf. on Semiconductors*, Pergamon Press, p. 264-285 and p. 382-421; Aug., 1959.

Wooley, J. C., and Evans, J. A., "Temperature Variation of Optical Energy Gap for GaSb—In Sb Alloys," *Proc. Phys. Soc. London*, p. 354-360; Sept. 1, 1960.

	n	*300° K Gap (ev)*	*(e) mobility*	*h) mobility*	*Absorption 1000/cm*	
					300° K	*77° K*
B		1.0	.9			
C (diamond)		5.6	1800	1200	5.3	5.5
Ge	4.0	.65	4000	2000	.68	.8
Se (amp)				.005	.15	.18
Se (hex)		1.79				
Si	3.44	1.08	1200	500	1.5	1.85
Sn (grey)		.08				
Te	5-6.3	2.13				
AlSb	3.18	1.6	300	300	1.8	
AlP		3.0				
AlAs		2.16		200		
As_2Te_3		1.0	170	80		
AgCl			200		4.5	
AuCs					2.45	
Bi_2Se_3		.35	600			
Bi_2Te_3		.2	200	100		
CdO					2.19	
Cd_3As_2		.6				
CdTe		1.5	600	50		
CdS	2.32	2.5			2.43	
Ca_2Sn		.9				
Ca_2Pb		.46				
CuO		2.3				
$CnInSe_2$		.9	1000			
GaAs	3.34	1.35	5000	400	1.5	
GaP	2.97	2.23			2.3	
GaSb	3.75	.67	4000	850	.7	
GaTe			20			
HgO	2.5					
HgS	2.7					
InP	3.3	1.34	3400	50	1.4	
InAs	3.42	.35	23,000	240	.35	
InSb	3.98	.16	60,000	10,000	.17	
KI					5.5	
Mg_2Ge		.74	530	110		
Mg_2Si		.77	370	65		
Mg_2Sn		.26	300	200		
Mg_3Sb_2		.8				
PbS	4	.4	600	250	.4	
PbSe		.25	1200	900	.29	
PbTe		.31	1200	500	.32	
RbI					5.5	
SiC		2.8	100			
Sb_2Se_3		1.2	15	45		
Sb_2Te_3		.3		270		
TlCl						
ZnO	2.01	3.2	200		3.3	
ZnS	2.28	3.8				
$ZnSb_2$		.55				
ZnSe	2.7					
ZnTe	3.0				2.15	
Anthracene			.02		3.1	

TABLE I

	n	*Lattice Constant A°*	*Effective Electron Mass*	*Energy Gaps 300° K ev*	*microns*	*0° K ev*	*microns*	*Mobility Electrons cm/v/sec*	*Mobility Holes cm/v/sec*
In Sb	3.98	2.8	.015	.17	7.35	.25	5.0	60,000	10,000
In As	3.42	2.62	.03	.33	3.79	.45	2.78	23,000	240
Ga As	3.34	2.44	.08	1.45	.863	1.53	.817	6,000	300
Ge	4.0	2.44	.14	.65	1.925	.75	1.67	4,000	2,000
Si	3.44		.18	1.08	1.16	1.14	1.09	1,200	500
In P	3.3	2.54	.2	1.25	1.0	1.34	.935	3,400	50
Ga Sb	3.74		.2	.67	1.87	.80	1.57	4,000	800
Al Sb	3.18	2.66	1.0	1.6	.78	1.7	.735	500	500
Ga P	2.97			2.24	.558	2.4	.521		
Al P		2.36		3.0	.416				

TABLE II—Potential semiconductor light switches

High-Frequency Limitations of Solid-State Devices and Circuits

[Continued from page 18]

above and semiconductor below. The following characteristics appear possible:

(a) Junction diameter	— *.002 cm*
(b) Base semiconductor resistivity	— *.001 ohm-cm*
(c) Maximum doping at edges of active layer	— $\sim 1.7 \times 10^{16}$/cc
(d) Active layer thickness	— 2×10^{-4} *cm*
(e) Wafer thickness > skin depth	
(f) Wafer diameter	— *1 mm*
(g) Computed breakdown voltage	— $\sim$ *13 v*
(h) Minimum junction cap	— *.022 pf*
(i) Spreading resistance	— *.25 ohm*
(j) Semiconductor skin resistance	— *10 Gc- .4 ohm* *100 Gc-1.2 ohm*
(k) Metallic skin resistance, *guess*	— *10 Gc- .5 ohm* — *100 Gc-1.5 ohm*
(l) Computed *Q* max	— *10 Gc-60* — *100 Gc-2.5*
(m) CW power dissipation for *50°C* rise with all heat passed through silicon	— *170 mw*
(n) Probable power output as doubler *10-20 Gc*	— *200 mw*
(o) Probable efficiency	— *50-70%*

With such a low capacitance varactor many small dots in parallel, using the pepper shaker concept of Figure 2, are feasible, giving a potential power capacity of several watts if such a diode can be built successfully.

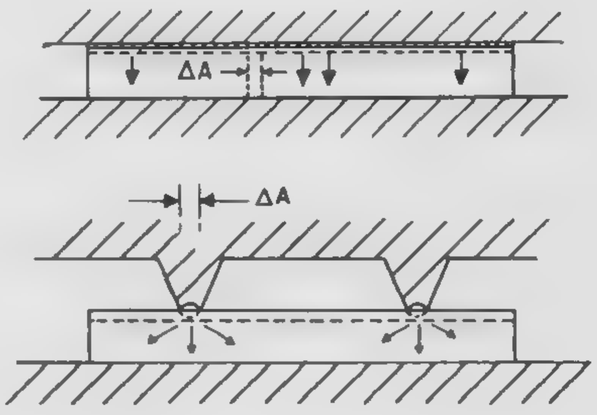


***FIGURE 5*—In the large junction, heat and current from each differential area must, at least, pass through a narrow column as shown above. In a small junction, heat and electrical resistance is reduced by a spreading effect.**

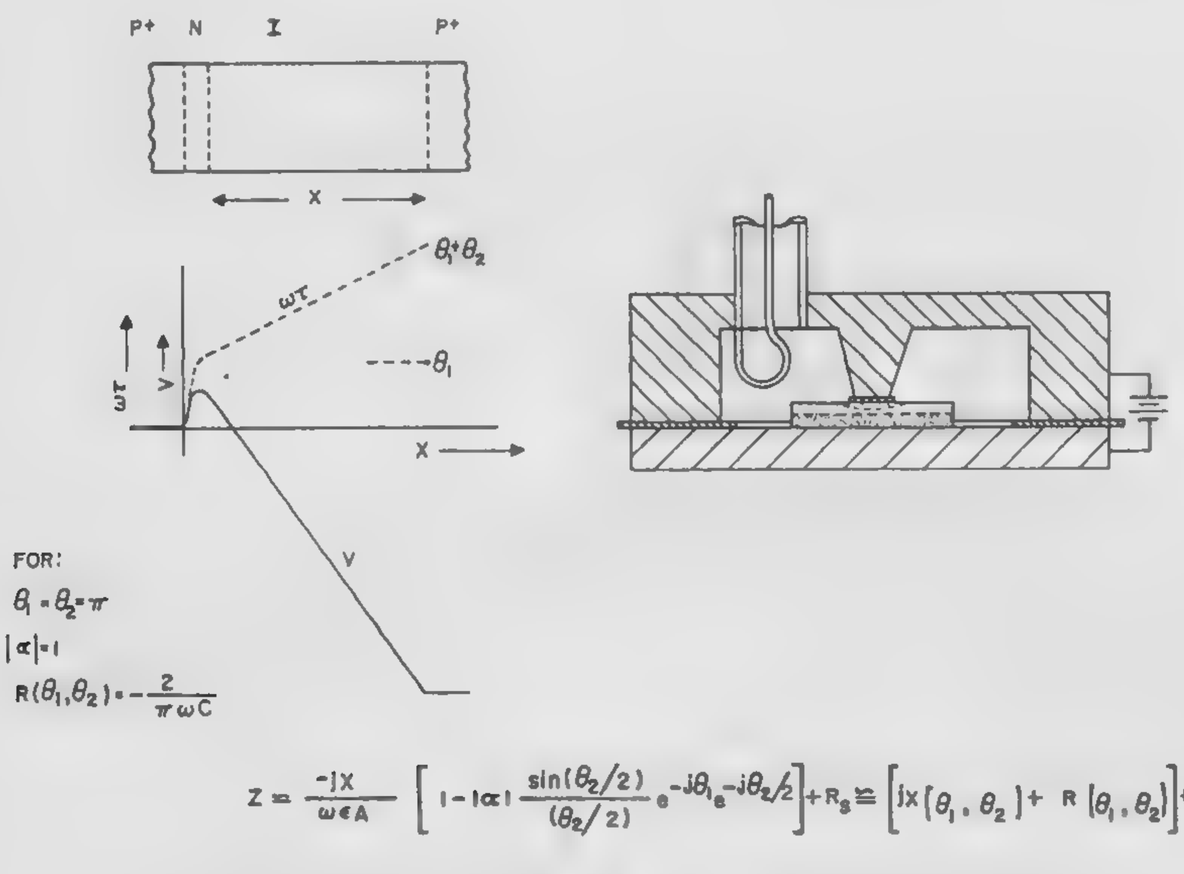


***FIGURE 6*—Principle of transit-time multi-layer diode. Current wave is delayed in passing through the base layer. At high frequencies, this current wave can provide a negative resistance in passing through the intrinsic zone.**

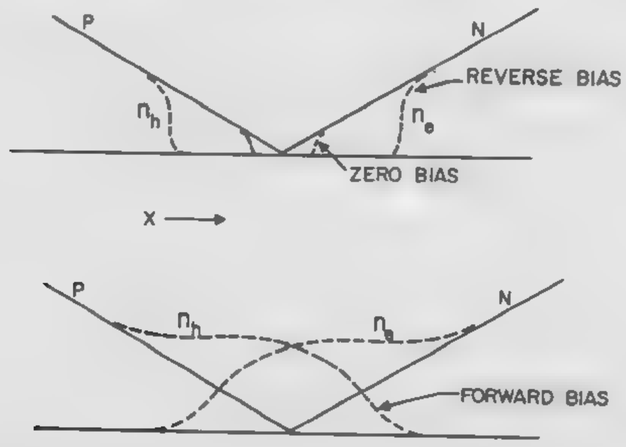


***FIGURE 7*—Illustrating the mechanism for large capacitive charge storage in a diffused varactor when driven strongly at high frequency such that forward bias occurs during a fraction of the cycle.**

Are Transistors Approaching Their Maximum Capabilities?

[Continued from page 21]

factors which limit transistor performance have been considered; speed, power output, low power operation, and noise. The conclusions, with respect to speed, are first that we are approaching the limit on the *(power gain)*$^{1/2}$*-bandwidth* product and can expect to see further increases of no more than an order of magnitude. Secondly, storage time is rapidly becoming a negligible portion of the total switching time in saturating switching circuits.

Advancement Prospects

For high-power operation, we expect to see further advances in power-handling ability at both low and high frequencies, although at high frequencies the power density will not increase by more than a factor of *two* or *three*.

For low power operation, vast improvements have been made in recent years, and one can indeed talk in terms of picowatt operation, albeit only at very low frequencies. Much improvement is possible and expected at high frequencies. The present state of the art is no closer than *three* to *four orders* of magnitude to the ultimate limits.

Small improvements in the low-frequency noise performance due to further reduction of $1/f$ noise can be expected. At high frequencies, noise improvement will result only from improvements in the high-frequency performance characteristics of transistors.

$$G^{1/2} \cdot B = f_{max} = \left[\frac{f_T}{8\pi r_b' C_c}\right]^{1/2} = \frac{1}{4\pi}\left[\frac{1}{r_T r_c}\right]^{1/2} \qquad (1.1)$$

$$\tau_T = \frac{kTC_{Te}}{qI_e} + \frac{w^2}{nD} + \frac{x_c}{2v_{sl}} + \left[\frac{kT}{qI_e} + r_c'\right] C_c \qquad (1.2)$$

$$\tau_c = r_b C_c = R_s \frac{2s^2\epsilon}{3x_c} \qquad (1.3)$$

$$G^{1/2} \cdot B = f_{max} \approx \frac{(9 \pm 3) \times 10^6}{s} \qquad (1.4)$$

$$P \cdot B = \frac{I_i^2}{2\pi C_c} = \frac{I_o^2 \,|\, h_{fb} \,|^2}{16\pi C_c} \qquad (2.1)$$

$$P \cdot R \cdot \omega_{max}^2 = K^2 = \left[\frac{Q_B V_{sl}}{\epsilon}\right]^2 \qquad (2.2)$$

$$t_{sw} = G\left[\frac{\epsilon \Delta V_e}{x_e J} + \frac{w^2}{nD} + \frac{x_c}{2v_{sl}} + \frac{\epsilon \Delta V_c}{x_c J}\right] \qquad (3.1)$$

$$t_{sw} = G\left[\sqrt{\frac{2\epsilon \Delta V_e}{v_{sl} J}}\right] = G\left[\frac{4 \times 10^{-10}}{\sqrt{J}}\right] \qquad (3.2)$$

Series of expressions referred to in comments on speed, and high- and low-power potential of transistors.

Low-Noise Reciprocal Parametric Amplifier With Power Matching at Input-Output

[Continued from page 52]

tuned to b to achieve maximum pump modulation of the diodes. By means of the conductance g'_{ct} the values of a and $\vec{G}_t$ can be adjusted.

Capacitive Admittance

Due to the capacitor C_N, the admittance of the idler circuit at frequency Ω_I is capacitive, thus producing the effect of the feedback admittance Y.

Test Setup Performance

The test setup was operated at $f_a = \frac{\Omega_I}{2\pi} = 200\ Mc$ and $f_b = \frac{b}{2\pi} = 940\ Mc$.

(1)—Amplifier operation ($a = 0.5$)

Characteristics of the amplifier are shown in Figures 4-7. Theory yields $\vec{G}_t = 9.5\ db$, $\overleftarrow{G}_t = 0$ and $NF = 2.15\ db$ at resonance.

(2)—Isolator operation ($a = 0$)

At resonance the values $\vec{G}_t = -1\ db$ with total bandwidth $B_{total} = 17\ Mc$, $\overleftarrow{G}_t = -30\ db$, standing-wave-ratio $m_{in} = m_{out} = 1.5$ and $NF = 1.14\ db$ were obtained; theory yields $\vec{G}_t = 0\ db$, $\overleftarrow{G}_t = 0$ and $NF = 0\ db$ ($F_{ex} = 0$).

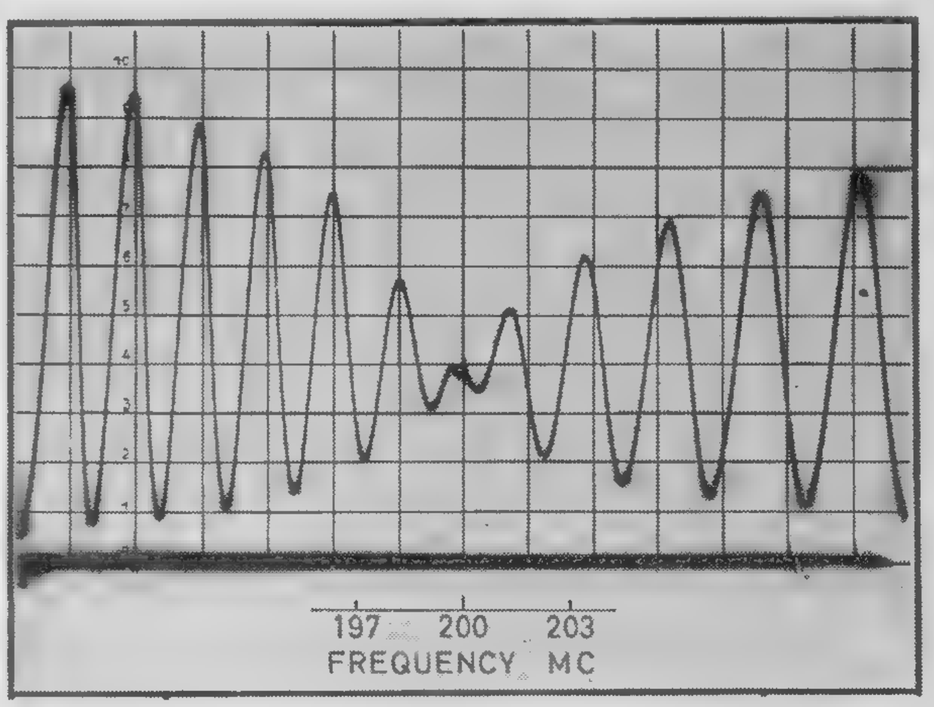


FIGURE 7—Output standing-wave-ratio m_{out} versus frequency ($a = 0.5$). $m_{out} = 2$ at $\frac{\Omega_I}{2\pi} = 200\ Mc$.

Large Signal Models for Junction Transistors

[Continued from page 56]

problem may be solved by the use of superposition. Individual solutions are obtained for operation in the forward and inverse active regions with appropriate boundary conditions; these solutions are superimposed to obtain the total solution. Thus the total emitter current and collector current are each given by a first-order differential equation containing both Q_{BR} and Q_{BF}. The characteristic equation for the saturation region is therefore of second order. Of the two natural frequencies, one is generally dominant for most practical applications. Storage time is found by solving for $Q_{BR}(t)$, setting it equal to zero, and solving for time.

The Lumped Model

The lumped model differs from the others in that the continuity equation never need be written as a partial differential equation. Rather, the space variable is removed at the outset by writing finite difference equations for the base region. A number of division points, having arbitrary spacing, are selected within the base region. At each point difference equations are written for diffusion currents, and continuity is expressed in difference equation form. Defined are lumped elements which are analogous to conductance and capacitance, but which have terminal variables density and current; each division point thus serves as a node to which the appropriate lumped elements are connected. The resulting *network* provides a means of making detailed calculations, while providing *1:1* correspondence with the physical processes in the base region. To obtain electron current, the space-charge neutrality requirement is invoked.

In forming the single-π-section model, one selects four points in the base region: one at each boundary and two interior points. The lumped model is formed and the interior points are forced to approach the boundaries, where the densities are determined by the law of the junction; a single-π-section model results.

It is to be emphasized that this is the same difference approach which is applied to transmission lines to obtain π or T section approximations composed of lumped R, L, and C elements. The less-familiar elements diffusance (H_d), combinance (H_c) and storance (S) are obtained for the base region, because the linearly-related variables are density and current rather than voltage and current.

The solution of transient problems is straightforward: nodal equations are written for densities and currents in the base region; boundary densities and junction voltages are related by the law of the junction. The explicit superposition of active region conditions for the saturation region is not necessary; problems may be solved directly.

Comparison of Models

From the engineer's point of view, the ideal model is one which provides a clear, precise, and tractable representation of the device performance in terms of the physical processes; thus lending itself well both to analysis and to physical reasoning and qualitative understanding. In assessing the degree in which the models approach the ideal, we shall compare them as analytical tools, and as means for representing physical processes.

As analytical tools, the *Ebers-Moll*, charge-control, and single-π-section lumped models are equivalent in the sense that all have similar describing equations, the same natural frequencies, and yield the same solutions to transient problems. The *Ebers-Moll* model is a well-established, useful tool for first order solutions, and it, as well as the lumped model, can be extended to include the non-linear behavior of the junction; this is not conveniently done with the charge-control model. Higher-order solutions are most easily obtained with the lumped model, which lends itself to a sequence of solutions of increasing accuracy as more division points are used. The generation of higher-order lumped models is straightforward; one selects the desired number of division points and obtains the model parameters by the well-defined difference equation procedure. In contrast to the charge-control model, the symbolic elements of the lumped model provide a means of applying all of network theory to the analysis of the device; thus the lumped model provides an extremely powerful analysis tool. For example, one can obtain the form of the model from the difference equation procedure and select the element *values* by network synthesis procedures.

With regard to the representation of physical processes, only the lumped model provides a *1:1* correspondence between the elements of the model and the physical processes. The charge-control model provides limited contact with processes, while the *Ebers-Moll* model is the most remote from them. Again in contrast to the charge-control model, the lumped elements not only provide a *1:1* correspondence with processes; but each lumped element has an explicitly defined relationship between its terminal variables.

By well-defined procedures, the lumped model may be extended to include the effects of drift fields and space charge within the base region; at all times *1:1* correspondence between elements and processes is maintained, and in all cases explicit analytical expressions for terminal variables are obtained.

Of the three models described, the lumped model provides the closest approximation of the ideal model.

Some Aspects of Digital Circuit Design

[Continued from page 58]

emitter current I_1. We begin by plotting the combined *V-I* characteristic of the emitter-base diode of the grounded-base transistor and the emitter source. This is labeled I_R-I_2. The parallel-diode characteristics define the limits of the emitter-base voltage. The characteristic of the input transistor (with its spread) is also plotted, and the intersection of the two characteristics will give the emitter current I_1. It can be seen that all intersections must lie within the area bounded by the four characteristics which are shown. If we assume that all diode characteristics are parallel and uniformly distributed, then the probability density between two slightly different emitter currents is proportional to the distance between the boundaries, multiplied by the current difference. These distances are plotted (for example the distance X shown) to give a distribution which may be normalized to obtain the probability density function. This density function may be combined with others (a task sometimes easier said than done) to obtain a distribution of output voltage.

Transient Performance Factors

After a *dc* design is obtained, the problem is, of course, only partially solved. Equally important is the specification of those device parameters which affect transient performance. For this purpose, a model is devised from which one hopes to predict the transient performance of the circuit. A great deal of interest has been generated recently in the charge parameter model. It has been found, however, that the piecewise linear model based on small-signal parameters works well. When the transistor is driven by a low-impedance source, the charge parameter model loses most of its advantages, and the choice of models becomes virtually a toss-up. A very complete small-signal equivalent circuit is shown in Figure 6; the parameters are:

α_o = *dc* current gain

$$\omega_{\alpha i} = \frac{1}{T_e} = \text{intrinsic cutoff frequency}$$

$$T_e = \frac{1}{C_d r_e} = \text{transit time}$$

m = excess phase shift factor
C_D = emitter-base diode diffusion capacitance
r_e = incremental emitter-base diode resistance
C_{et} = emitter-base junction capacitance
$r_{bb'}$ = base-spreading resistance
C_{et} = collector-base junction capacitance
r_s = incremental resistance of the collector-base diode during saturation
C_s = collector base diode diffusion capacitance during saturation
R_{CC}, R_{EE} = bulk resistance
L_B, L_C, L_E = external lead inductances
C_{cb} = external collector-base capacitance due to header, etc.

Summarizing, there are certain techniques that the circuit designer may use to simplify his work. In the main, however, successful circuit design is a matter of experience, and trial and error.

Solid-State Sensors for Process Control

[Continued from page 60]

wider temperature range. Results of an investigation of single crystal SiC demonstrated the feasibility of *PTC* resistors with characteristics similar to the silicon devices, but with an operating range up to at least *900° C*, with intermittent operation observed up to *1200° C*. The limitation does not seem to be with the SiC material, but is rather a problem of suitable contact materials. This operation was achieved in an oxidizing atmosphere. The setup used to perform some of the measurements is shown in Figure 1. Curves of resistance versus temperature for different samples are shown in Figure 2. A closeup of one of the sensors, operating in the flame of a propane torch, is shown in Figure 3.

There has been considerable interest in high output thermocouples useful over extremely wide temperature ranges. SiC-graphite, and carbon-boronated carbon are two such thermoelements with *Seebeck* coefficients up to 300 $\mu v/°$ *C* and temperature range up to *2500°C*[4].

Exotic metals have been used to make extremely small, and thus very fast, thermocouples capable of covering a temperature range up to *2500° C*. Few of these have yet made their way into industrial use; moreover they exhibit very low sensitivity and a rather unstable nature[7].

Silicon Strain-Gage Elements

The first commercial silicon strain-gage elements were offered to the public a little over 2 years ago, but already these amazing piezoresistive sensors are well established in the instrumentation field[1]. The tiny, rugged filaments have been incorporated in pressure gages, accelerometers, velocity sensors, etc. Here is a device with dynamic characteristics equal to those of piezoelectric sensors, and equally sensitive to steady pressures. Moreover, the sensitivity is *50* to *100* times greater than for metallic gages. They exhibit virtually no hysteresis or zero level drift, and excellent resistance to vibration and shock. To avoid some of the temperature limitations on silicon devices, a brief investigation was conducted on silicon-carbide strain gages. Filaments cut from random samples gave results shown in Figure 4. Gage factors of initial devices were around *30;* no attempt was made to prepare materials for optimum performance. It is hoped that SiC strain gages may provide an answer to pressure sensing in high temperature and corrosive atmospheres.

Piezoelectric sensors are becoming increasingly temperature independent and able to withstand much higher temperatures due to improvements in ferroelectric ceramics. The wide dynamic range, high output, and force range of the devices account for their popularity. Their use in process control is limited due mainly to the lack of *dc* response.

Intermetallic Resins

Recent developments promise almost revolutionary changes in the field of strain-gage instrumentation. Intermetallic resins have been used to make piezoresistive pressure cells in which the output varied by as much as *300,000:1* over the range of the devices[3]. These devices were made sensitive enough to detect a *.001-gm* pressure variation, with ranges all the way up to *250,000* pounds sq. in. The frequency range extended from *dc* to *3000 cps*. These sensors have already been made insensitive to temperature variations up to *300° F*. The simplicity of these devices, their ruggedness, and flexibility certainly warrant further study of the potential of rare earths for sensor applications.

Piezojunction Devices

Piezojunction devices are of more recent vintage. Two types have been described in the literature. A tunnel diode strain gage with gage factors in the vicinity of *30,000* has been demonstrated*. Of similar nature is the piezojunction transistor, which is somewhat more stable a device and achieves high sensitivity by virtue of its inherent gain. Piezojunction transistors possess a frequency range from *dc* to *100 kc*[5,6].

In the measurement of flow, few promising new techniques appear to be in sight. The only solid-state techniques employed at the moment are indirect ones. In the thermal method, capable of $\pm 2\%$ accuracy, two thermistors monitor the flow of heat introduced locally by an *rf* generator or a hot-wire method. Sonic techniques measure the transit time of a sound pulse between two piezoelectric transducers acting alternately as transmitter and receiver. Better than *2%* accuracy and higher response speed than with the thermal method are achieved with this rather elaborate measuring technique.

The use of solid-state phenomena in binary-state indicators is not particularly widespread. An exception is the photocell or photoconductive sensor. Many other phenomena, such as the sharp *Curie* transitions in ferroelectric and ferromagnetic materials may find similar applications for thermal limit indication.

System Considerations

Earlier, it was stated that for lack of digital devices, a common language such as frequency would rank next in desirability. The possibility of digital sensors is quite remote at the present. However, there are two efforts in that direction. One makes use of a large number of $BaTiO_3$ samples, each doped to a different *Curie* temperature, to create an array which, with the use of suitable circuitry, gives a digital output at *1°* intervals from *0* to *120° C*. Another makes use of the photoelastic effect in certain optically-transparent materials. A number of such materials with cross-sectional areas related at 1:2:4:8:16 are stacked up; light is focused through each plate on separate detectors. A binary-coded output is achieved with the use of additional circuitry. Resolution of *1* part in *1000* is claimed for this device.

Resistive Solid-State Sensors

One approach is based on the availability of an entire family of resistive solid-state sensors. The dual-input, twin-*T* oscillator, illustrated in Figure 5, is characterized by a relative null frequency which is proportional to the square root of the ratio of its two inputs. This system utilizes one sensor and a dummy as a remote portion of a bridge arrangement. A bridge unbalance, produced by the sensor environment, causes the null network to shift oscillator frequency. Thus the output frequency becomes a function of sensor environment. Resolution better than *0.1%* was achieved using a *10-kc* center frequency with several sensors remotely connected by twisted pairs. It is felt that further thought is necessary to make the sensor a more integral part of a control system.

---

* Bell Telephone Laboratories, Inc.

[1] Geyling, F. T., and Forst, J. J., "Semiconductor Strain Transducers," *BSTJ*, p. 705; May, 1960.

[2] Lion, S., "Instrumentation in Scientific Research," *McGraw-Hill;* 1959.

[3] Ludewig, Jr., F. A., "Digital Transducer: Force Input . . . Binary Output" *Control Engineering*, p. 107-109; June, 1961.

[4] Nadler, M. R., and Kempter, C. P., "Thermocouples for Use in Carbon Atmospheres," *Rev. Sci. Inst.*, p. 43; Jan., 1961.

[5] Rindner, W., and Nelson, R., "Piezo-Junctions: Elements of a New Class of Semiconductor Devices," *Proc. IRE*, p. 2106; Oct., 1962.

[6] Rindner, W., and Nelson, R., "A New p-n Junction Strain Transducer" *WESCON*, Paper 3.4; 1962.

[7] Walker, B. E., Ewing, C. T., and Miller, R. R., "Thermoelectric Instability of Some Noble Metal Thermocouples at High Temperatures," *RSI*, p. 1029-1040; Oct., 1962.

Considerations Underlying the Study of Sensory Elements

[Continued from page 63]

must be discharged before another large influx can occur. Now all of these conductances lie distributed along a membrane that has a large capacitance, about *1 μf/cm²*. In the case of a purely tubular structure, such as a nerve fiber, this can be simplified to a ladder network, the inner and outer fluids forming resistive lines between which the capacitance of the membrane is distributed. Across the distributed capacitance lie the distributed conductances with their particular current-voltage relations. Thus, for non-regenerative fluctuations there will be a transmission line spread along the fiber showing an exponential decay spatially and temporally, and one can define a space (phase) constant and a time constant for small steps of current inserted at one end.

Membrane Potential

But consider what happens if you drive current more strongly between the inside and outside of this fiber. The membrane potential is driven more postive than its *−80 mv*. If it is driven into the neighborhood of *−60 mv*, the Na^+ conductance becomes greater than the K^+ conductance. Na^+ flowing in drives the inside of the membrane more positive, whereupon the Na^+ conductance increases still further; and the membrane potential regenerates locally up to the Na^+ potential, Na^+ flowing in along its own concentration gradient. But then the Na^+ current is truncated by its *cutoff;* and K^+, now operating through its own increased conductance, pulls the membrane back to the K^+ potential. As Na^+ flows in locally, current flows out in adjacent membrane. This outflow, in turn, biases that membrane to where it shows the regenerative Na^+ flow; and so, a transient, the nerve spike, sweeps down the nerve. Very little of the stored energy is dissipated, although a single spike may give as much as several *ma/cm²* peak current locally.

System Oddities

Our apologies for presenting so oversimplified a picture of nervous action. But it is important to have such an image, if we are to try to understand biological transducers.

It has been shown that not only can the different ions be handled differently across a nerve membrane, but the flux in one direction can be coupled variously to that in the other direction. Many other oddities are apparent; for example, suppose we were to replace much of the external Na^+ with K^+. The membrane potential would be much closer to *0* than *80 mv*. If current is applied so as to bring that potential to *80 mv*, the K^+ conductance would again decrease. As the new resting membrane potential is approached again, the conductance increases—thus giving us a negative resistance for K^+, as well as the one formerly described for Na^+. The *Hodgkin-Huxley* equations are a remarkable description of these voltage-dependent conductances and their interactions, and the exploration of the consequences still continues. Some tissues show conductances that differ markedly from those described by these authors for squid nerve, although they are of the same form. For reference, the vast literature, primarily published in the *Journal of Physiology* for the past 10 years, is recommended.

Transfer Functions

When one sees that conductances can be tailor-made by coupling several tissues to one another in specific ways, one gains some idea of how broad and difficult is the study of any one transducer, or synapse, or transfer function. One might make a tension-sensitive device by stretching nerve so that gaps develop through which the membrane can depolarize. One can make a light-sensitive device by coupling a photochemical to one of the channels, either in pump fashion, or putting one of the bleaching products in competition with an ionic species, etc. One of the major problems is to find how organic, un-ionized molecules can so couple to such a system as to produce signals, as in the sense of smell. *Pitts* and *Gesteland* have a theory about it, but it is too complex and tentative to present at this time.

Generator and Synaptic Currents

In any case, the membrane has the wherewithal to couple to signals external to it; and, by converting them into an electrical change in a self-powered device, it can amplify them and transmit them. What is not obvious is that it can combine signals in an extraordinary fashion as well. Let us consider the receiving end of a nerve fiber and suppose it is critically damped against regeneration. If what we do increases the Na^+ inflow, we provide a current flowing inward at the end, driving the potential in the adjacent membrane more positive, until, if it goes positive enough, a spike is set off, which thereafter propagates. If this current is generated at a receptor, it is called a *generator* current; if it occurs at a *synapse*, it is called *synaptic* current. But let us suppose that between the current-generating end and the place where a spike is generated, we interpose another sensitive point which, on receipt of the proper stimulus, increases only the K^+ conductance. Then much of the current from the excited end is shunted through the lower conductance at membrane potential, and the current is decoupled from the membrane capable of generating a *spike*. This is called *inhibition*, and is one form of it. It is essentially divisive in its function, rather than subtractive in this picture and is best illustrated by *Kuffler's* study of the stretch receptor in the tail of a lobster or crayfish. You can see that very complex interactions between transducers can occur, and the output becomes a nonsimple function of several input variables. These phenomena are best seen in *synaptic* regions, where neurons join to neurons and the transduction of the various inputs to one neuron must be mixed in complex ways.

It is evident that if this sketch is even partly true, the simple nerve fiber, seen this way as a distributed combinatorial system, has a flexibility that is yet to be properly imitated with electronic-circuit analogs.

Synthesis of Electronic Bistable and Monostable Circuits

[Continued from page 70]

acterized by the two stable points and two trigger points in the *I-V* plane. Four-point, *I-V* characteristics for the configuration of Figure *7a* are shown in Figures *7b*, *c* and *d*.

Stable and Quasi-Stable States

Working from a 4-point characteristic, one can remove a stable state of the configuration by the proper insertion of voltage or current sources. For example, in Figure *7b*, a single crossing of the V_{AC} axis can be achieved, and a potentially monostable circuit is obtained when direct or converted devices are substituted for the controlled-*G* models. Continuing to work from the *4*-point characteristic, one can establish where energy storage elements should be introduced and of what type to achieve a quasi-stable state. In Figure *8a*, a monostable circuit, which is generated in the above manner, is shown.

Counting Circuit Example

The energy storage requirements to achieve a quasi-stable state in a monostable circuit are related closely to the problem of memory if a bistable circuit is to have the counting property. Again, the *4*-point, *I-V* characteristic of a potentially bistable configuration is used. The type and location of energy storage in the configuration are easily established, together with proper locations of trigger input. The counting circuit of Figure *8b* is an example.

Signal Processing With Parametric Delay Lines

[Continued from page 88]

$3 \times 3 \times \frac{3}{8} = 3.4$. The reasoning given assumes that mismatch losses can be eliminated.

Figures so far obtained for actual lines are detailed in table I below with measured calculations for the *simpump* and *distripump* lines.

In experimental *simpump* and *distripump* lines, SVC1 diodes were used with FX 1487 ferrite tubes for inductance loading. L per section $= 0.07\ \mu h$. The *distripump* line contained thirty-five sections; simpump line, fifty.

	C_1 / C_2	$\vec{V}_2 / V_1$		T_2 / T_1	
		Measured	Calc.	Measured	Calc.
Simpump	3.3	2.0	2.5	0.6	0.56
Distripump	2.8	2.2	2.24	0.5	0.42
Reverse Distripump	2.31	1.4	1.92	0.8	0.70
Reverse Distripump	0.43	0.6	0.55	1.4	1.36

TABLE I

Gain Characterization of High-Frequency Linear Amplifier Devices

[Continued from page 90]

if we know GF and U. Feedback amplifier performance is known if we know its gain and feedback characteristics.

Maximum Available Gain Expression

Since U and GF characterize the device, the remaining work is simply that of putting them into more usual forms. With some manipulation we can rewrite the relation for *Maximum Available Gain****,

$$G_{max} = \sqrt{GF} \qquad \left[k = \sqrt{k^2 - 1}\right]$$

where $k = \frac{\sqrt{GF}}{2U} + \cos \Phi$, and Φ is the phase of y_{21}/y_{12}.

When $k > 1$ the device is unconditionally stable and G_{max} is realizable. When $k < 1$, no problem results because additional resistive loading can be added to make $k = 1$. Under these conditions, a maximum stable gain is achieved, given by $G_{ms} = \sqrt{GF}$.

The agreement between the analysis and experimental results is indicated in Figure 2, where *Gain Figure* has been plotted as measured under quite different circumstances.

Feedback for Wide-Band Amplifier Use

Typical data for germanium transistors are shown in Figures 4 and 5. In Figure 6, feedback was added to a 2N1195 transistor in an attempt to make U and GF (for the resulting device and feedback circuits) constant over a wide frequency range, thus resulting in a wide band amplifier. And Figure 7 shows a *1-kMc* stripline amplifier used to measure some of the *Gain Figure* data of Figure 3.

The specification of U and GF of a device provides information in a form immediately useful to circuit designers for synthesis, stability, and maximum realizable gain determinations.

Notes

Notes

Recipients of Outstanding Paper Awards

1962 International Solid-State Circuits Conference

R. P. Rafuse, Research Laboratory of Electronics, MIT

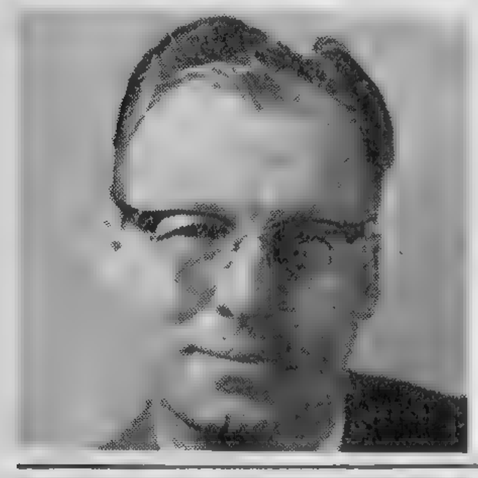
Paper WM 2.2: **High Power Operation of Varactor Devices**

Citation: **A Significant Contribution to the Design of Parametric Circuits**

D. L. White, Bell Telephone Laboratories, Inc.

Paper WA 3.2: **Amplification of Ultrasonic Waves**

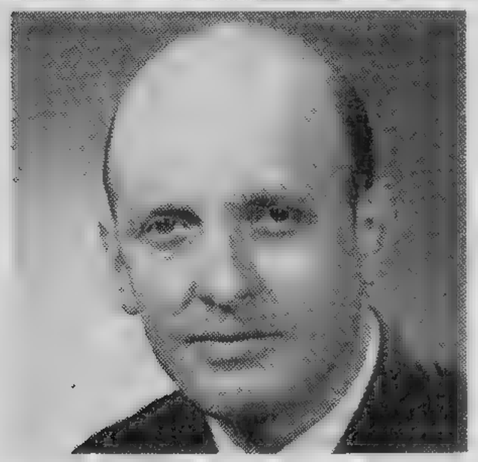
Citation: **An Exciting New Mode of Amplification of Potentially Great Importance**



W. P. Weimer, RCA Laboratories Division, RCA

Paper WA 3.4: **Evaporated Circuits Incorporating a Thin-Film Transistor**

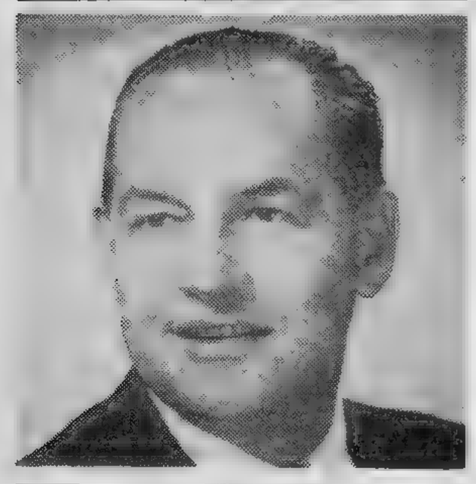
Citation: **A Vital Contribution to a Major Field of Solid-State Technology**



W. E. Proebster, IBM Corporation

Paper WA 4.2: **The Design of a High-Speed Thin-Magnetic-Film Memory**

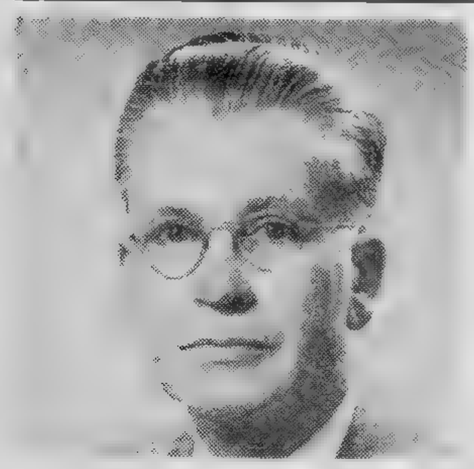
Citation: **A Major Advance in the Technology of Solid-State Memory**



A. F. Dietrich, Bell Telephone Laboratories, Inc.

Paper TA 8.2: **Carrier Pulses at Microwave and Millimeter-Wave Frequencies**

Citation: **An Effective Advance in the Field of Ultra-High Speed Pulse Generation**



W. M. Sharpless, Bell Telephone Laboratories, Inc.

Paper TA 8.2: **Carrier Pulses at Microwave and Millimeter-Wave Frequencies**

Citation: **An Effective Advance in the Field of Ultra-High Speed Pulse Generation**

SCOPE OF THE CONFERENCE

TWELVE DAYTIME SESSIONS, with three devoted to tutorial and invited papers, have been programmed for the 1963 INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE, that will be held in the Irvine Auditorium and University Museum of the University of Pennsylvania.

BROAD ADVANCES in the field of solid-state device applications and circuits will be covered in fifty-three papers. The general subject areas include digital memories, logic, low-frequency circuits, microwave circuits, digital design techniques, linear circuits, integrated circuits and optoelectronics. Invited and tutorial speakers will cover high-frequency generation and amplification, transistor switching circuits, and solid-state sensing.

IN A FORMAL OPENING, in the Irvine Auditorium, a special paper-award presentation ceremony will be held to cite speakers for outstanding 1962 conference efforts.

Additionally, the formal opening will feature a keynote address by James H. Mulligan, Jr., chairman of the electrical engineering department of New York University, who served as chairman of the 1958 Transistor and Solid-State Circuits Conference. He will talk on "The Role of Network Theory in Solid-State Electronics—Present Accomplishments and Future Challenges."

INFORMAL discussions have also been scheduled for the 1963 meeting, and eleven such sessions have been placed on the Wednesday and Thursday evening agenda.

TOPICS include nanosecond switching circuits, integrated linear circuits, statistical and computer techniques in circuit design, magnetic thin-film memories, packaging and the measurements problem, and special circuit design considerations for the nuclear environment. Other subjects on the discussion program are coherent optical techniques and applications, integrated digital logic, broadband amplifiers, combined analog-digital circuit techniques, and partial switching of ferrites.

Conference DIGEST OF TECHNICAL PAPERS

ADDITIONAL COPIES of the DIGEST OF TECHNICAL PAPERS, priced at $5.00 per copy, may be obtained from H. G. Sparks, The Moore School of Electrical Engineering, University of Pennsylvania, 200 South 33 St., Philadelphia 4, Pa. Remittance (payable in U. S. currency) should be made to the order of: Solid-State Circuits Conference.

General Conference and Informal Session Locations

IRVINE AUDITORIUM and University Museum, where all of the daytime meetings will be held, are located on the campus of the University of Pennsylvania.

IRVINE AUDITORIUM is located at the northwest corner of 34th and Spruce Streets; the University Museum is just east of the southeast corner of 34th and Spruce Streets.

THE INFORMAL Wednesday-Thursday evening sessions will be held in the Sheraton Hotel, 1725 Pennsylvania Boulevard, in central Philadelphia.

Daily Luncheons

DAILY LUNCHEONS on Wednesday, Thursday and Friday will be served to a limited number in the University Museum, University of Pennsylvania.

Conference Fees

Registration—	
Member IEEE:	$12.00
Non-Member:	14.00
Wednesday Lunch:	3.50
Thursday Lunch:	3.50
Friday Lunch:	3.50

Full-time students will be registered free-of-charge for all technical sessions.

EXECUTIVE COMMITTEE

Chairman: Franklin H. Blecher, Bell Telephone Laboratories, Inc., North Andover, Mass.

Secretary: Francis J. Witt, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

Treasurer: Robert Mayer, Sun Oil Co., Newton Square, Pa.

Asst. Treasurer: Henry Sparks, The Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, Pa.

Committee Chairmen

Program: Sorab K. Ghandhi, Philco Scientific Laboratory, Blue Bell, Pa.

International Arrangements: Tudor R. Finch, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

Public Relations: Lewis Winner, Consultant, New York, N. Y.

Editorial: Veikko R. Saari, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

Awards: Robert F. Cotellessa, College of Engineering, New York University, New York, N. Y.

Local Arrangements

Chairman: Henry G. Sparks, The Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, Pa.

Vice-Chairman: R. L. Miller, Tele-Dynamics, Inc., Philadelphia, Pa.

Membership:

C. L. Zoi, Bell Telephone Co. of Pa., Philadelphia, Pa.
F. LaVerghetta, Philco Corp., Computer Div., Willow Grove, Pa.
J. Standeven, Philco Corp., Computer Div., Willow Grove, Pa.

Sponsors' Advisory Committee

Chairman: Murlan S. Corrington, RCA, Camden, N. J.

IEEE PTGCT Rep.: Ralph J. Schwarz, Dept. of E.E., Columbia University, N. Y., N. Y.

IEEE ECSC Rep.: Arthur P. Stern, Martin Marietta Corp., Baltimore, Md.

IEEE Phila. Sect. Reps.: Robert Mayer, Sun Oil Co., Newton Square, Pa.
Harry J. Woll, RCA, Camden, N. J.

Univ. of Penna. Rep.: John G. Brainerd, The Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, Pa.

Technical Program Committee

Chairman: S. K. Ghandhi, Philco Scientific Laboratory, Blue Bell, Pa.

Secretary: A. K. Rapp, Philco Scientific Laboratory, Blue Bell, Pa.

Members:

R. L. Bright, Westinghouse Electric Corp., Pittsburgh, Pa.
W. F. Chow, Remington Rand Univac, Blue Bell, Pa.
E. U. Cohler, Sylvania Electric Products, Inc., Needham, Mass.
R. S. Engelbrecht, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
C. A. Franklin, Defense Research Board, Ottawa, Canada
V. Grinich, Fairchild Semiconductor, Palo Alto, Calif.
C. S. Kim, Electronics Lab., Gen. Elec. Co., Syracuse, N. Y.
A. W. Lo., IBM Corp., Poughkeepsie, N. Y.
P. Lombardo, Airborne Instruments Laboratory, Deer Park, L. I., N. Y.
J. T. Lynch, Burroughs Corp., Paoli, Pa.
J. S. Mayo, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
R. E. McMahon, MIT Lincoln Laboratory, Lexington, Mass.
M. McWhorter, Stanford Electronics Laboratory, Stanford, Calif.
M. Melehy, University of Connecticut, Storrs, Conn.
K. E. Mortenson, Microwave Associates, Inc., Burlington, Mass.
P. B. Myers, Martin Marietta Corp., Baltimore, Md.
J. A. Narud, Motorola Semiconductor Products, Inc., Phoenix, Ariz.
R. Purcel, Raytheon Company, Waltham, Mass.
R. P. Rafuse, MIT, Cambridge, Mass.
J. Schmidt, Fairchild Semiconductor, Palo Alto, Calif.
A. C. Scott, University of Wisconsin, Madison, Wis.
S. Shamis, New York University, N. Y., N. Y.
A. E. Slade, Arthur D. Little, Inc., Cambridge, Mass.
T. O. Stanley, RCA Laboratories, Princeton, N. J.
P. M. Thompson, Plessey Co., Ltd., Romsey, Hampshire, England
R. R. Wesbter, Texas Instruments, Inc., Dallas, Tex.
E. P. Stabler, Electronics Lab., Gen. Elec. Co., Syracuse, N. Y.

ISSCC 63 SCHEDULE OF REGISTRATION HOURS, LUNCHEONS AND SESSIONS

		UNIVERSITY OF PENNSYLVANIA			SHERATON HOTEL						
		Houston Hall	Irvine Auditorium	University Museum	Upper Lobby	W. Ballroom	E. Ballroom - Assembly	Penn.- West	Penn.- East	Ind.- Const.	Delaware Valley
TUES., FEB. 19	4:00-8:00 P.M.	.....	.....	.....	Registration	.....	.....	.....	.....	.....	.....
WED., FEB. 20	8:00-11:00 A.M.	Registration	.....	.....	.....	.....	.....	.....	.....	.....	.....
	11:00 A.M.-4:00 P.M.	.....	Registration	.....	.....	.....	.....	.....	.....	.....	.....
	9:00-11:45 A.M.	.....	SESSION I Digital Memories	SESSION II [Tutorial] Freq.-Pwr. Limitations of Solid-State Devices	.....	.....	.....	.....	.....	.....	.....
	12:00-1:15 P.M.	.....	.....	LUNCH	.....	.....	.....	.....	.....	.....	.....
	1:45-2:45 P.M.	.....	FORMAL OPENING	.....	.....	.....	.....	.....	.....	.....	.....
	2:50-5:30 P.M.	.....	SESSION III Logic I	.....	.....	.....	.....	.....	.....	.....	.....
	3:00-5:30 P.M.	.....	.....	SESSION IV Low-Freq. Circuits	.....	.....	.....	.....	.....	.....	.....
	8:00 P.M.	.....	.....	.....	.....	INFORMAL DISCUSSIONS					
						WE 1 Integrated Linear Circuits	WE 2 Nanosecond Switching Circuits	WE 3 Magnetic Thin-Film Memories	WE 4 Statistical and Computer Techniques in Circuit Design	WE 5 Packaging and the Measurements Problem	WE 6 Special Circuit Design Considerations for the Nuclear Environment
THURS., FEB. 21	8:00 A.M.-4:00 P.M.	.....	Registration	.....	.....	.....	.....	.....	.....	.....	.....
	9:00 A.M.-12:00 Noon	.....	SESSION V Microwave Circuits	SESSION VI [Tutorial] Transistor Switching Circuits	.....	.....	.....	.....	.....	.....	.....
	12:00-1:15 P.M.	.....	.....	LUNCH	.....	.....	.....	.....	.....	.....	.....
	1:30-5:00 P.M.	.....	SESSION VII [Invited] Solid-State Sensing	SESSION VIII Digital Design Techniques	.....	.....	.....	.....	.....	.....	.....
	8:00 P.M.	.....	.....	.....	.....	INFORMAL DISCUSSIONS					
						THE 7 Coherent Optical Techniques and Applications	THE 8 Integrated Digital Logic	THE 9 Broadband Amplifiers	THE 10 Combined Analog-Digital Circuit Techniques	THE 11 Partial Switching of Ferrites	
FRI., FEB. 22	8:00-11:00 A.M.	.....	Registration	.....	.....	.....	.....	.....	.....	.....	.....
	9:00 A.M.-12:00 Noon	.....	SESSION IX Logic II	SESSION X Linear Circuits	.....	.....	.....	.....	.....	.....	.....
	12:00-1:15 P.M.	.....	.....	LUNCH	.....	.....	.....	.....	.....	.....	.....
	1:30-4:30 P.M.	.....	SESSION XI Integrated Circuits	SESSION XII Optoelectronics	.....	.....	.....	.....	.....	.....	.....

Solid-State Circuits Conference